Ultra High Speed Submicron InP/InGaAs SHBTs with 478 GHz f_{max}

Daekyu Yu, Kyungho Lee, and Bumman Kim

Dept. of E. E. Eng. and MARC, Pohang University of Science and Technology

Abstract

InP based single heterojunction bipolar transistors (SHBT's) for high speed circuit applications were fabricated. Typical common emitter DC current gain (β) and BV_{CEO} were about 17 and 10V, respectively. Maximum f_T of 154 GHz and f_{max} of 478 GHz were achieved for 0.5x10 μm^2 emitter size devices at 300 kA/cm^2 collector current density and 1.5V collector bias. This is the highest f_{max} ever reported for any non-transferred substrate HBTs, in so far as we know. This paper highlights aspects of the use of conventional process, and we are in great hopes that offer inherent advantages with direct implications to applications in high-speed electronic circuits.

1. Introduction

As the development of "multimedia" is recent years, high performance HBT's have been used extensively for applications in fiber optical communications and wireless communications. We have developed InP based SHBT's for the applications of high-speed electronic circuits and optoelectronic circuits, etc. Much effort has been made to reduce the base collector capacitance (C_{bc}) and base resistance (R_b) in HBT for a high speed operation since $f_{max} \cong (f_T/8\pi R_b C_{bc})^{1/2}$. The process techniques to reduce R_b and C_{bc} such as isolation implantation of the extrinsic base and collector region [1], laterally etched undercut [2], epi regrowth for the thick base layer [3], L-shaped base electrode [4], and transferred-substrate technique [5] have contributed to the remarkable improvement on the device performance.

However, this paper emphasize practical aspects of using only conventional process. The base resistance (R_b) was minimized by optimizing base contact resistivity. To reduce the C_{bc}, a base-pad-isolation structure was utilized, which can eliminate the capacitance at the base-pad area. Additional, the emitter parasitic resistance and inductance were minimized by using emitter metal widening and air bridge structures.

2. Device Structure and Fabrication

The epitaxial layer of the fabricated HBTs is grown by Solid Source Molecular Beam Epitaxy (SSMBE) on a Fe-doped semi-insulating (100) InP substrate. The layer structure included, from the top, InGaAs emitter contact layer, InGaAlAs graded layers with gradual composition variation, InP emitter (700 Å, Si-doped to 7.0 × 10^{17} cm^{-3}), InGaAs base (400 Å, C-doped to 6.0 × 10^{19} cm^{-3} with 20 Å space), InGaAs collector layer (4000 Å, Si-doped to 2.0 × 10^{16} cm^{-3}), and InGaAs subcollector.

Fabrication started with the evaporation of Ti/Pt/Au emitter contact metals having 0.8 µm width. Emitter etch, which is one of the most delicate steps, was carried out by selective etch of citric-based and subsequent hydrochloric-based wet processes, and the emitter was slightly undercut. After the emitter etch, a self-aligned Pt/Ti/Pt/Au base metal was evaporated [Fig. 1(a)]. The emitter was protected by photo-resist using base contact mask and the base and collector layers were then etched with a citric-based etchant. Next, Polyimide was coated, and then flatly etched without mask using O_2 RIE until the emitter metal was exposed. Next, a Ti/Au emitter widening metal was evaporated [Fig. 1(b)], and second polyimide etch was performed until the epilayer was exposed. Next, SiN was deposited. The SiN was mask etched and the residual polyimide was removed by ashering [Fig. 1(c)] [6]. The subcollector was etched for device isolation. In this etching process between the active base area and the base area for interconnecting base pad were isolated. Next, Ti/Pt/Au collector metal and pad metal were evaporated. Lastly, Au air-bridge formation followed [Fig. 1(d)]. An SEM pictures of the fabricated HBT is shown in Fig. 2. For high speed InP HBTs, the emitter and base metal widths were 0.8 µm and 1 µm. The base-to-emitter spacing measured form SEM picture was about 0.15 µm.

3. Device Measurement Results

The I-V curves of the HBT with 0.5(0.15 µm undercut considered) × 10 μm^2 emitter area were measured and depicted in Fig. 3. As shown, the common-emitter dc current gain (β) of the HBTs are about 17 at a collector current density of 1 × 10^5 A/cm^2. The breakdown voltages of the HBTs at an open base, BV_{CEO} are 10 V. The Base sheet resistance of 482 Ω/□ and specific contact resistivity of 2.5 × 10^{-7} Ω•cm^2 were measured using Transmission Line Measurement (TLM). The transfer length, L_T, expressed as $(\rho_{BC}/R_{SB})^{1/2}$ is 0.228 µm, therefore, the base contact resistance was maintained low. The microwave performance of the fabricated HBTs was characterized by on-wafer S-parameter measurements from 0.5 to 40 GHz using a Agilent 8510C network analyzer. The frequency dependence of current gain, Mason's unilateral gain, and maximum stable gain/maximum available gain was shown in Fig. 4. The f_T and f_{max} were obtained assuming a –20 dB/decade frequency dependence of the current gain and Mason's unilateral gain, respectively. The f_T and f_{max} of HBT are 154.5 GHz and 478.4 GHz (Gain ≅ 21.7 dB at 40GHz), respectively, at I_C=15.2 mA and V_{CE}=1.5 V. This was the highest f_{max} ever reported for any non-transferred substrate HBTs, in so far as we know. Also, Fig 5 shows the dependence of f_T and f_{max} on collector current density at V_{CE}=1.5 V.

4. Conclusions

The high-speed InP/InGaAs SHBTs were fabricated by using the developed POSTECH process. This process includes a base-pad isolation, emitter metal widening, and air bridge structures. High frequency performance of f_T = 154.5 GHz and f_{max} = 478.4 GHz was obtained for a 0.5 × 10 μm^2 emitter. This is the highest f_{max} ever reported for any non-transferred substrate HBTs. This conventional process is a promising technique for high-speed electronic circuits. Also, as the device is scaled down, the device RF performance will be more and more progressed.

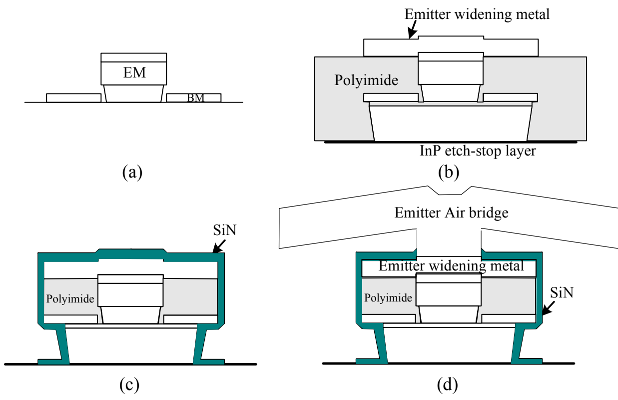

Fig. 1. Process flow (a) Self-aligned base metal, (b) Emitter metal widening, (c) SiN passivation, (d) Emitter Air bridge

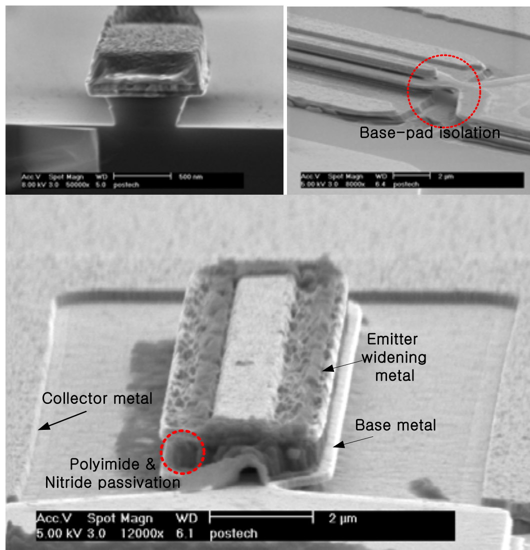

Fig. 2. SEM pictures for the fabricated HBT with a 0.8(effective 0.5) × 10 μm² emitter.

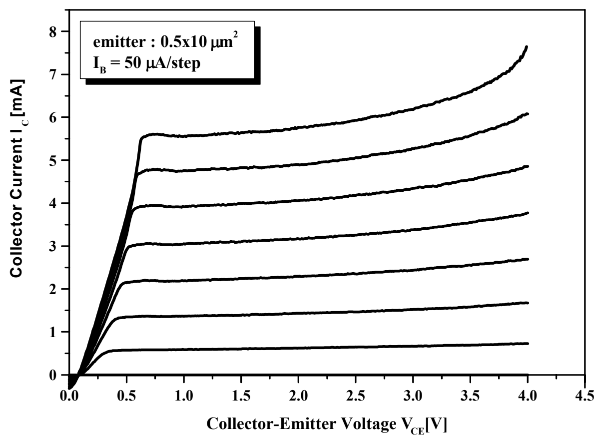

Fig. 3. Common emitter I_C-V_{CE} characteristics for the fabricated HBT with a 0.5 × 10 μm² emitter

5. References

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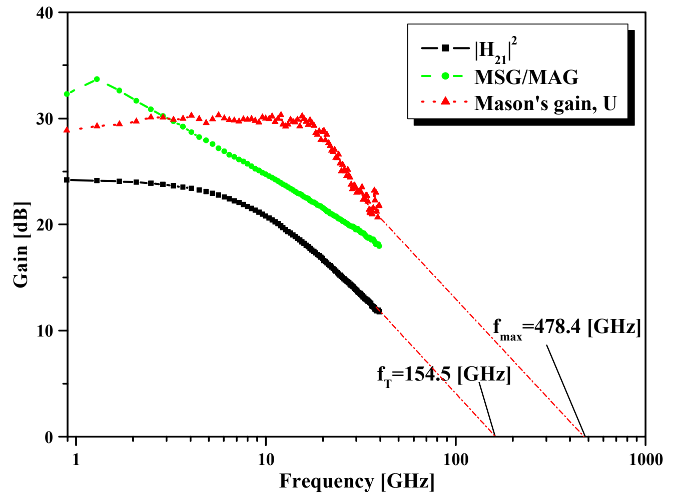

Fig. 4. Frequency dependencies of $|h_{21}|^2$, MSG/MAG, and Mason's gain for the fabricated HBT with a 0.5 × 10 μm² emitter.

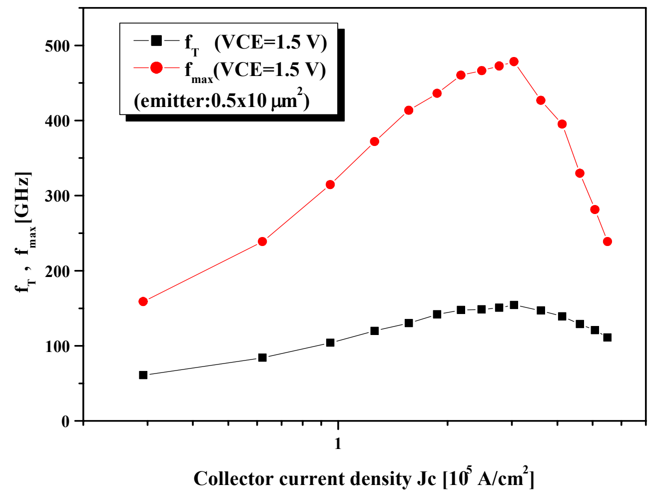

Fig. 5. Dependence of f_T and f_{max} on collector current density for the fabricated HBT with a 0.5 × 10 μm² emitter