# 밀리미터파 응용을 위한 $f_T$=321GHz, $f_{max}$=190GHz를 가지는 InP/InGaAs/InP DHBT의 제작

최광식, 유대규, 이경호, 윤제형, 김범만
포항공과대학교 전자전기공학과
tel) 054-279-5584 / fax) 054-279-8115

# Fabrication of InP/InGaAs/InP DHBT with 321 GHz $f_T$ and 190 GHz $f_{max}$ for Millimeter-wave applications

**Kwangsik Choi, Daekyu Yu, Kyungho Lee, Jehyung Yoon, and Bumman Kim**
**Dept. of E. E. Eng. Pohang University of Science and Technology**
**E-mail : torisis@postech.ac.kr**

**Abstract** - InP based double heterojunction bipolar transistor (DHBT) for RF circuit applications is fabricated using SSMBE grown DHBT epi. In order to improve high speed performances, we are focused on the vertical scaling and parasitic reduction. Maximum $f_T$ of 321 GHz and $f_{max}$ of 190 GHz are achieved for $1.0 \times 10\ \mu m^2$ devices at collector current density of 324 $kA/cm^2$ and collector voltage of 1.3 V. Typical common emitter DC current gain ($\beta$) and common emitter breakdown voltage ($BV_{CEO}$) are about 35 and 5.7 V, respectively. It is one of the highest $f_T$ ever reported for any emitter-up bipolar transistors. This device technology supports the promising potential of InP/InGaAs/InP DHBTs for commercial millimeter-wave applications.

## 1. Introduction

In recent years, the millimeter-wave band system have gained increased interest for system applications due to its wide frequency spectrum, high data rate, and compact sized hardware solutions. The majority of millimeter-wave circuits have been implemented in InP-based or GaAs-based transistor technologies. For high frequency applications, the operation frequency of transistor is pushed steadily in higher frequencies. Among the device technologies, InP based HBTs deliver superior high speed performances to any other devices. To achieve the high cutoff frequency ($f_T$) and the maximum oscillation frequency ($f_{max}$), which is the figure of merits for high speed performances, the HBT design must: achieve low base and collector transit times for high $f_T$, balance the reduction in collector transit time with the reduction in breakdown voltage and an increase in $C_{CB}$, minimize the base resistance ($R_B$), minimize the extrinsic $C_{CB}$, and minimize the emitter contact resistance ($R_E$). HBTs with high $f_T$ and $f_{max}$ are reported in many literatures [1-3]. While InP/InGaAs single heterojunction bipolar transistors (SHBTs) have low breakdown voltages due to InGaAs collector layer, double heterojunction bipolar transistors (DHBTs) have high speed properties and high breakdown voltage at the same time using InP collector layer.

In this paper, high speed InP/InGaAs/InP DHBT has been developed. For the high $f_T$, the vertical scaling by thin base and collector is employed and the base layer is compositionally graded.

For the high $f_{max}$, the base-collector junction capacitance ($C_{CB}$) is reduced by collector undercut process and base pad isolation because $f_{max} \cong (f_T/8\pi R_B C_{CB})^{1/2}$. And the emitter metal widening technique is employed to reduce emitter parasitic resistance. With those techniques, the DHBT with 321 GHz $f_T$, 190 GHz $f_{max}$, and 5.7 V $BV_{CEO}$ is fabricated.

## 2. Design of High Speed DHBT

Table 1. Epi layer description of the fabricated DHBT

| Layer Description | Composition | Conc. [$cm^{-3}$] | Thickness [Å] |
|---|---|---|---|
| Emitter Cap | $In_{0.53}Ga_{0.47}As$ | 3E19 | 1000 |
| | $In_{(x)}Ga_{(y)}Al_{(1-x-y)}As$ | 3E19 | 200 |
| | InP | 1E19 | 900 |
| Emitter | InP | 7E17 | 700 |
| Space | $In_{0.46}Ga_{0.54}As$ | undoped | 20 |
| Base | $In_{(x)}Ga_{(1-x)}As$ | 8E19 | 250 |
| Setback | $In_{0.53}Ga_{0.47}As$ | 2E16 | 200 |
| Collector | $In_{(x)}Ga_{(y)}Al_{(1-x-y)}As$ | 2E16 | 300 |
| Delta Doping | InP | 1E18 | 30 |
| Collector | InP | 2E16 | 1000 |
| Sub Collector | InP | 1E19 | 200 |
| | $In_{0.53}Ga_{0.47}As$ | 3E19 | 3000 |
| | InP | 1E19 | 100 |
| | $In_{0.53}Ga_{0.47}As$ | 3E19 | 3000 |
| Substrate | Fe-doped Semi-insulated InP | | |

The whole layer description is shown in Table 1. The epitaxial layers of the fabricated DHBT are grown by Solid Source Molecular Beam Epitaxy (SSMBE) on a Fe-doped semi-insulating (100) InP substrate by IntelliEPI Inc. The $In_{(x)}Ga_{(y)}Al_{(1-x-y)}As$ layer in emitter cap layers is linearly compositional graded, where the In mole fraction is fixed, x = 0.53, and the Ga mole fraction is linearly decreased from y = 0.47 to 0.20 toward the base to reduce the conduction band discontinuity between emitter cap layers.

The base layer is highly doped to 8E19 $cm^{-3}$ to obtain a low base sheet resistance. But this high doping concentration causes the low DC current gain ($\beta$) due to Auger recombination in the base. To compensate the low $\beta$, $In_{(x)}Ga_{(1-x)}As$ base layer is designed to be thin to 250 Å and linearly compositional graded from x = 0.46 to 0.53 toward collector. This scheme, thin and graded base, contributes to the improved $f_T$.

The InP/InGaAs/InP DHBT has the current blocking problem because of conduction band discontinuity between base (InGaAs) and collector (InP). Therefore the bandgap engineering (or grading scheme) is another important issue for higher $f_T$, especially for DHBT. So far various design schemes have been proposed to avoid the current blocking effect, such as those using a composite collector [4], InGaAsP graded layers [5], and staggered band lineup of InP/GaAsSb/InP [6]. In our case, to remove the discontinuity at the conduction band, the linearly compositional graded $In_{(x)}Ga_{(y)}Al_{(1-x-y)}As$ layer is employed at the collector, similar to the emitter cap design with $In_{0.53}Ga_{0.47}As$ setback layer. Additionally, to compensate the reverse electric field induced by the $In_{(x)}Ga_{(y)}Al_{(1-x-y)}As$ layer, delta doped InP layer is introduced within collector layers [7]. Total collector thickness of 1500 Å is employed for small space-charge time ($\tau_{sc}$). Sub-collector layers are designed suitable to the undercut process explained in reference [8].

## 3. Device Fabrication

We have fabricated DHBT using a conventional mesa structure. The summary of process sequence follows that an emitter contact metal is evaporated, the emitter mesa is etched with emitter metal mask, a self-aligned base metal is evaporated, a base and collector mesa is formed by wet etching, the polyimide is coated for passivation and flattened by $O_2$ RIE until the emitter metal is exposed, an emitter widening metal is evaporated, residual polyimide is removed by $O_2$ RIE, sub-collector is etched by wet etchant for device isolation and base pad isolation, a

collector and pad metals are evaporated, and a Au plating is carried out. The comprehensive process sequence can be found in [3]. In this work, the emitter and base metal width is 1.0μm and 1.0 μm. The collector undercut process is carried out after base and collector mesa formation using method suggested at [8]. The schematic cross-section of DHBT is depicted in Fig. 1.

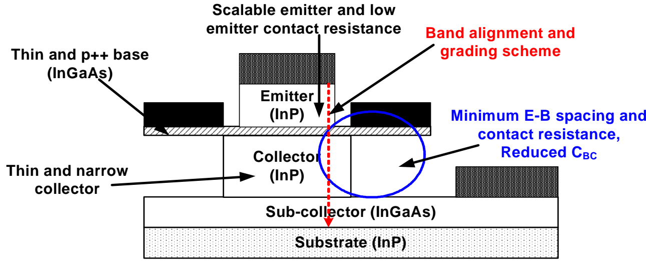


Fig. 1. Schematic of high speed InP DHBT

## 4. Device Results

### A. DC performance

The measured I-V curve of the fabricated DHBT with $1.0 \times 10\ \mu m^2$ emitter area is depicted in Fig. 2. As shown, the common-emitter dc current gain (β) of the DHBTs is about 35 at a collector current density of 200 $KA/cm^2$. The breakdown voltage of the device at an open base, $BV_{CEO}$, is 5.7 V. The sheet resistance and specific contact resistivity of base is 872 Ω/□ and $1.4 \times 10^{-6}\ \Omega \cdot cm^2$, respectively, measured using transmission line measurement (TLM). The transfer length, $L_T$, expressed as $(\rho_{BC}/R_{SB})^{1/2}$ is 0.4 μm and the base contact resistance is maintained low.

### B. Microwave performance

The microwave performance of the fabricated DHBT is characterized by on-wafer S-parameter measurements from 0.5 to 40 GHz using a HP8510C vector network analyzer (VNA). The frequency dependences of current gain, Mason's unilateral gain, and maximum stable gain/maximum available gain are shown in Fig. 3. The $f_T$ and $f_{max}$ are obtained assuming a –20 dB/decade frequency dependence of the current gain and Mason's unilateral gain, respectively. Fig. 4 shows the dependences of $f_T$ and $f_{max}$ on collector current density at $V_{CE}$ = 1.3 V. The $f_T$ and $f_{max}$ of DHBT are 321 GHz and 190 GHz at $I_C$ = 26 mA and $V_{CE}$ = 1.3 V. The forward transit time ($\tau_F = \tau_b + \tau_{sc}$) associated with this device is calculated to be $\tau_F$ = 0.39 ps from the measured S-parameters. This high cutoff frequency is obtained by applying vertical scaling scheme at the base and collector epitaxial structure, which leads to the reduced base transit time ($\tau_b$) and collector delay time ($\tau_{sc}$). Also, the grading of base layer leads to the further reduced base $\tau_b$.

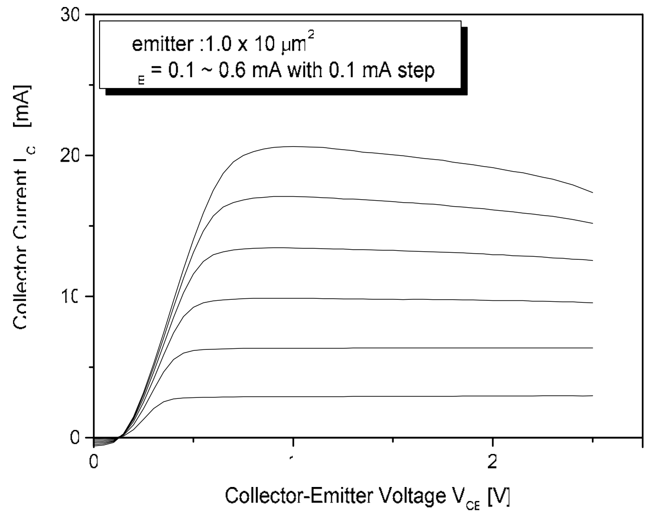


Fig. 2. Common emitter $I_C$-$V_{CE}$ characteristics of the fabricated DHBT with a $1.0 \times 10\ \mu m^2$ emitter

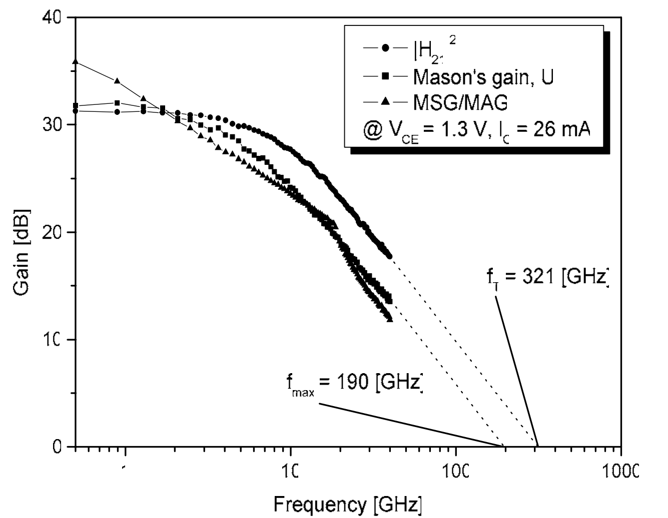


Fig. 3. Frequency dependences of $|H_{21}|^2$, Mason's gain, and MSG/MAG for the fabricated DHBT with a $1.0 \times 10\ \mu m^2$ emitter

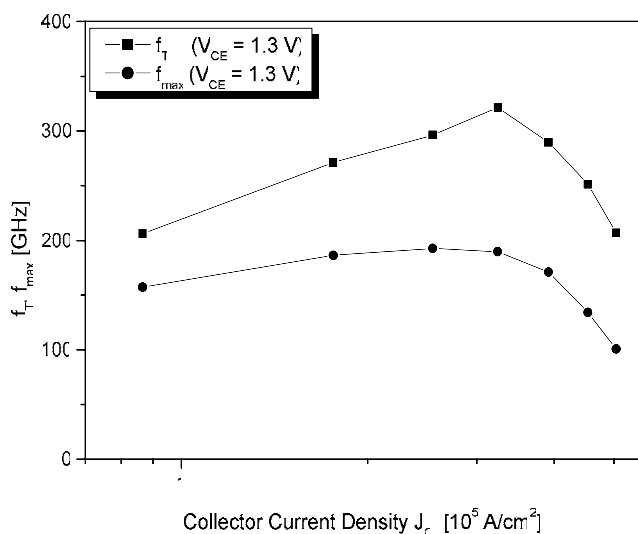


Fig. 4. Dependences of $f_T$ and $f_{max}$ on collector current density for the fabricated DHBT with a $1.0 \times 10\ \mu m^2$ emitter

## 5. Conclusions

The high-speed InP based DHBT is fabricated using a simple process technique. High frequency performances of $f_T$ = 321 GHz and $f_{max}$ = 190 GHz are obtained for a $1.0 \times 10\ \mu m^2$ emitter-up DHBT. The high cutoff frequency can be achieved by using thin base/collector layer design and reducing parasitic. The emitter metal widening, base-pad-isolation, and collector undercut process are employed to reduce parasitic. Finally the further improvement of $f_{max}$ is strongly expected by lateral scaling in the geometrical layout.

## 6. References

[1] Z. Griffith, *et. al*, "InGaAs-InP mesa DHBTs with simultaneously high fτ and fmax and low $C_{cb}/I_c$ ratio," *IEEE Electron Device Letters*, Vol.25, no.5, pp. 250-252, 2004.

[2] W. Hafez, *et. al*,, "Vertical scaling of 0.25um emitter InP/InGaAs single heterojunction bipolar transistors with $f_T$ of 452 GHz," *IEEE Electron Device Letters*, Vol.24, no.7, pp. 436-438, 2003.

[3] D. Yu, K. *et. al*, "Realization of High-Speed InP SHBTs using Novel but Simple Techniques for Parasitic Reduction," *Indium Phosphide and Related Materials (IPRM)*, pp. 753-756, 2004.

[4] A. Feygenson, R. A. Hamm, *et. al*, "High Speed InGaAs/InP Composite Collector Bipolar Transistors," *DRC Dig.,* pp. 99-100, 1992.

[5] M. Ida, K. Kurishima, *et. al*, "InP/InGaAs DHBTs with 341-GHz $f_T$ at high current density of over 800 kA/cm$^2$," *IEEE IEDM Tech. Dig.,* pp. 776-779, 2001.

[6] C. R. Bolognesi, *et. al*, "Investigation of High-Current Effects in Staggered Lineup InP/GaAsSb/InP Hetero-junction Bipolar Transistors: Temperature Characterization and Comparison to Conventional Type-I HBTs and DHBTs," *IEEE IEDM Tech. Dig.,* pp. 768-771, 2001.

[7] T. R. Block, *et. al*, "Molecular beam epitaxy growth and characterization of InGaAlAs-collector heterojunction bipolar transistors with 140 GHz $f_{max}$ and 20 V breakdown," *J. Vac. Sci. Technol.*, B 14(3), pp. 2221-2224, 1996.

[8] Y. Jeong, *et. al*, "$f_{max}$ enhancement in InP-based DHBTs using a new lateral reverse-etching technique," *Indium Phosphide and Related Materials (IPRM)*, pp. 22-25, 2003.