Ultra High-Speed 0.25-μm Emitter InP-InGaAs SHBTs with f_{max} of 687 GHz

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ABSTACT

We have developed novel but simple process techniques for high speed InP SHBTs. For parasitic reduction, the collector layer is undercut using an etch-stop layer, the base pad is isolated, and the emitter metal is widened using thick plated gold. For transit time reduction, the SHBT employs InGaAs base with graded In-composition and InGaAlAs emitter setback with graded Al-composition. Maximum extrapolated f_{max} of about 687 GHz with f_T of 215 GHz is achieved for 0.25 × 8 μm^2 emitter area devices at I_C = 8 mA and V_{CE} = 1.5 V. Within the author's knowledge, this is the highest f_{max} ever reported for any non-transferred substrate HBTs. These data clearly show that the optimized conventional process can offer direct implementation of InP HBT for ultra high-speed electronic circuit.

I. Introduction

In recent years, the millimeter-wave band has gained increased interest for system applications due to its wide frequency spectrum, high data rate, and compact sized hardware solutions. Application areas based on the advanced transistor technologies are extended to commercial fields including fiber-optic network, mobile wide-band cellular systems, fixed wireless broad-band access systems, wireless local area networks, and wireless vehicle and traffic information systems.

The majority of millimeter-wave circuits have been implemented in InP-based or GaAs-based transistor technologies. HEMTs have historically been used for high-speed applications because of their relatively high current gain cut-off frequency (f_T) and maximum oscillation frequency (f_{max}). Highly scaled Si-based transistors such as SiGe HBT and CMOS will the challenge InP-based transistors for millimeter-wave markets, accompanied by the ability to integrate high degree of functionality on a single chip. However, in the recent year, InP-based HBTs deliver superior performance to any other transistors. The fundamental material properties of InP are exceptionally well suited to high-speed HBTs for digital, microwave, and opto-electronic applications. The InP-based HBTs promise higher current gain cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) as the devices are vertically and laterally scaled down. However, the increase in f_T by vertical scaling of epilayer may come at the expense of f_{max} if parasitic components are not carefully controlled. Among the parasitic components, collector base capacitance (C_{CB}) is the most importance parameter as

the collector layer is vertically scaled down. A large part of C_{CB} originates from the extrinsic base area in the mesa structured HBT. A simple collector undercut is the most widely used technique to reduce C_{CB} of InP Double-HBTs (DHBTs) due to the selective etching nature [1] - [3]. The air filling gap between the base layer underneath the base contacts and a subcollector has the lowest dielectric constant of unity. In the case of Single-HBTs (SHBTs), however, the base layer is also etched during the undercut process because the selective etch cannot be employed. Several undercut techniques have been employed to reduce C_{CB} in SHBTs [4] [5] but yields for the processes are usually poor due to the complicated processes, especially for scaled-down devices.

In this paper, we report a high speed SHBT based on a conventional mesa structure with the 0.25 μm emitter width and the development of novel but simple process techniques for reduction of not only the C_{CB} but also other parasitics for realization of the high speed InP SHBTs. To reduce C_{CB}, the collector layer is undercut using an etch-stop layer in the SHBT, similar to the undercut process in the DHBT and a base-pad-isolation structure is utilized, which can eliminate the capacitance at the base-pad area. The base resistance (R_B) is minimized by maximizing the base doping (8.0×10^{19} cm^{-3}), placing the base ohmic contact as close to the emitter junction as possible and optimizing the base contact resistivity (ρ_{BC}). Additionally, the emitter parasitic resistance and inductance are minimized by using emitter metal widening and air-bridge structures with plated thick gold. These optimized conventional processes deliver the extremely high speed InP SHBTs.

II. Scaling Law of HBT

1. Review of the Fundamental Scaling Theory

Two measures of the high frequency performance of HBT are given by

$$f_{\max} = \sqrt{\frac{f_T}{8\pi R_B C_{CB}}} \qquad (1)$$

$$\frac{1}{2\pi f_T} = \frac{C_{JE} + C_{CB}}{g_m} + \tau_B + \tau_{SC} + (R_E + R_C)\, C_{CB} \qquad (2)$$

where τ_B and τ_{SC} are base and collector transit times, respectively. C_{JE} *and* C_{CB} are base-emitter and collector-base junction capacitances, respectively. g_m (= qI_C/kT) is transconductance. And R_E, R_B and R_C are emitter, base and collector resistances.

The conventional mesa structure HBT is illustrated in Fig 1. A large-sized HBT is scaled down by a scaling factor (γ) to produce a smaller HBT with smaller resistance, inductance and capacitance. To ensure that the operation bandwidth increases by γ : 1 for all digital and analog circuits, all transit times and all capacitances must be reduced by γ : 1, while maintaining the values for all resistances, transconductance, and collector bias current (I_C). These relationships are summarized in Table I along with the scaling behavior of the important physical parameters.

2. Scaling Limits on HBT in Conventional HBT Process

1) Limit to the Enhancement of f_{max} (ρ_{BC}, $W_{J,BC}$ and $W_{S,EB}$)

As shown in Eq. (1), the base resistance (R_B) and collector-base capacitance (C_{CB}) are very

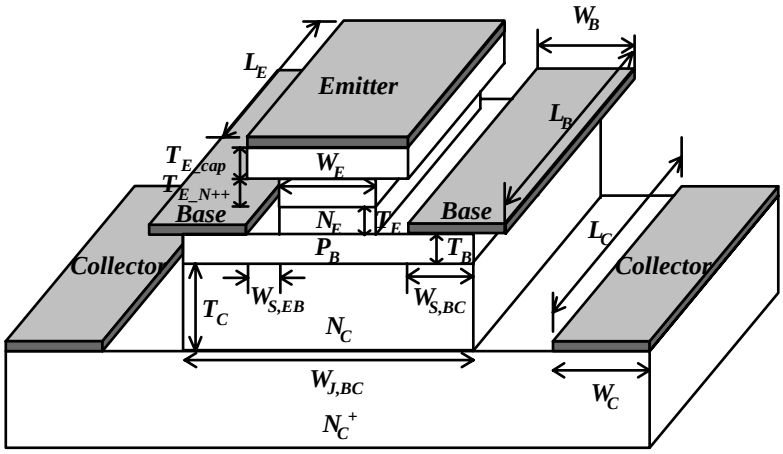


Fig. 1. The structure of conventional mesa type HBT

TABLE I. FUNDAMENTAL SCALING RULES ON HBT

Physical Parameters	Symbol	Scaling Factor
Emitter thick.	T_E	γ^{0}
Emitter doping	N_E	γ^{1}
Emitter-base junction width	W_E	γ^{-2}
Emitter-base spacing	$W_{S,EB}$	γ^{-1}
Emitter-base junction length	L_E	γ^{0}
Emitter contact resistivity	ρ_{EC}	γ^{-2}
Base thickness	T_B	$\gamma^{-0.5}$
(Base doping) x (Base hole mobility)	(P_B) x (μ_{PB})	$\approx \gamma^{0.5}$
Base contact width	W_B	γ^{-2}
Base contact length	L_B	γ^{0}
Base contact resistivity	ρ_{BC}	γ^{-2}
Collector thickness	T_C	γ^{-1}
Collector doping	N_C	γ^{0}
Collector-base junction width	$W_{J,BC}$	γ^{-2}
Collector-base junction length	L_C	γ^{0}
Collector current	I_C	γ^{0}
Collector current density	J_C	γ^{2}
Bias voltage	V_{CE}, v_{ce}	γ^{0}

important parameters for achieving high maximum oscillation frequency (f_{max}). C_{CB} can be minimized by narrowing base-collector junction area or the base ohmic contact width. However, this reduction

must be carried out without increase of the base specific contact resistivity (ρ_{BC}) because R_B of the device can be increased drastically as the base contact width becomes narrower than the contact transfer distance L_T($=\sqrt{\rho_{BC}/R_{SB}}$). The contact resistivity of InGaAs (p+) has been reached to as low as 1~2 x 10^{-7} Ω·cm^2 and it is very hard to reduce any further. Therefore, both ρ_{BC} and $W_{J,BC}$ (collector base junction width) cannot follow the scaling factor of γ^{-2} rule. And, there is a trade-off for the scaling of R_B and C_{CB} in the conventional mesa-type HBT. Also, Self-Aligned Base Metal (SABM) technology has been widely used to reduce the base resistance. In the conventional HBT process with wet chemical etching using an emitter electrode mask, there is a practical limit to the minimum size of the emitter-base spacing ($W_{S,EB}$), preventing the scaling.

2) Limit to the Enhancement of f_T (ρ_{EC}, J_C and BV_{CEO})

Eq. (2) shows that, to improve the cut-off frequency, not only the base and collector transit-times are reduced through vertically scaling, but also the collector current density (J_c) should be increased and R_E be reduced. However, due to base push-out (or Kirk effect) at high current densities, the effective base thickness is increased, resulting in an increase in the carrier transit time and a decrease in f_T. To mitigate the problem, the collector layer should be highly doped and thin. The penalty for the collector is an increase in the collector-base capacitance and reduction of breakdown voltage. Therefore, there are the trade-offs for J_C, C_{CB} and breakdown voltage (BV_{CEO}) in the conventional mesa-type HBT. Similarly, ρ_{BC} and ρ_{EC} cannot be reduced continuously, following the scaling factor of γ^{-2}.

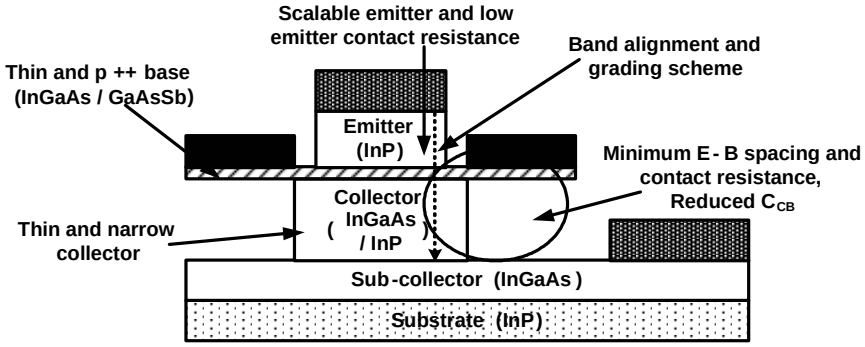


Fig. 2. Schematic of high speed HBT (SHBT & DHBT)

3) Design Issues for High Speed HBT

The schematic cross-section and high speed optimization issues are described in Fig. 2. To get high f_T and f_{max}, the HBT design must: achieve low base and collector transit times for high f_T, trade properly off the required fast collector transit time with the low breakdown voltage (BV_{CEO}) and high C_{CB}, minimize R_B, extrinsic C_{CB}, and R_E. The general approach to improve the f_T is the use of thin base/collector layers. However, the approach can only be employed at the expense of the reduced f_{max} due to the increased R_B and C_{CB}, and may not be suitable for the applications demanding both high f_T and f_{max} [6].

In this point of view, bandgap engineering (or grading scheme) is another important issue for higher f_T, especially for DHBTs. The compositional and/or doping graded base layer is very helpful for reducing the base transit time. Also, various grading schemes for the base-collector junction have been proposed to avoid the current blocking effect, such as composite collector [7], pn-pair doping [8], InGaAsP graded layers [9], staggered band lineup of InP/GaAsSb/InP [10], and optimization of

ballastic carrier transport. The emitter resistance and inductance should be minimized to reduce the parasitic delay. The R_B is the most important factor for higher f_{max} and has three components: contact resistance, gap resistance, and intrinsic spread resistance. The minimum base resistance can be achieved by highly doped base layer, scaling of emitter width, self-alignment, and optimization of base ohmic contact. The C_{CB} reduction technique, independent of base contact width, is a compulsory for achieving both high f_T and f_{max}.

III. Design and Fabrication

TABLE II. EPITAXIAL LAYER STRUCTURE OF FABRICATED HBTs

Layer	Composition	Doping (cm^{-3})	Thickness (Å)
Emitter-cap	In(x)GaAs : x=0.53	$> 1 \times 10^{19}$	1000
	In(x)Ga(y)Al(1-x-y)As x=0.53, y=0.19~0.47	$> 1 \times 10^{19}$	200
	InP	1×10^{19}	900
Emitter	InP	7×10^{17}	700
Spacer	InGaAs : x=0.46	Undoped	20
Base	In(x)GaAs x=0.46~0.53	8×10^{19}	400
Collector	InGaAs : x=0.53	2×10^{16}	1000
Insertion	InP	2×10^{16}	50
Collector	InGaAs : x=0.53	2×10^{16}	1500
Etch-stop	InP	$> 1 \times 10^{19}$	100
Subcollector	InGaAs : x=0.53	$> 1 \times 10^{19}$	6000

The epitaxial layer of the HBTs is grown by Solid Source Molecular Beam Epitaxy on a Fe-doped semi-insulating (100) InP substrate. The layer structure includes, from the top, InGaAs emitter contact

layer, InGaAlAs graded layer, InP emitter layer (700 Å, Si-doped to 7.0 × 10^{17} cm^{-3}), InGaAs base layer with Indium mole fraction graded from of 0.46 to 0.53 (400 Å, C-doped to 8.0 × 10^{19} cm^{-3} with 20 Å spacer), InGaAs collector layer (2500 Å, Si-doped to 2.0 × 10^{16} cm^{-3}), and InGaAs subcollector layer(6000 Å, Si-doped to 1.0 × 10^{19} cm^{-3}). The details are outlined in Table II.

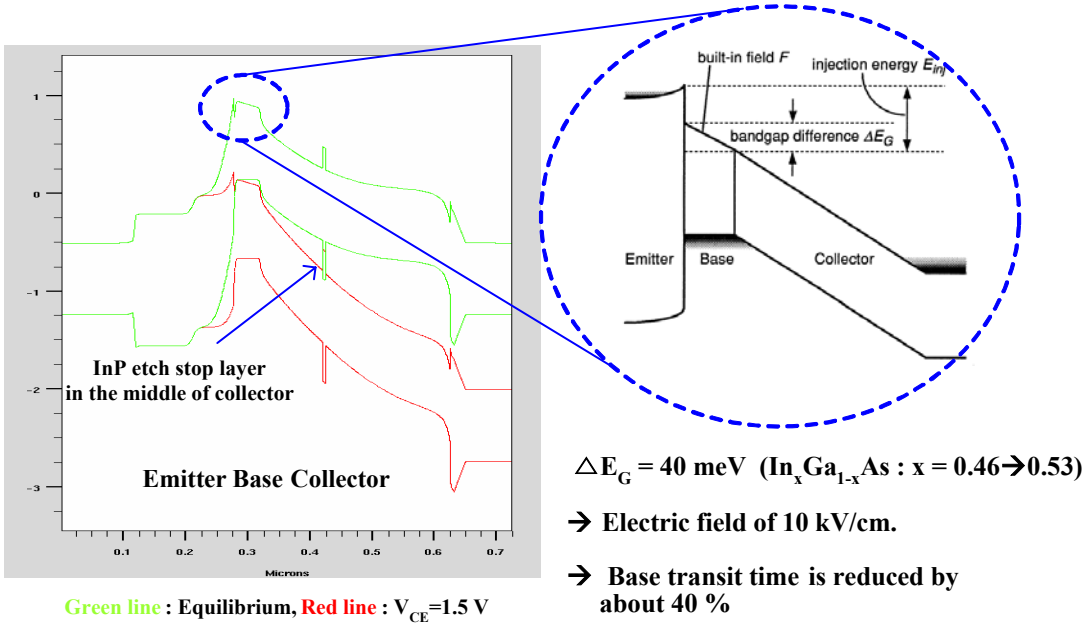


Fig. 3. The energy band diagram of the fabricated HBT having the Indium mole fraction graded ($In_xGa_{1-x}As$: x = 0.46→0.53) base layer.

The conduction band discontinuity (ΔE_C) between InGaAs emitter-cap layer and InP emitter layer is suppressed by using the compositional graded InGaAlAs layer. Also, the potential drop across the Indium mole fraction graded base is 40 meV, which corresponds to an electric field of 10 kV/cm. The calculated base transit time (τ_B) is reduced by about 40 % [11]. Fig 3 shows the energy band diagram of the device with the Indium mole fraction graded base layer calculated using the ATLAS device

simulator.

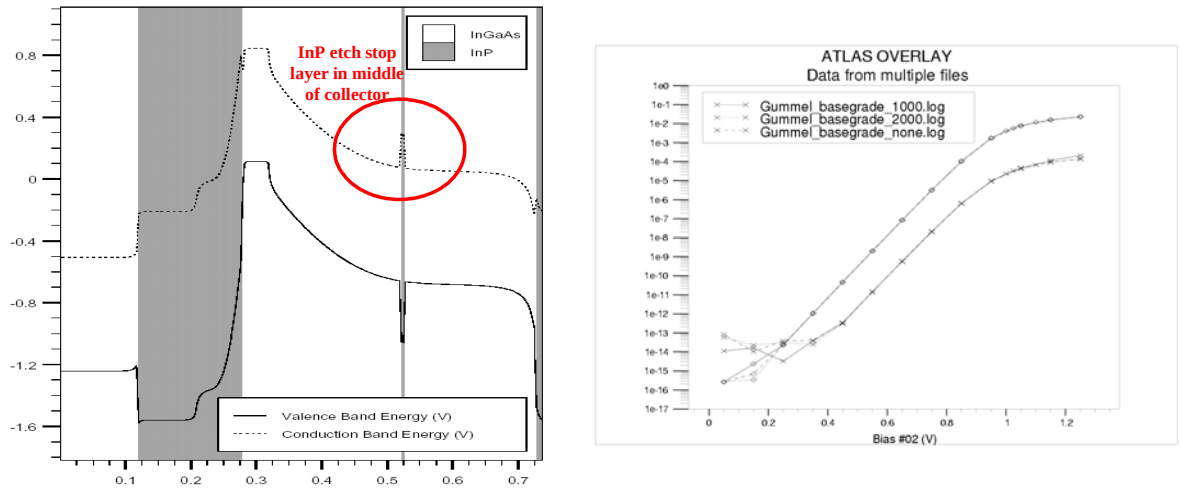


Fig. 4. Energy band diagram for Epi. with insertion etch stop layer and effect of collector insertion layer on DC Characteristic of HBT.

Lastly, an important addition is two InP etch-stop layers for undercut process in SHBTs. First, DC Characteristics are almost identical for the devices of the with/without collector insertion layer as shown Fig. 4. Due to the etch-stop layers, the undercut process similar to the DHBT can be employed without having any base layer etch problem. Therefore, the base contact resistance is maintained low. Fig. 5 compares the f_{max} of the new undercut process and conventional undercut process devices calculated using our own models. As shown, f_{max} of above 700 GHz can be achieved using the new process for the deep submicron scaled device.

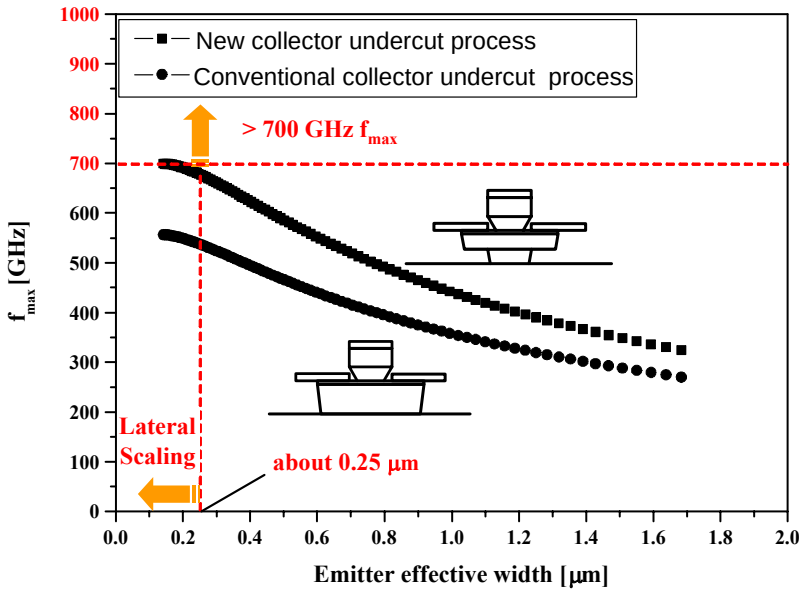


Fig. 5. Comparison of the new collector undercut device and conventional device for scaled down devices

In Fig. 6, whole process flow is shown. Fundamentally, the device are fabricated using a standard mesa process. Fabrication started with the evaporation of Ti/Pt/Au emitter contact metals having 0.5 μm width. Emitter etch, which is one of the most delicate steps, is carried out by selective etch of citric-based and subsequent hydrochloric-based wet processes, and the emitter is slightly undercut as shown Fig. 7. After the emitter etch, a self-aligned Pt/Ti/Pt/Au base metal is evaporated [Fig. 6(a)]. The emitter is protected by photo-resist using base contact mask and the base and collector layers are then etched with a citric-based etchant. In this etching process, the collector layer is undercut simultaneously.. Next, polyimide is coated, and then flatly etched without mask using O_2 RIE until the emitter metal is exposed. Next, a Ti/Au emitter widening metal is evaporated [Fig. 6(b)], and the

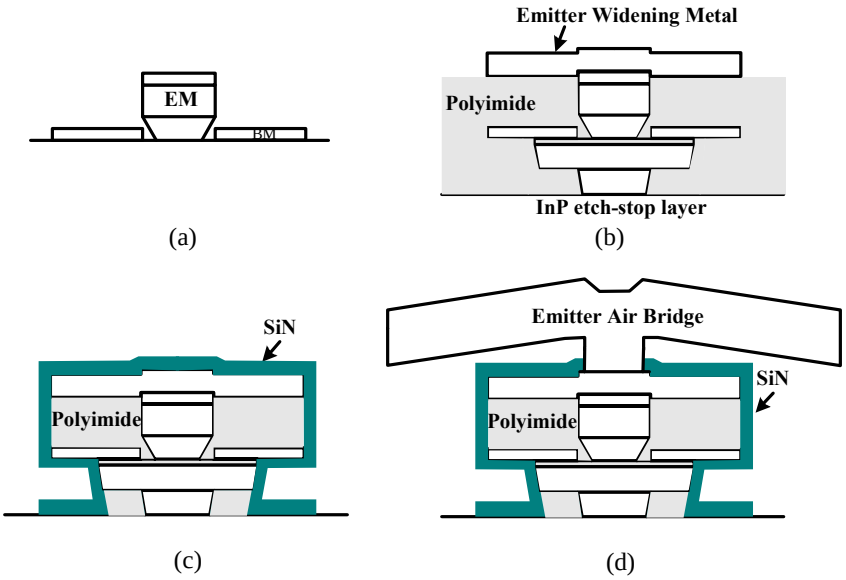


Fig. 6. Process flow (a) Self-aligned base metal, (b) Emitter metal widening, (c) SiN passivation, (d) Emitter air bridge

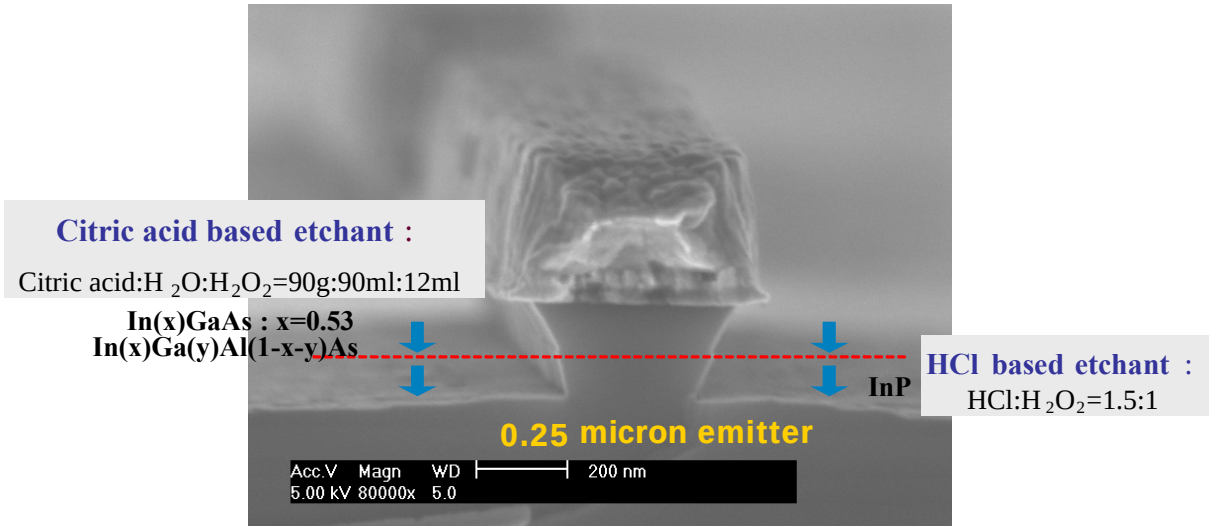
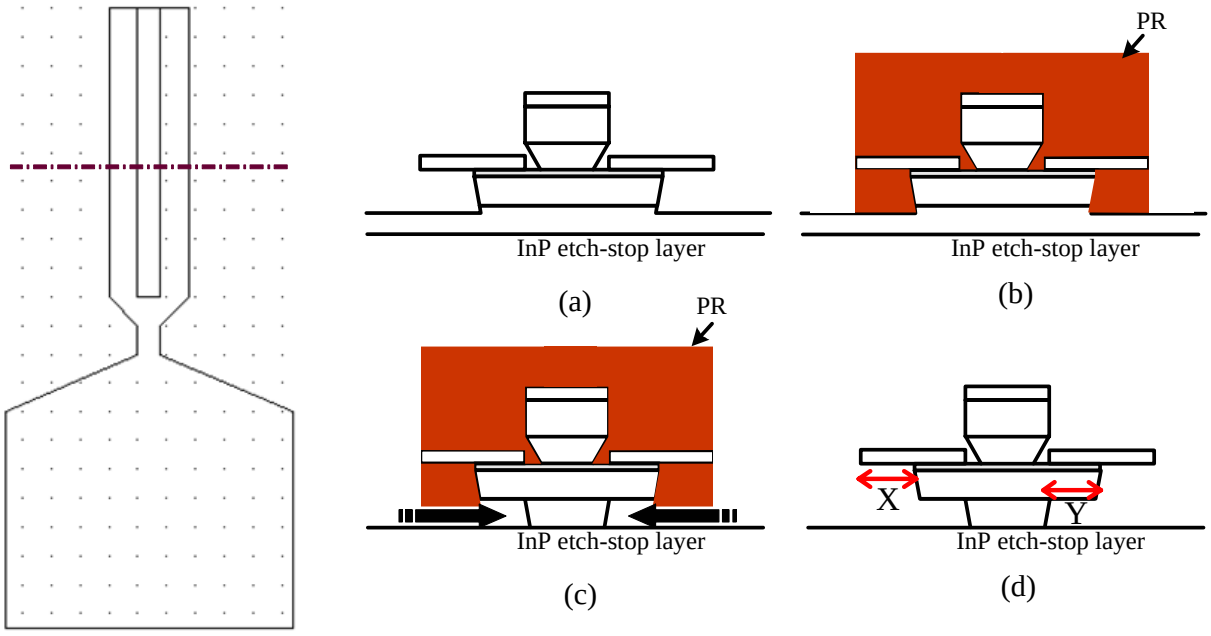


Fig.7. SEM pictures for the fabricated HBT having a 0.25 μm effective emitter width after emitter etch.

second polyimide etch is performed until the epilayer is exposed. Next, the SiN is deposited. The SiN is mask etched and the residual polyimide is removed by ashering [Fig. 6(c)]. The subcollector is

etched for device isolation. In this etching process, the active base area and the base area for interconnecting base pad are isolated. Next, Ti/Pt/Au collector metal and pad metal are evaporated. Lastly, Au air-bridge formation is followed [Fig. 6(d)]. The detailed process can be referred to our paper [12].



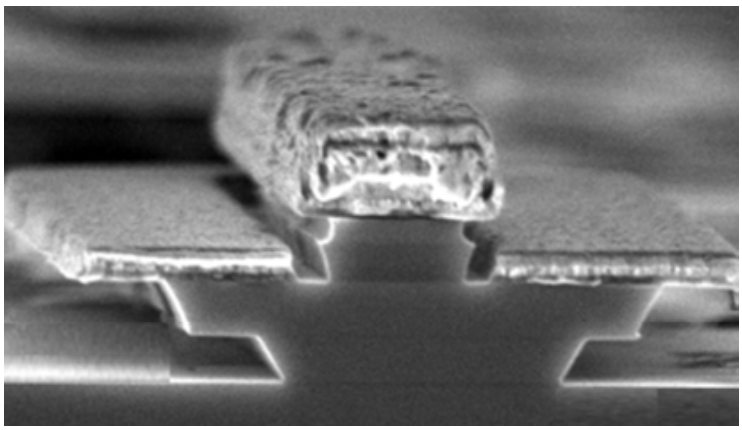


Fig. 8. New collector undercut process flow and SEM pictures

(a) 1st BC etching, (b) PR protection, (c) 2nd BC etching (d) PR strip

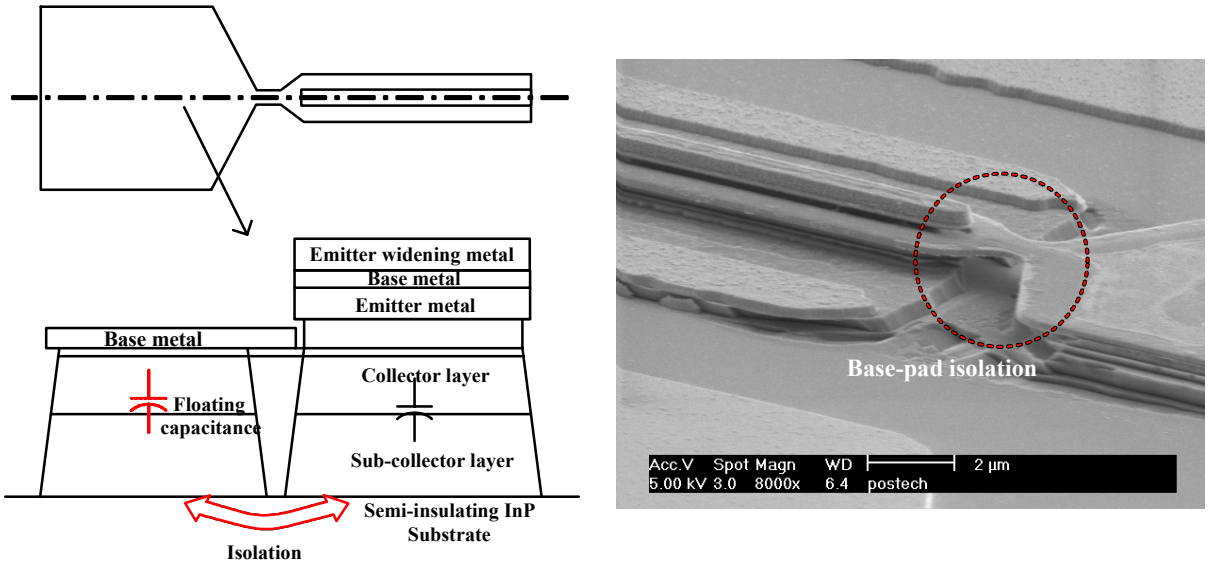


Fig. 9. Base pad isolation structure

Fig. 8 and 9 show the new undercut process and the base-pad isolation structure for minimizing R_B and C_{CB}, respectively. In Fig. 8(d), X is determined by trade-off of R_B and C_{CB} and Y is adjusted to have similar widths for emitter-base and base-collector junctions.

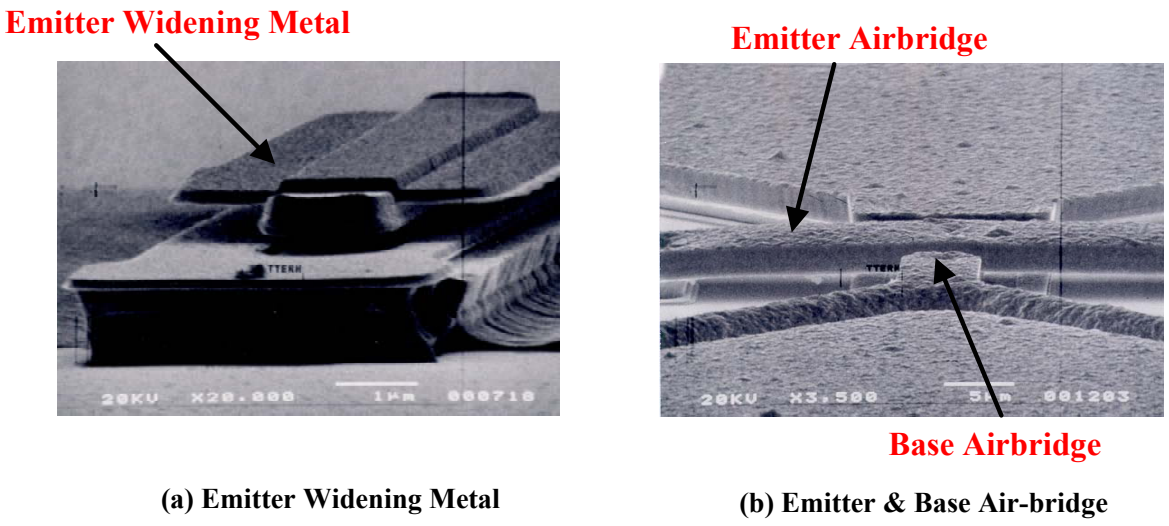


Fig. 10. Special interconnection structure for minimizing the emitter parasitic resistance and inductance.

For the high speed InP HBTs, the emitter and base metal widths are 0.5 μm (effectively 0.25 μm) and 1 μm, respectively. The base resistance (R_B) is minimized by maximizing the base doping (8.0×10^{19} cm^{-3}) and optimizing the base contact resistivity. Additionally, the emitter parasitic resistance and inductance are minimized by using emitter metal widening and an air bridge structure using plated thick gold [see Fig. 10].

IV. Device Measurement Results

1. DC performance

I-V curves of the HBT with 0.25×8 μm^2 emitter area are measured and depicted in Fig. 11. As shown, the common-emitter dc current gain (β) and breakdown voltage of the fabricated HBTs are

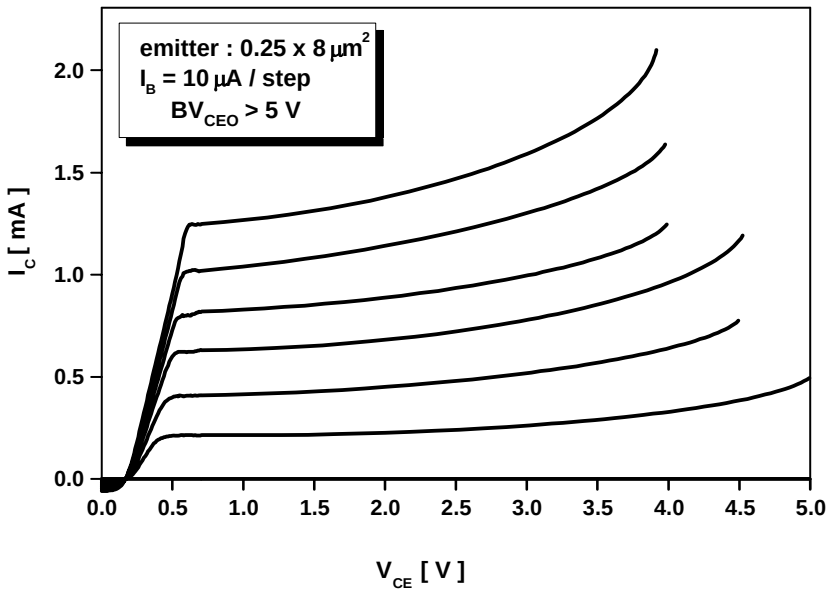


Fig. 11. Common emitter I_C-V_{CE} characteristics of the fabricated HBT with a 0.25×8 μm^2 emitter area

about 23 and above 4 V, respectively at a collector current density of 1×10^5 A/cm^2. The breakdown voltage of the HBTs at an open base, BV_{CEO}, is very high, above 5 V. The base sheet resistance (R_{SB}) of 472 Ω/□ (hole mobility ≅ 41.38cm^2/V·s for 400 Å thick C-doped to 8.0×10^{19} cm^{-3} base) and specific contact resistivity (ρ_{BC}) of 1.65×10^{-7} Ω•cm^2 are measured using transmission line measurement (TLM). The transfer length L_T, expressed as $(\rho_{BC}/R_{SB})^{1/2}$, is 0.19 μm and the base contact resistance is maintained low.

2. Microwave performance

The microwave performances of the HBT are characterized by on-wafer S-parameter measurements for 0.5-40 GHz and 50-75 GHz bands using an Agilent 8510C network analyzer calibrated by thru-reflect-line (TRL) method. To analyze RF performance of fabricated HBT, we have extracted the small signal equivalent models. The junction depletion capacitances and bias independent parasitic capacitances are extracted from "*cold*" S-parameters under reverse and low forward biases. The series resistances are directly determined from "*over-driven*" S-parameter [13]. Also, the values for the transit times are calculated from the measured S-parameters. By plotting f_T vs. $1/I_C$ and fitting a line, the intersection at the y-axis provides the value for $\tau_F = \tau_B + \tau_{SC} + (R_E + R_C)\, C_{CB}$ and the slope information for the emitter charging time τ_E.

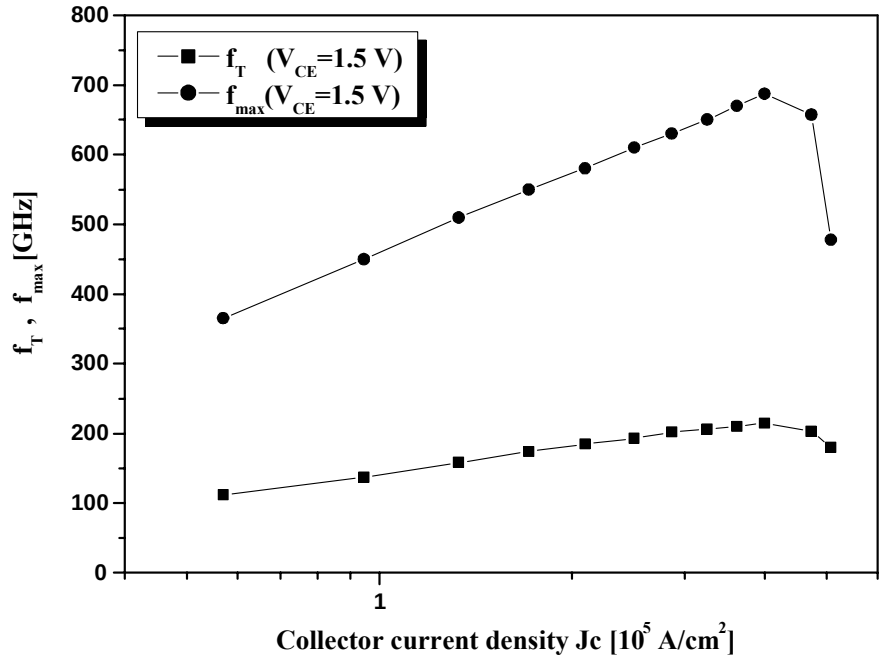


Fig. 12. Dependence f_T and f_{max} on collector current density of the fabricated HBT with a 0.25 × 8 μm^2 emitter area

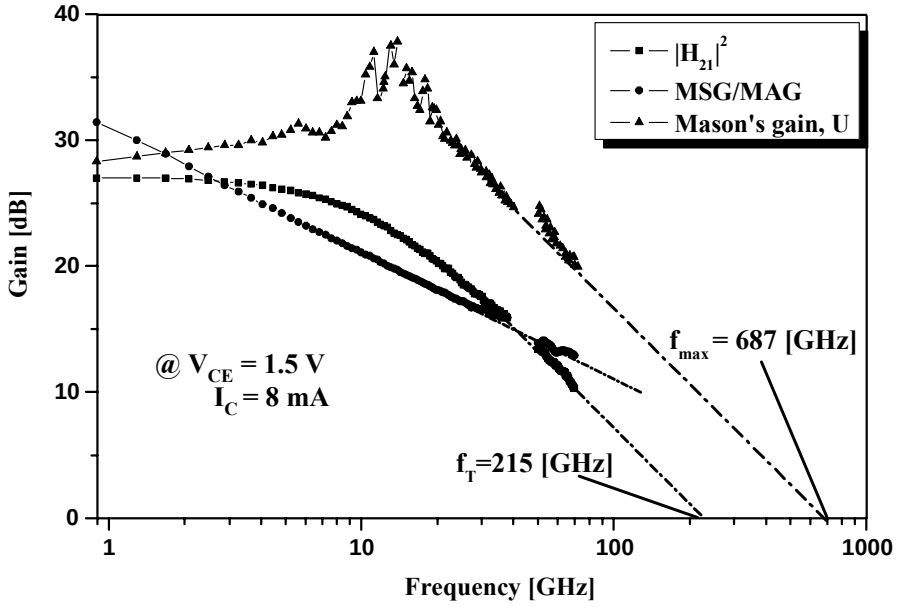


Fig. 13. Frequency dependencies of $|h_{21}|^2$, MSG/MAG, and Mason's gain at I_C = 8 mA and V_{CE} = 1.5 V.

Fig. 12 shows the dependence of f_T and f_{max} on collector current density at 1.5 V collector bias. The frequency dependence of the current gain, Mason's unilateral gain, and maximum stable gain/maximum available gain are shown in Fig. 13. The Mason's unilateral gain curve for pad-deembedding case is smooth and follows the –20 dB/decade frequency dependence very well. The pad-deembedding is inevitable for the characterization of the small size device because the pad parasitic components are not negligible compared with the intrinsic device components. The estimated f_T and f_{max} of the HBT are 215 GHz and 687 GHz, respectively, at I_C = 8 mA and V_{CE} = 1.5 V. This is the highest f_{max} ever reported for a mesa-type HBTs.

In Fig.14, emitter-collector total delay time versus inverse of collector current density is shown. For the transit time reduction, the SHBT employs InGaAlAs emitter setback with graded Al (Aluminum) composition and Indium mole fraction graded base with about 40 meV of potential drop. As the results, an excellent forward transit time (τ_B+τ_{SC}) of 0.63 ps can be achieve, from the 40-nm base/250-nm collector device.

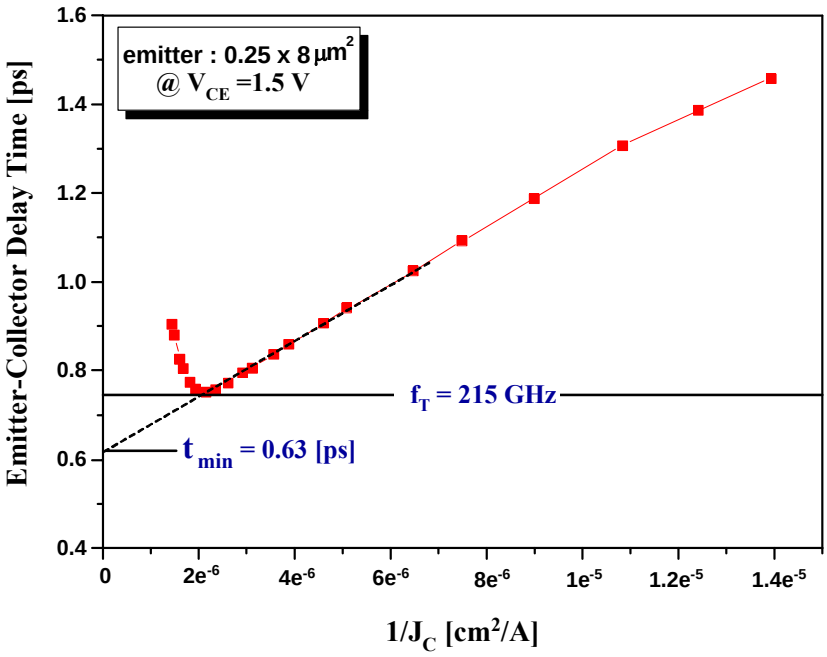


Fig. 14. Small-signal equivalent circuit model (Core Part) at I_C = 8 mA and V_{CE} = 1.5 V

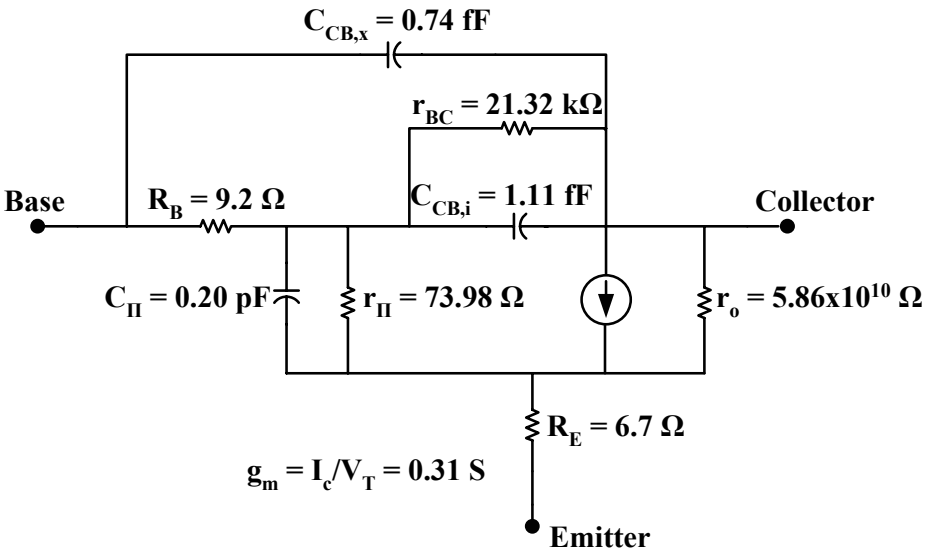


Fig. 15. Small-signal equivalent circuit model (Core Part) at I_C = 8 mA and V_{CE} = 1.5 V

From the measured S-parameters, small-signal model parameters of the device are extracted based on an HBT equivalent hybrid-π model and are shown in Fig. 15. Despite the conventional structure, the time constant $R_B \cdot (C_{CB,i}+C_{CB,x})$ is very low, about 17 fs, due to the base contact optimization, the base-pad isolation and new collector undercut. These improved structure results in a very high-speed SHBT. Fig. 16 compares the f_T and f_{max} of our HBTs with those taken from literature. It can be seen that excellent f_{max} is obtained by using the proposed novel but simple process techniques for parasitic reduction. Only better performance has been reported by UCSB using the transferred substrate process. The process is very complicated and is not manufactured. Recently, UCSB abandons the process.

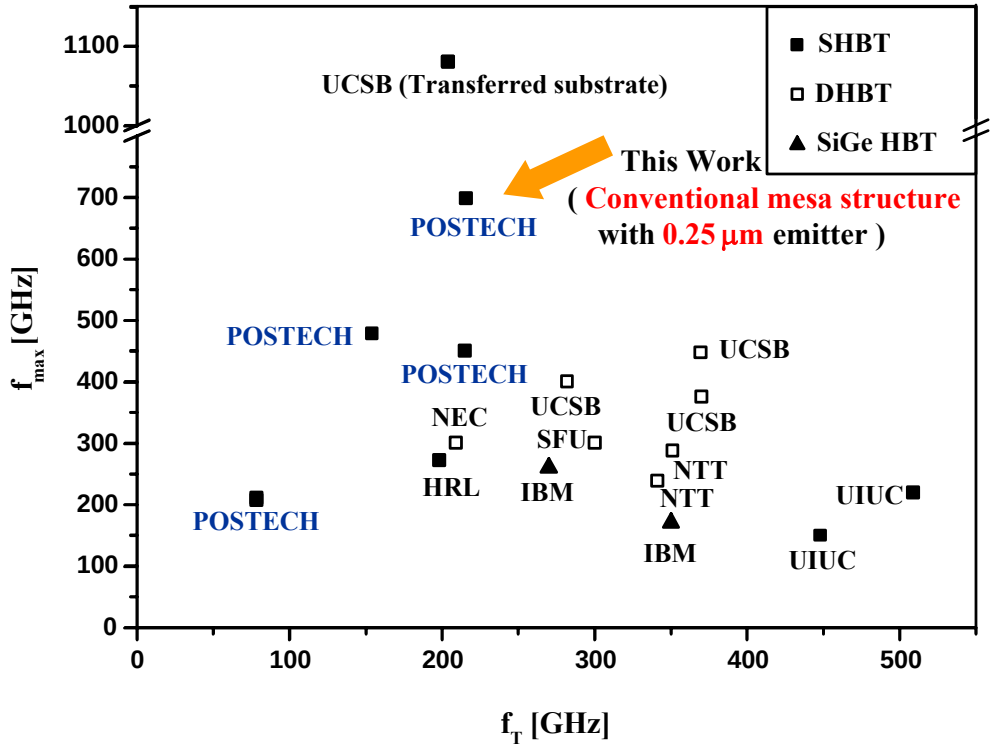


Fig. 16. Overview of f_T and f_{max} data for high Speed HBTs.

V. Scaling of HBT and Challenges for Higher f_T and f_{max}

Fig. 17 shows the scaling trends of the InP/InGaAs SHBT fabricated in Postech. We choose 600 Å base and 6000 Å collector layers as the 1st generation InP/InGaAs SHBT because this structure is designed for high f_{max}. The 1st generation SHBT with 1.0 μm emitter geometry has 80 GHz f_T and 208 GHz f_{max} and the device is laterally and vertically scaled down for improved f_T and f_{max}. As a result, the

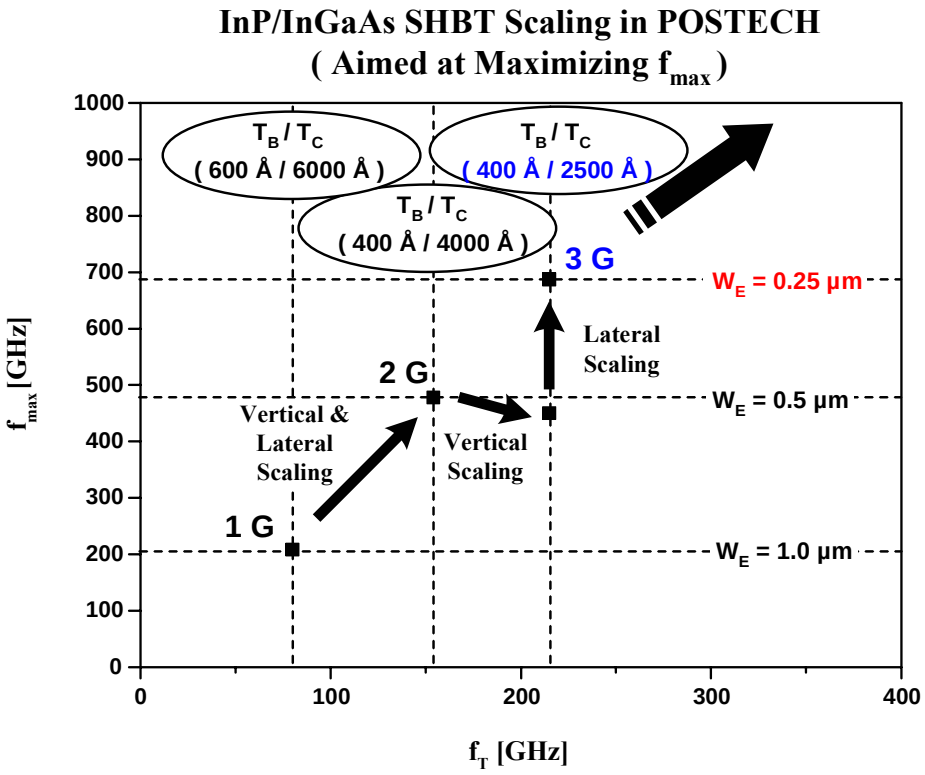


Fig. 17. Scaling trend of InP/InGaAs SHBT fabricated in Postech

high-frequency performance of f_T = 154 GHz and f_{max} = 478 GHz is obtained from the 2nd generation SHBT with 0.5 μm emitter width, 400 Å base and 4000 Å collector thicknesses [14]. Subsequently, the vertical and lateral scaling of device is continued by collector layer thickness reduction from 4000 Å

to 2500 Å and W_E from 0.5 μm to 0.25 μm, respectively. From the 3rd generation HBT, we could demonstrate the maximum extrapolated f_{max} of about 687 GHz with f_T of 215 GHz, above described. This is the highest f_{max} ever reported for a mesa-type HBTs. As the device is vertically and laterally scaled down further, the SHBT will deliver RF performances with $f_{max} \geq 800$ GHz with about f_T of 300 GHz or $f_T \geq 500$ GHz and about f_{max} of 600 GHz. However, f_T is limited by the emitter and collector charging times due to the large R_E. For further improvement, we must find a new process/structure scheme to reduce the R_E and epi-design to increase the Kirk current level (J_K). To reduce $R_{E,cont}$, ρ_{EC} must be improved following the scaling factor of γ^{-2} or the emitter contact area must be maintained large through the emitter regrowth process [15]. As the device is laterally scaled down, the emitter epitaxial resistance ($R_{E,epi}$) is no less important than the $R_{E,cont}$ and the emitter epitaxial resistance ($R_{E,epi}$) must be kept low by the emitter layer thickness scaling.

Conclusions

High-speed InP/InGaAs SHBTs are fabricated by using the Postech process. For the parasitic reduction, the collector layer is undercut using the etch-stop layer, base pad is isolated, and emitter metal is widened using thick plated gold. A high frequency performance of f_T = 215 GHz and f_{max} = 687 GHz is obtained from the HBT with a 0.25 × 8 μm^2 emitter area. This is the highest f_{max} ever reported for a mesa HBTs. As the device is scaled down further, especially vertical scaled down, the device RF performance will be enhanced further. These data clearly indicate that this conventional

process can be a practical technique for implementation of the InP HBT for high-speed electronic circuits.

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