PA30

An Improved Behavioral Large-Signal Modeling of RF LDMOSFET with an Accurate Nonlinear Drift Resistance

Kyungho Lee, Jounghyun Yim, Jehyung Yoon, Bumman Kim, Donghyun Baek*, Soonhag Lee*, and Ilhun Shon*

Dept. of E.E. Eng., Pohang University of Science and Technology,

***System LSI Division, Samsung Electronics Co., Ltd.**

Abstract

An improved behavioral large-signal model of RF LDMOSFET was developed to enhance the accuracy while keep the physical meaningfulness. Nonlinear drift resistance was carefully investigated and extracted directly from DC measurement data using the concept of the common intrinsic drain voltage in the two or more LDMOSs with different LDD lengths. The model was validated in DC and RF characteristics and had good agreements with the measured data.

1. Introduction

The major difficulty for modeling silicon lateral-diffused metal oxide field effect transistors (LDMOSFET's) arises from the nonlinear drift resistance (R_{dn}), that is not adequately characterized in popular MOSFET models [1]. Several papers for LDMOSFET model explain the nonlinear drift resistance, intrinsically [2, 3] or extrinsically [4, 5]. The intrinsic approach means that the channel current includes the LDD effect, regardless of its physical meaning. The extrinsic method uses a JFET or a nonlinear resistor. Among the extrinsic methods, the most popular model treats the LDD effect as a nonlinear drift resistance and is very accurate. Most of them extract the resistance from the device simulation result [1, 4] or the direct probing the intrinsic drain voltage with their special test structures. However, the device simulation results are somewhat unreliable and the direct probing method needs an additional test structure with significant restriction on LDD length.

In this paper, we have proposed a new extraction method of R_{dn}. We use two devices with the same intrinsic MOSFET but different LDD lengths. This method makes possible that the channel output resistance (r_{ds}) and R_{dn} are divided and extracted directly from DC measurement results. Additionally, we could improve our previous model [2] by including a bias dependent intrinsic gate resistance (R_i) and phase delay of transconductance (τ) also.

2. Nonlinear Drift Resistance and Its Extraction

Due to the increase of potential drop across the LDD region with enhanced gate voltage, the intrinsic MOSFET of the LDMOS is forced away from saturation into triode region of operation, causing the sharp transconductance fall-off. The proposed extraction algorithm reuses the above physical interpretation of R_{dn} behavior. From the DC-IV measurements under the forced operation of V_{gs} for two devices with different LDD lengths, we can calculate the difference of the extrinsic drain voltage (V_{ds1} and V_{ds2}) between two devices, while the intrinsic (extrinsic) drain current maintained the same (I_{d2}). Details are depicted in Fig. 3(a). Using this routine, we can easily extract R_{dn} for the whole bias range. Its extraction and fitting results are shown in Fig. 3(b).

3. Overall Modeling Procedure

Fig. 1 shows the equivalent circuit of the improved version of our previous work [2], which includes a nonlinear drift resistance. We have carried out modeling for the LDMOS with a total gate length of 400 um and LDD length of 0.7 um fabricated by 0.25 um technology at Samsung Electronics Co., Ltd. Fig. 2 shows overall modeling procedure used in this work. Details are as follows.

At first, R_{dn} is extracted using the proposed method mentioned in section 2. S-parameters are measured with several bias conditions and de-embedded. The series parasitic elements are determined from "cold" S-parameters with $V_{gs} = V_{ds} = 0$ V. The next step is to fit the intrinsic channel current model, which is performed after de-embedding the extrinsic series resistances including R_{dn}. Substrate network is extracted and fitted under the bias condition with $V_{ds} = 0 \sim 9$ V and $V_{gs} = 0$ V. These results are depicted in Fig. 4.

After the de-embedding of series parasitic elements, substrate network, and nonlinear drift resistance, we obtain the intrinsic part of LDMOS, which is exactly the same as the typical MOSFET model. Nonlinear capacitances, intrinsic gate resistance, and g_m delay are extracted following reference [6] and are fitted. The major results of them are shown in Fig. 5. After the whole extraction and fitting steps, we have constructed the model in Agilent's ADS, using symbolic defined device (SDD).

4. Results and Discussion

Fig. 6 compares the measured and simulated results of the DC characteristics. As shown in the figures, the simulation results are in good agreements with measurement data. From the intrinsic and extrinsic DC-IV, we find that the intrinsic MOSFET of LDMOS operates mostly in the triode region with large nonlinearity. Fig. 7 shows RF gain characteristics under various bias conditions from the measurement and the simulation of the developed model. Again, they fit well in the wide bias range.

5. Summary

A behavioral large-signal model that includes nonlinear drift

resistance has been developed to predict the RF LDMOSFET characteristics accurately while keeping the physical meaningfulness. A simple and accurate extraction methodology of nonlinear drift resistance is proposed for modeling the LDD region. The simulated DC and RF characteristics have good agreements with measured ones.

References

[1] M. N. Marbell, *et al.*, *EUMC*, pp. 225-228, 2004.

[2] Y. Yang, *et al.*, *IEEE T-MTT*, pp. 1629-1633, 2001.

[3] M. Miller, *et al.*, *IEEE MTT-S*, pp. 19-22. 1997.

[4] J. Jang, *et al.*, *IEEE MTT-S*, pp. 967-970, 2001.

[5] N. Hefyene, *et al.*, *SISPAD*, pp. 203-206, 2002.

[6] M. Berroth, *et al.*, *IEEE T-MTT*, pp. 891-895, 1990.

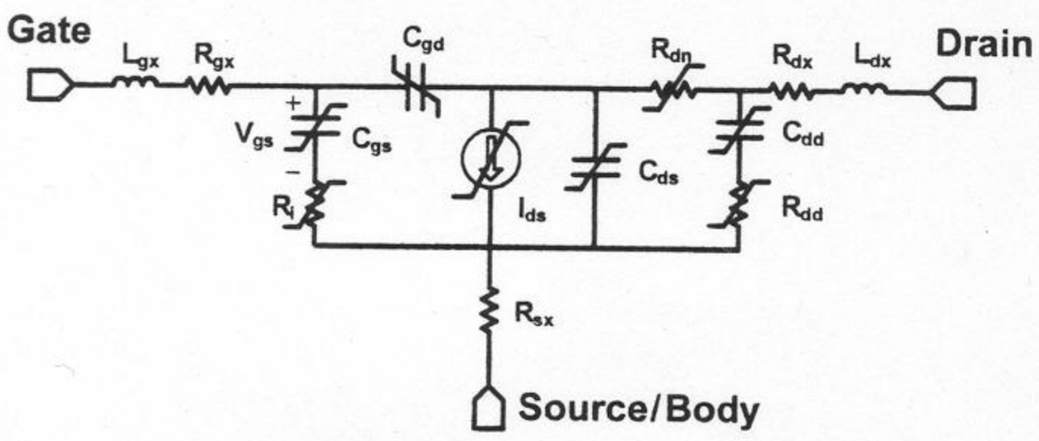
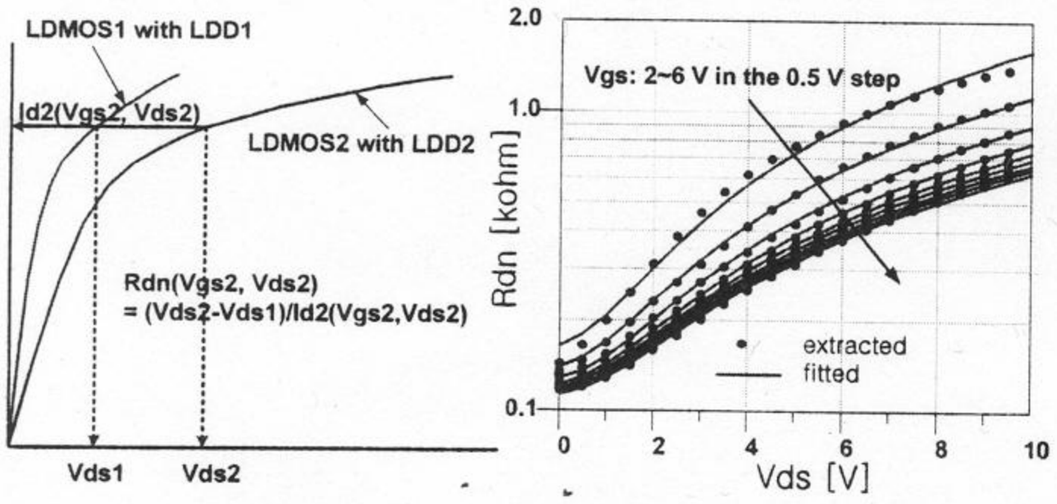
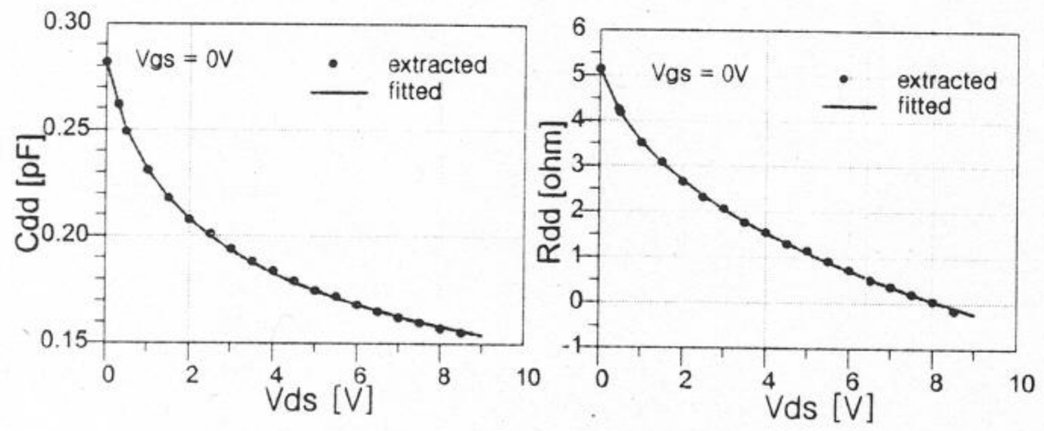


Fig. 1. Large signal equivalent circuit of RF LDMOSFET including the nonlinear drift resistance (R_{dn}).



(a) (b)

Fig. 3. Nonlinear drift resistance (R_{dn}): (a) extraction algorithm, (b) extraction and fitting results.



(a) (b)

Fig. 4. Extraction and fitting results of substrate network elements, (a) Cdd, (b) Rdd.

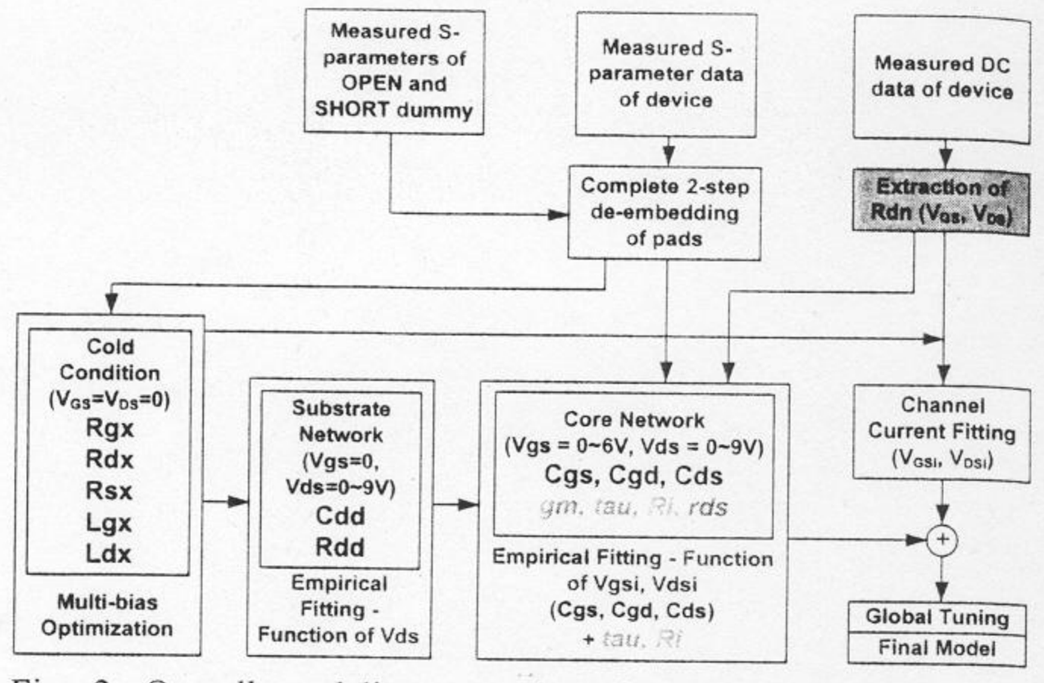
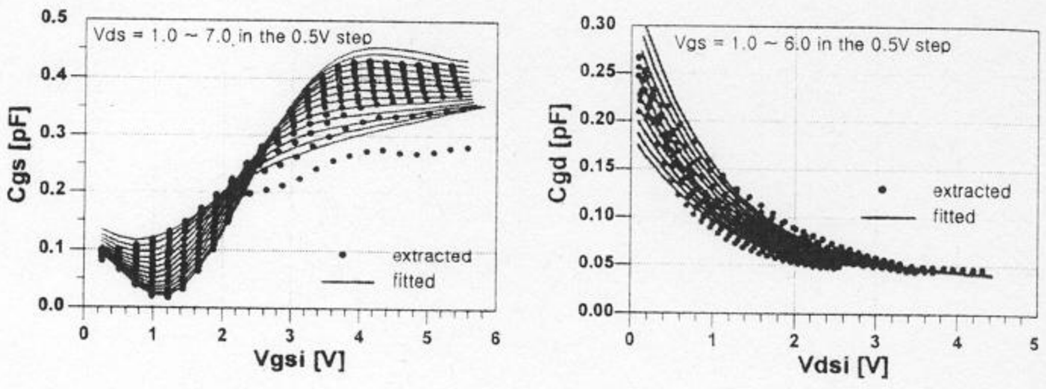
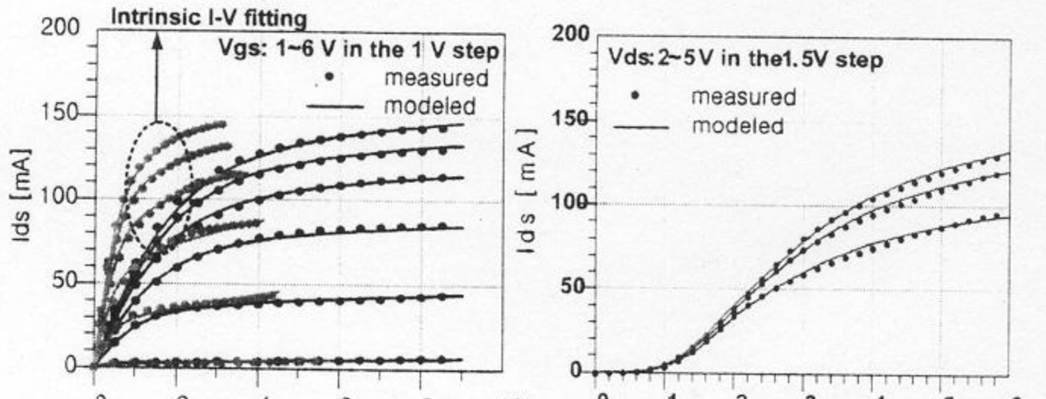


Fig. 2. Overall modeling procedure for RF LDMOSFET with nonlinear drift resistance.



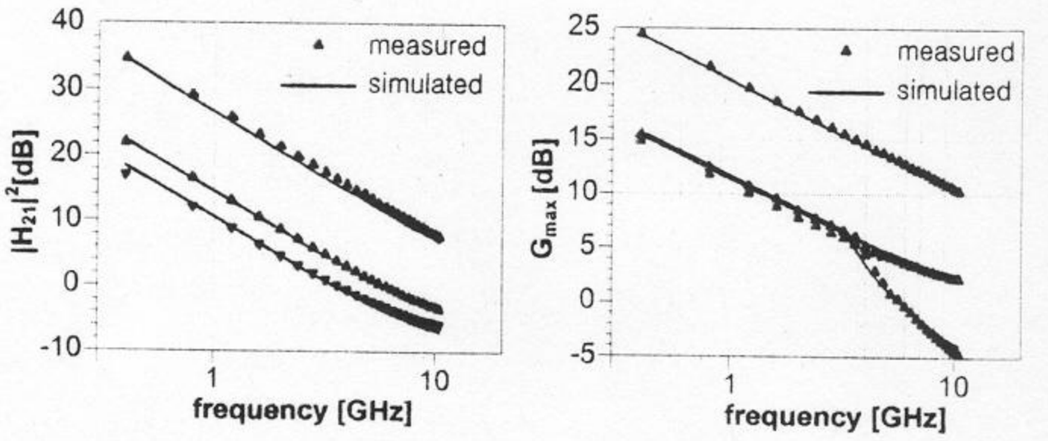
(a) (b)

Fig. 5. Extraction and fitting results of major nonlinear elements, (a) Cgs, (b) Cgd.



(a) (b)

Fig. 6. Measured and simulated results of DC characteristics, (a) I_{DS}-V_{DS}, (b) I_{DS}-V_{GS}.



(a) (b)

Fig. 7. Measured and simulated results of RF gain characteristics, (a) $|H_{21}|^2$, (b) G_{max}(MSG/MAG) in the frequency range of 0.4-10.4 GHz, at (V_{DS},V_{GS}) = (1.0V, 2.5V), (4.0V, 1.5V), and (7.0V, 0.5V).