Development of High Speed InP/InGaAs/InP DHBT with High Breakdown Voltage

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Abstract

InP-based double heterojunction bipolar transistors (DHBTs) for high speed applications are fabricated using SSMBE grown epi. In order to improve f_T and f_{max} simultaneously, we are focused on the vertical scaling and parasitic reduction. Especially, for the low base resistance, a new self-aligned base metallization (SABM) scheme is developed. Maximum f_T of 290 GHz and f_{max} of 296 GHz are achieved for 0.8(effective 0.5) × 6 μm^2 devices at collector current density of 400 kA/cm^2 and collector voltage of 1.5 V. The breakdown voltage is moderately high, BV_{CEO} of 6.2 V. This device technology supports the promising potential of InP/InGaAs/InP DHBTs for high frequency applications.

1. Introduction

Due to the demand for high speed circuits, the operation frequency of transistor is pushed steadily into higher frequencies. Among the device technologies, InP based HBT's deliver superior high speed performances to any other devices. While the InP-based single heterojunction bipolar transistors (SHBT's) have low breakdown voltages due to the narrow bandgap of InGaAs collector layer, the InP-based DHBT's have high speed properties and high breakdown voltage at the same time using InP collector layer.

In this paper, high speed InP/InGaAs/InP DHBT has been developed. For the high f_T, the vertical scaling by thin base and collector is employed and the base layer is compositionally graded. For the high f_{max}, the base resistance is reduced by decreasing the gap resistance and the base-collector capacitance (C_{CB}) is reduced by collector undercut process and base pad isolation because $f_{max} \cong (f_T/8\pi R_B C_{CB})^{1/2}$. Additionally, the emitter metal widening technique is employed to reduce emitter parasitic resistance. With those techniques, the DHBT with f_T of 290 GHz, f_{max} of 296 GHz, and BV_{CEO} of 6.2 V is developed.

2. Device Structure and Fabrication

The base layer is highly doped to 8E19 cm^{-3} to obtain a low base sheet resistance. To achieve a high β and reduced base transit time, the base layer is thin to 250 Å and linearly compositional graded from x = 0.46 to 0.53 toward collector.

To minimize the carrier blocking effect due to the conduction band discontinuity between InGaAs (base) and InP (collector), the linearly compositional graded $In_{(x)}Ga_{(y)}Al_{(1-x-y)}As$ layer, where the In mole fraction is fixed, x = 0.53, and the Ga is linearly controlled from y = 0.47 to 0.20 toward the base, is employed at the collector. Additionally, to compensate the reverse electric field induced by the graded layer, delta-doped InP layer is introduced within collector layers. The whole layer structure is shown in Table 1.

We have fabricated mesa structure DHBT. The emitter and base metal widths are 0.8 μm and 1.0 μm, respectively. The collector undercut process is carried out after base and collector mesa formation using the method suggested in the reference [1]. The comprehensive process sequence can be found in our previous work [2]. Differently with the conventional SABM technique (Fig. 1(a)), we have developed a new SABM technique for further reduced extrinsic base resistance. First, the emitter mesa is formed by the mask of PR definition of emitter. Second, metallization process is followed for both emitter and base contact with Pt/Ti/Pt/Au. This simple but novel technique reduces the emitter to base contact distance (S_{EB}). In this step, the emitter contact resistivity as well as the base are precisely controlled and investigated. As the result of minimized S_{EB}, the extrinsic base resistance is smaller and f_{max} can be improved significantly. The schematic of new emitter mesa formation technique is depicted in Fig. 1(b).

3. Device Measurement Results

The measured common emitter I-V curve of the fabricated DHBT with 0.5 × 6 μm^2 emitter area is depicted in Fig. 2. The common-emitter dc current gain (β) of the DHBTs is about 25. The breakdown voltage of the device at an open base, BV_{CEO}, is 6.2 V. The sheet resistance and specific contact resistivity, measured using transmission line measurement (TLM), are 12 Ω/□ & $1.8 \times 10^{-8}\ \Omega \cdot cm^2$ for emitter, 872 Ω/□ & $1.4 \times 10^{-6}\ \Omega \cdot cm^2$ for base. The transfer length, L_T, expressed as $(\rho_{BC}/R_{SB})^{1/2}$ is 0.4 μm and the base contact resistance is maintained low.

The microwave performance is characterized by on-wafer S-parameter measurements from 0.5 to 40 GHz using a HP8510C vector network analyzer. The frequency dependences of current gain $|H_{21}|^2$, Mason's unilateral gain, and maximum stable gain/maximum available gain (MSG/MAG) are shown in Fig. 3. The f_T and f_{max} are obtained assuming a –20 dB/decade frequency dependence of the current gain and Mason's unilateral gain, respectively. Fig. 4 shows the dependences of f_T and f_{max} on collector current density at V_{CE} = 1.5 V. The f_T and f_{max} of DHBT are 290 GHz and 296 GHz at J_C = 400 kA/cm^2 and V_{CE} = 1.5 V.

4. Conclusions

The high speed InP-based DHBT is developed. High frequency performances of f_T = 290 GHz and f_{max} = 296 GHz are obtained for a 0.5 × 6 μm^2 DHBT with BV_{CEO} = 6.2 V. These excellent performances have been achieved by thin layer design of base/collector, grading scheme for base and collector, reducing C_{CB}, and minimizing base resistance with a new SABM technique. Finally the further improvement of f_{max} is expected by improving base ohmic contact resistivity and lateral scaling in the geometrical layout.

5. References

[1] Y. Jeong, *et. al*, "f_{max} enhancement in InP-based DHBTs using a new lateral reverse-etching technique," *Indium Phosphide and Related Materials (IPRM)*, pp. 22-25, 2003.

[2] D. Yu, *et. al*, "Realization of High-Speed InP SHBTs using Novel but Simple Techniques for Parasitic Reduction," *Indium Phosphide and Related Materials (IPRM)*, pp. 753-756, 2004.

Layer Description	Composition	Conc. [cm^{-3}]	Thickness [Å]
Emitter Cap	In0.53 Ga0.47As In(x)Ga(y)Al(1-x-y)As InP	3E19 3E19 1E19	1000 200 900
Emitter	InP	7E17	700
Space	$In_{0.46}$ $Ga_{0.54}As$	i	20
Base	$In_{(x)}Ga_{(1-x)}As$	8E19	250
Setback Collector Delta Doping Collector	In0.53 Ga0.47As In(x)Ga(y)Al(1-x-y)As InP InP	2E16 2E16 1E18 2E16	200 300 30 1000
Sub Collector	InP In0.53 Ga0.47As InP In0.53 Ga0.47As	1E19 3E19 1E19 3E19	200 3000 100 3000
Substrate	Fe-doped Semi-insulated InP		

Table 1. Epi layer structure of the fabricated DHBT

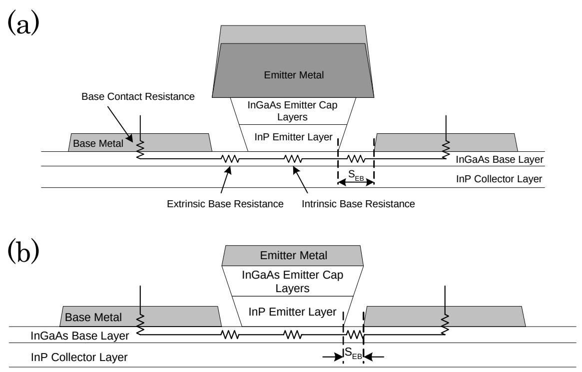

Fig. 1. Emitter mesa formation technique, (a) normal, (b) new.

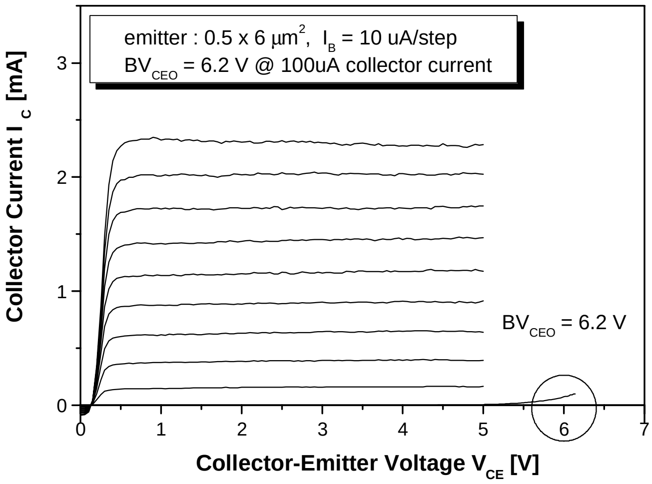

Fig. 2. Common emitter I_C-V_{CE} characteristics of the fabricated DHBT with 0.5 × 6 μm^2 emitter area.

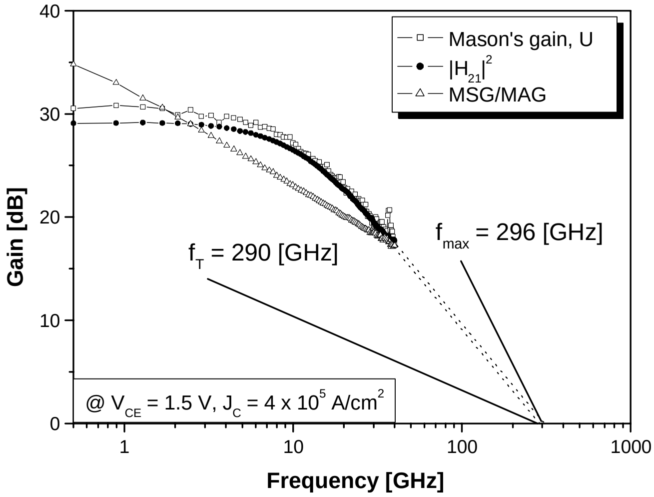

Fig. 3. Frequency dependences of Mason's gain U, $|H_{21}|^2$, and MSG/MAG for the fabricated DHBT with 0.5 × 6 μm^2 emitter area.

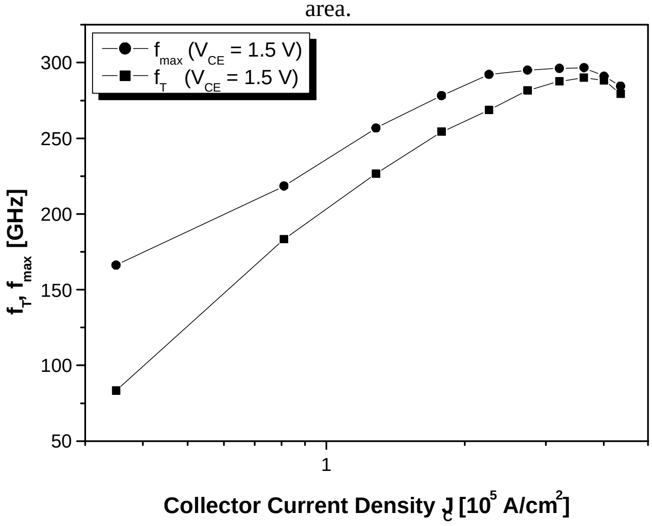

Fig. 4. Dependences of f_T and f_{max} on collector current density for the fabricated DHBT with 0.5 × 6 μm^2 emitter area.