A Modified Cascode Type Low Noise Amplifier Using Dual Common Source Transistors

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Abstract **Low Noise Amplifier (LNA) based on GaAs MESFET has been implemented with a modified cascode configuration using two common source transistors to fulfill a high gain and linearity, low noise figure and low power consumption. The circuit design concept is introduced and also implemented. The measured performances of the LNA at 900 MHz are a gain of 17dB, noise figure of 1.6dB, and IIP3 of 8.5dBm using a supply of 4.7mA and 2.7V.**

I. INTRODUCTION

As the wireless communication system becomes mature and widespread, the requirement of a low noise amplifier (LNA) for the system has become a lot more sophisticated. It needs to minimize the noise figure with a good input matching, and to provide a sufficient gain with high linearity for a wide dynamic range. Besides, dc power consumption should be lowered for portable equipment. Because there are some trade-offs for the design goals [1], it is very difficult to fulfill the multiple-demands. The cascode type LNA, which has a series connection of a common source and common gate stages is widely used for the LNA. Because it is composed of two gain stages with one dc path, it can deliver a high gain with low dc power consumption. Moreover, it is reported that it has a good isolation due to the common gate stage and a fairly good noise figure due to the common source input [2], [3]. But it cannot simultaneously deliver the linearity required by the system.

To fulfill the multiple requirements of LNA, we are proposing a modified cascode type LNA using dual common source transistors. The two transistors have different gate width and bias and the LNA performance can be further optimized using the extra design freedom of the proposed circuit configuration. Section II discusses concept of the proposed design. Section III describes the implemented circuit and measured results.

II. THEORY AND ANALYSIS

A cascode amplifier is a very popular configuration for a LNA. In the design, the common source stage is the most important part for high performances, because the noise figure and IIP3 of the amplifier depend on the stage. The gate width and gate-source voltage of the common source stage transistor are adjusted for good performances. But the optimum design of the gate width and voltage for noise figure and IIP3 are quite different. Moreover, if the dc power consumption and gain are under consideration with them, the problems become a lot more complicated. Therefore, the multiple demands of LNA cannot be achieved by optimizing only the gate width and voltage of the transistor.

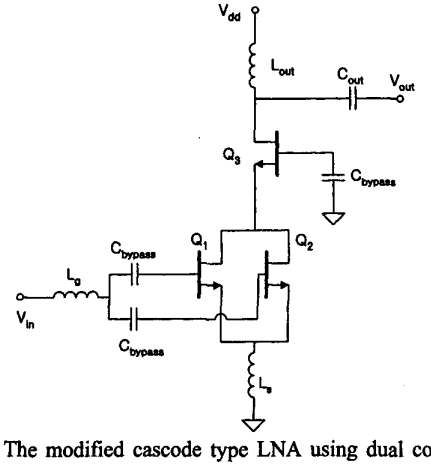

Fig. 1 The modified cascode type LNA using dual common source transistors.

To fulfill the multiple demands, we have modified the cascode amplifier by adding an additional transistor to the common source stage as shown in Fig. 1. The dual common source transistors (Q_1 and Q_2) have different gate-source voltage and gate width for further optimization of design parameters.

Fig. 2 shows a simple equivalent circuit model of the common source stage using two transistors. Z_{cg} is the input impedance of common gate stage and Z_S is the source impedance. Because two transistors are parallel connected on each port, the gate-source capacitances and channel currents are paralleled in the model. Using the

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equations in reference [4], the dc current and noise figure of this circuit are analyzed under the assumption that the feedback terms of drain-gate capacitance and Z_3 are negligible.

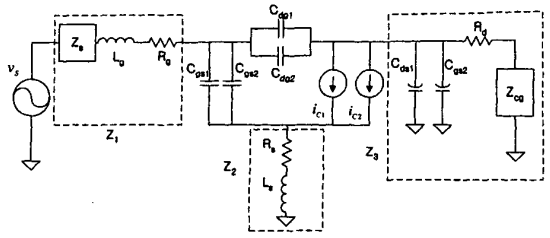

Fig. 2 The equivalent circuit model of the common source stage using two transistors.

$$I_{TOTAL} = I_{D1} + I_{D2} = \beta\left[W_1 (V_{GS1} - V_t)^2 + W_2 (V_{GS2} - V_t)^2\right] \quad (1)$$

$$NF \approx 1 + \frac{R_{ext}}{R_S (W_1 + W_2)} + 2\beta\Gamma R_S \left(\frac{f}{f_{1/f}}\right)^2 \times\left[\frac{W_1}{V_{GS1} - V_t} + \frac{W_2}{V_{GS2} - V_t}\right] \quad (2)$$

where W_1 and W_2 are the gate widths of Q_1 and Q_2, and V_{gs1} and V_{gs2} are the gate source voltages of Q_1 and Q_2., respectively

The transconductance of the common source stage is also formulated following reference [5]. Here, the parasitic resistances are ignored and the input matching condition is a series resonance.

$$G_m = \frac{2\beta\left[W_1 (V_{GS1} - V_t) + W_2 (V_{GS2} - V_t)\right]}{2\omega R_S K (W_1 + W_2)} \quad (3)$$

where g_{m1} and g_{m2} are the transconductances of Q_1 and Q_2, respectively. The linearity of the amplifier is mainly determined by the channel currents of transistors Q_1 and Q_2. Using Taylor series expansion, the nonlinear channel currents are expressed as follows [6].

$$i_{ds}[v_{gs}, v_{ds}] = g_m v_{gs} + g_d v_{ds} + g_{m2} v_{gs}^2 + g_{md} v_{gs} v_{ds} + g_{d2} v_{ds}^2 + g_{m3} v_{gs}^3 + g_{m2d} v_{gs}^2 v_{ds} \cdots \quad (4)$$

Because the nonlinearity of channel current primarily relies on the nonlinearity of V_{gs}, we can simplify the equation for IIP3 only by using the nonlinearity of V_{gs}. Therefore, the previous equations in [7], [8] are modified to the pertinent equations for the dual common source transistors.

$$IIP_3(2\omega_1 - \omega_2) = \frac{1}{6\,\mathrm{Re}[Z_s(\omega)] \cdot |H(\omega)| \cdot |A_1(\omega)|^3 \cdot |\varepsilon(\Delta\omega, 2\omega)|} \quad (5)$$

$$H(\omega) = \frac{1 + j\omega(C_{gs1} + C_{gs2})[Z_1(\omega) + Z_2(\omega)]}{g_{m1} + g_{m2} - j\omega(C_{gs1} + C_{gs2}) + j\omega(C_{gs1} + C_{gs2}) Z_1(\omega) \times[1 + Z_2(\omega)(g_{mj1} + g_{m2} + j\omega(C_{gs1} + C_{gs2}))]} \quad (6)$$

$$A_1(\omega) = \frac{1}{g_{m1} + g_{m2} + g(\omega)} \cdot \frac{1 + j\omega(C_{dg1} + C_{dg2}) Z_3(\omega)}{Z_x(\omega)} \quad (7)$$

$$\varepsilon(\Delta\omega, 2\omega) = g_{m31} + g_{m32} - \frac{2(g_{m21} + g_{m22})^2}{3} \cdot \times\left[\frac{2}{g_{m1} + g_{m2} + g(\Delta\omega)} + \frac{1}{g_{m1} + g_{m2} + g(2\omega)}\right] \quad (8)$$

$$g(\omega) = \frac{1 + j\omega(C_{dg1} + C_{dg2})[Z_1(\omega) + Z_2(\omega)]}{Z_x(\omega) + j\omega(C_{gs1} + C_{gs2})[Z_1(\omega) + Z_x(\omega)]} \quad (9)$$

$$Z_x(\omega) = Z_2(\omega) + j\omega(C_{dg1} + C_{dg2})[Z_1(\omega) Z_2(\omega) + Z_1(\omega) Z_3(\omega) + Z_2(\omega) Z_3(\omega)] \quad (10)$$

where g_{m1} and g_{m2} are the transconductances of Q_1 and Q_2, g_{m21} and g_{m22} are the g_{m2}s of Q_1 and Q_2 and g_{m31} and g_{m32} are the g_{m3}s of Q_1 and Q_2, respectively.

All parameters in equations (5) to (10) are functions of the gate widths and gate-source voltages of the transistors. Therefore, using (1), (2), (3) and (5), we expect that the optimal parameters of W_1, W_2, V_{gs1} and V_{gs2} can be found for the initial design of LNA. As expected, the configuration with dual common source transistors increases the design flexibility. To improve IIP3, the derivative superposition using variation of the phase in g_{m3} as shown in Fig. 3 may be applied [9].

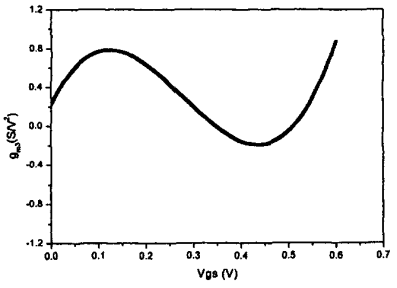

Fig. 3 Simulated gm3 characteristic of GaAs MESFET using TOM(Triquint Own Model)3 model.

III. Implementation and Measurement

Using 0.6um GaAs MESFET foundry of Triquint Semiconductor, we fabricated the LNA at cellular band. The gate widths of Q1 and Q2 are 1100 um and 300 um respectively and that of Q3 is 600 um. The matching elements including a load inductor, are external passive components. The bias circuits are designed using a simple connection of diodes and resistors. A power supply of 2.7V with a total current of 4.7mA is used. Fig. 4 shows the implemented chip with die size of 1.1x 0.5 mm^2 and MLF package of Amkor is used.

Fig. 5 shows the measured S parameters of the LNA. Both the input and output are well matched, satisfying |S11|, |S22| < -10 dB in the band. Fig. 6 is the measured results of gain and noise figure. As shown, the gain of S21 is 17dB, and the noise figure is about 1.6 dB at 900MHz. Figs.7 and 8 show the two-tone spectrum and IM3 vs input power characteristics of the LNA. For the two-tone spectrum, input power is –25dBm and the measured IMD is about 67dBc with IP3 of 8.5 dBm. Fig. 8 shows the fundamental and IM3 power levels for input power from -30 dBm to –20 dBm.

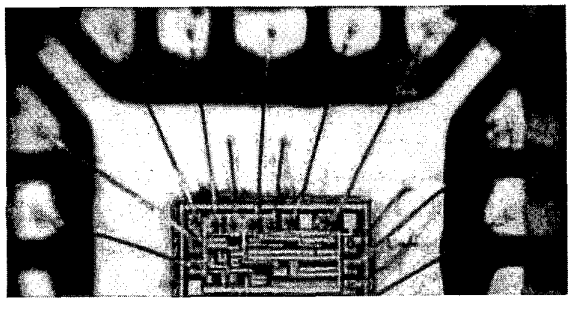

Fig. 4 Die micrograph of the fabricated LNA.

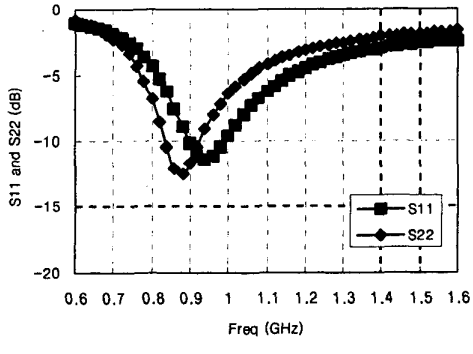

Fig. 5 Measured S parameters of the fabricated LNA.

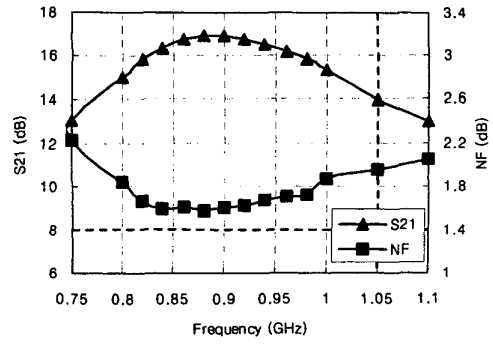

Fig. 6 Measured gain and noise figure of the fabricated LNA.

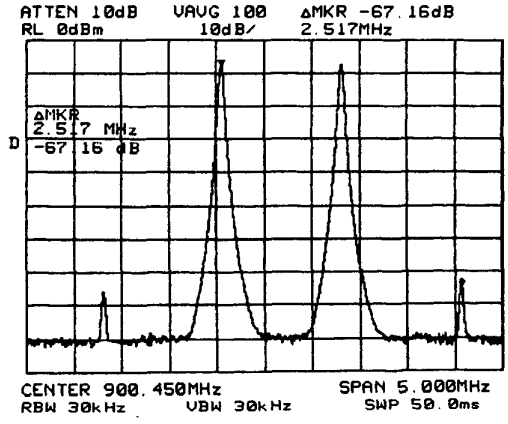

Fig. 7 Measured two-tone spectrum of the fabricated LNA with Pin=-25dBm (IIP3 = 8.5dBm).

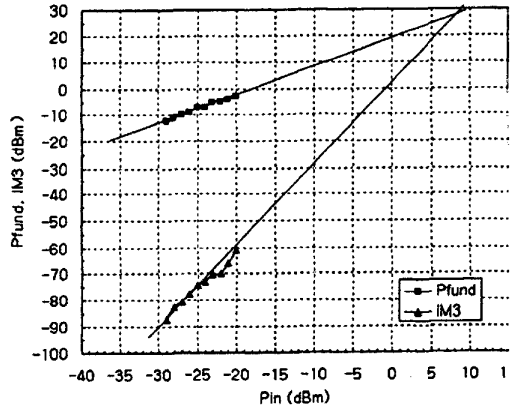

Fig. 8 Measured IMD characteristic of the fabricated LNA. (IIP3 = 8.5 dBm).

TABLE I

COMPARISON OF RECENTLY PUBLISHED CASCODE TYPE LNAS AND THIS WORK

Ref.	Tech.	Freq.	NF(dB)	Gain(dB)	IIP3(dBm)	Power
[3]	30 GHz SiGe Bipolar	1.8 GHz	1.3	17	-2	4.5mA(2.7V)
[10]	0.35 um CMOS	920 MHz	1.0	13	-1.5	8.6mW
[11]	75 GHz SiGe Bipolar	900 MHz	1.2	17	-9	5mA(2.7V)
[12]	0.5 um GaAs MESFET	1.57 GHz	2	17	N/A	N/A
[13]	0.35 um CMOS	900 MHz	1.75	10	3	10mA(2.7V)
[14]	0.8 um CMOS	900 MHz	1.2	14.5	-1	30 mW
This work	0.6um GaAs MESFET	900 MHz	1.6	17	8.5	4.7mA(2.7V)

Table I compares the performance of this fabricated LNA with recently published cascode type LNAs. The Gain, NF and power dissipation are comparable than previously reported cascode type LNAs, and the IIP3 is better than other cascode type LNAs.

IV. CONCLUSION

A cascode amplifier using dual common source transistors is introduced for LNA design. The theoretical background is discussed and the formula of optimum LNA design for the configuration has been given. Since it has more degree of freedoms for the circuit design, we could successfully design an LNA, that satisfies the multiple design requirements, such as noise figure, gain, IM3 level, and power consumption, using the configuration.

The LNA at 900MHz was fabricated using 0.6 um GaAs MESFET technology of Triquint Semiconductor. Die size is 1.1x0.5 mm^2. It has a gain of 17dB with a noise figure of 1.6dB and an IIP3 of 8.5dBm with power supply of 4.7mA and 2.7V.

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