Digital Controlled Adaptive Feedforward Amplifier for IMT-2000 Band

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Abstract— **We present a broad-band adaptive control method for IMT-2000 band multi-carrier power amplifiers adopting feedforward linearization. We have analyzed and implemented an error cancellation detection method employing a frequency hopping pilot and IF synchronous sampling correlator with DSP controller. An adaptive delta-modulated power gradient algorithm is used to adjust the signal and error cancellation loop control parameters. A 2.15 GHz feedforward power amplifier with digital controller is implemented. Band test results show that it covers over a 90 MHz band with more than 50 dBc of IMD at 5 MHz offset frequency for an 8.3 MHz WCDMA signal. The adaptation result shows very fast convergence.**

I. Introduction

For broad band linearization of a feedforward power amplifier, very accurate balances of the amplitude, delay, and phase are required over the frequency band [1]-[11]. In addition to the amplitude and phase matching conditions, an accurate broad-band cancellation detection and a robust adaptive control algorithm for fast convergence are also very important factors. For signal cancellation detection, a general schottky diode power detector can cover a very broad band. But for the error cancellation detection of broad band adaptation, a special detection method is required because a very small error signal (adjacent channel leakage signal) of about 25 - 90 dB below the main signal level must be distinguished.

To detect the cancellation level of the error signal, we propose frequency hopping pilot tone, which hops among the guard bands, where only a small leakage signal exists because the signal channel is not allocated. To detect the pilot signal in the guard band, we present a new correlation detection method adopting IF synchronous sampler, which eliminates the large DC offset effect caused by mixer and op-amps of conventional correlation detectors. It yields good detection accuracy when determining a microvolt range error signal in the presence of millivolt order DC offset [4]. The IF synchronous sampling correlator converts the correlated signal to a proper low frequency (IF), where the DC offset and main signal are easily filtered out.

In the digital adaptive control, the detection quality directly affects on the control performance and the control speed depends mainly on the adaptive control algorithm. A good control algorithm ought to have little overloading for fast conversion, little granularity, noise immunity, adaptivity, and may as well be free from the initial step effect. The general power gradient algorithm, based on the steepest descent method, is commonly employed [5]. Here we present an adaptive delta-modulated power gradient algorithm which improves conversion speed and granularity.

II. Description

1. *Operation of Feedforward Amplifier*

Fig. 1 shows the schematic diagram of a digital controlled adaptive feedforward power amplifier. The RF part of the feedforward amplifier has two cancellation loops: signal cancellation loop (first loop) and error cancellation loop (second loop). In the signal cancellation loop, the subtraction of the input signal component from the coupled output signal of the main amplifier provides the pure error signal. This error signal is amplified by the error amplifier and then cancels the distortion component of the amplifier output by direct subtraction in the error cancellation loop.

The control part has pilot generation and detection circuits, and a DSP controller. In Fig. 1, the detection circuit for the first loop uses a conventional schottky diode power detector, and the output controls the vector modulator by which the main path is adjusted to cancel the input signal component for the error signal path.

2. *IF Synchronous Sampling Correlator*

The block diagram of the IF synchronous sampling correlator is shown in Fig. 2. The guard band hopping pilot signal for error cancellation detection is generated and detected using this circuit.

The operational diagram to analyze the IF synchronous sampling correlator is given in Fig. 3. The main path is modeled as an arbitrary gain of A_1, phase of P_1, and delay of τ_m. IF input signal (V_{IF}) and LO input signal (V_{LO}) are given by

$$V_{IF} = A_i \cdot \cos(\omega_i t + \phi_i) \quad (1)$$

$$V_{LO} = A_o \cdot \cos(\omega_o t + \phi_o) \quad (2)$$

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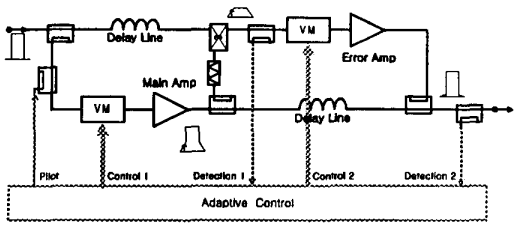

Fig. 1. Block diagram of the adaptive feedforward amplifier

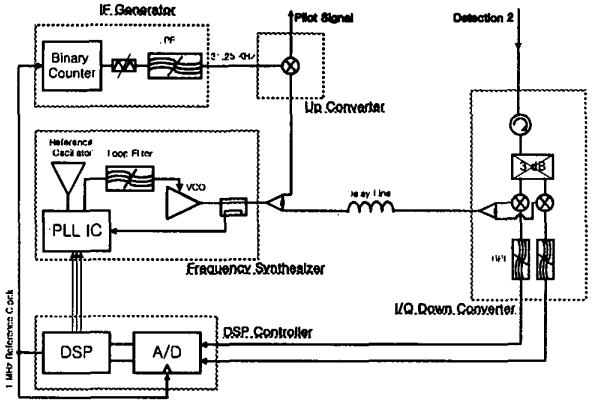

Fig. 2. Block diagram of the second loop detection circuits including the IF synchronous sampling correlator

where A_i and A_o are amplitudes, and ϕ_i and ϕ_o are phases.

After passing through the main path, the I and Q signals are given by

$$V_{p\_dI} = \frac{A_i A_o A_1}{2}[\cos(\omega_R t - \omega_R \tau_m + \phi_R + P_1) + \cos(\omega_L t - \omega_L \tau_m + \phi_L + P_1)] \quad (3)$$

$$V_{p\_dQ} = \frac{A_i A_o A_1}{2}[\cos(\omega_R t - \omega_R \tau_m + \phi_R + P_1 + 90^o) + \cos(\omega_L t - \omega_L \tau_m + \phi_L + P_1 + 90^o)] \quad (4)$$

where $\omega_R = \omega_o + \omega_i$, $\omega_L = \omega_o - \omega_i$, $\phi_R = \phi_o + \phi_i$, and $\phi_L = \phi_o - \phi_i$. We know that the up-converted pilot has two tones with a frequency spacing of $2\omega_i$.

The down-converted and then band pass filtered I and Q signals are represented as

$$V_{I\_down} = BPF\{V_{LO\_d} \cdot V_{p\_dI}\} = \frac{A_i A_o^2 A_1}{4}\cos(\omega_o \tau_m - \omega_o \tau_d - P_1)\cos(\omega_i t - \omega_i \tau_m + \phi_i) \quad (5)$$

$$V_{Q\_down} = BPF\{V_{LO\_d} \cdot V_{p\_dQ}\} = -\frac{A_i A_o^2 A_1}{4}\sin(\omega_o \tau_m - \omega_o \tau_d - P_1)\cos(\omega_i t - \omega_i \tau_m + \phi_i) \quad (6)$$

where $BPF\{\}$ is a band pass filter transfer function and V_{LO_d} is a delayed V_{LO} by τ_d.

After sampling synchronized at ω_i frequency, the final

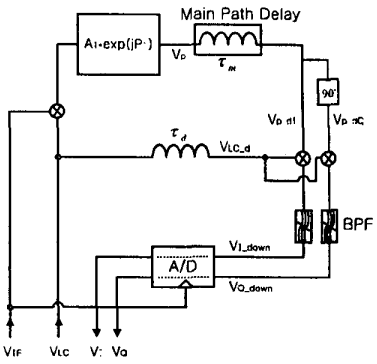

Fig. 3. Operation of the IF synchronous sampling correlator

output voltage of the synchronous sampler is obtained as

$$V_I = \frac{A_i A_o^2 A_1}{4}\cos(\omega_o \tau_m - \omega_o \tau_d - P_1) \quad (7)$$

$$V_Q = -\frac{A_i A_o^2 A_1}{4}\sin(\omega_o \tau_m - \omega_o \tau_d - P_1) \quad (8)$$

Then the error power can be calculated at the DSP as

$$P_{error} = |V_I|^2 + |V_Q|^2 = \frac{A_i^2 A_o^4 A_1^2}{8} \propto A_i^2 \quad (9)$$

Equation (9) shows that the calculated error power is independent of the main path parameters such as, gain (A_1), phase (P_1), and delays (τ_m and τ_d). The uncorrelated signals, such as thermal noise, main signal leakage, and adjacent channel leakage signal, can be sufficiently suppressed by averaging the signal for a suitable number of periods.

3. *Adaptive Control Algorithm*

The DSP controller receives two detected signals and controls two vector modulators. One vector modulator is controlled for signal cancellation and the other is for error cancellation. For both cases, we use an adaptive delta-modulated power gradient algorithm to find the minimum power point. It is expressed as

$$A[n+1] = A[n] + \delta[n] \cdot b[n] \quad (10)$$

where n indicates the control steps, $A[n]$ is the vector modulator control voltage, $\delta[n]$ is the adaptive step size, and $b[n]$ is the delta-modulated gradient coefficient. $b[n]$ and $\delta[n]$ are given as

$$b[n] = \begin{cases} 1 & \text{if, } P[n] \le P[n-1] \\ -1 & \text{if, } P[n] > P[n-1] \end{cases} \quad (11)$$

$$\delta[n] = \delta[n-1] \cdot M[n-1] \cdot b[n-1] \quad (12)$$

where $P[n]$ is the measured error power at the vector modulator control voltage of $A[n]$, and $M[n-1]$ is step size control coefficient. In this experiment, $M[n-1]$ is defined as

$$M[n-1] = \begin{cases} 2 & \text{if, } b[n-1] = b[n-2] = 1 \\ \frac{1}{2} & \text{if, } b[n-1] = -1 \\ 1 & \text{otherwise} \end{cases} \quad (13)$$

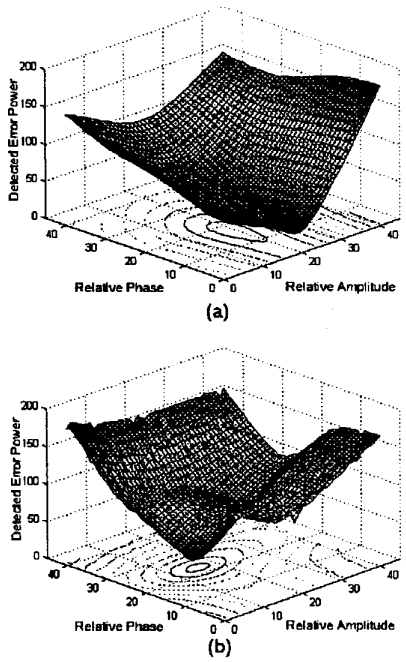

Fig. 4. Transfer characteristics of the loops: (a) first loop and (b) second loop

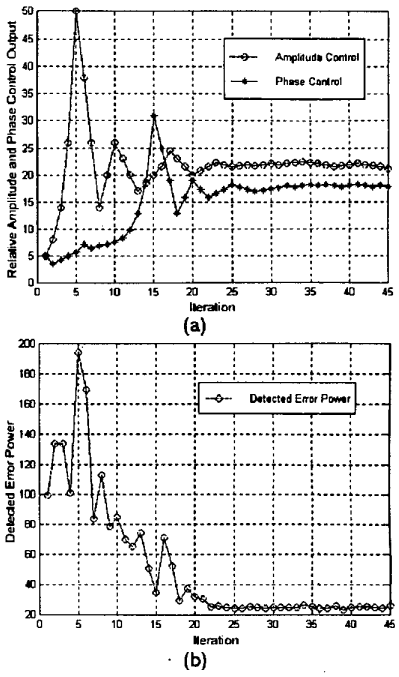

Fig. 5. Measured results of second loop adaptive control: (a) relative control voltages of the vector modulator versus iteration and (b) detected control error power versus iteration

Equation (13) means that if two continuous steps reduce the error power, the next step size is doubled. If the detected error power increases, the next step size is halved. Error power reduction occurs in just one previous step, the step size is maintained. This controlled stepping allows a very fast convergence without overloading. The repeated increase and decrease of error power causes the step size to converge to near zero, which generates less granularity. These are very important stepping characteristics near the optimum point. This method can give more freedom to determine the initial step size of $\delta[0]$.

III. Implementation

A 2.15 GHz centered main amplifier was built by balancing Ericson's PTB20147 BJT with simple open stub matching networks as a final stage. PTB20147 was also used as a single-ended drive stage. An additional two stage gain block drives the main amplifier. The whole main amplifier module shows a 52 dB gain and 39 dBm of P_{1dB} output characteristics. The gain flatness of the main amplifier is ± 0.1 dB within a 90 MHz operation bandwidth. It is driven to an average output power of 27 dBm for the WCDMA signal. At this drive level, the main amplifier has 28 dBc IMD at 5 MHz offset with respect to the WCDMA signal. The error amplifier was fabricated by using a single-ended PTB20147 BJT as a final stage along with additional three gain stages. The error amplifier shows a 56 dB gain and 36 dBm of P_{1dB} output characteristics. The vector modulator was made by the series connection of a reflection type attenuator and a phase shifter using a 3dB hybrid coupler, PIN diode, and varactor diode.

We have fully implemented the IF synchronous sampling correlator shown in Fig. 2. The IF generator has a binary counter for frequency dividing, and a voltage divider and low pass filter for waveform shaping. DSP controller gives a 1 MHz reference clock which is divided to 31.25 KHz by a binary counter. The 1 MHz reference clock also synchronizes the A/D converter. Then the A/D converter samples with a 1 MHz sampling frequency, that is, 32 time samples per 1 period of 31.25 KHz down-converted IF pilot signal.

IV. Results

Control transfer characteristics, which describe the detection performance, are measured. Fig. 4(a) and (b) show the first loop and second loop control transfer characteristics, respectively. The DSP controller sweeps its control outputs, which are relative phase and amplitude within the control ranges. The DSP measures the detected output through the A/D converter. The control transfer surface plots show no local minimum points, meaning that the general gradient algorithm can work.

Fig. 5 is the measured results of the 2nd loop adaptation control. From the outer side of the control transfer surface, the control voltage converges to near the optimum point within 20 iterations, which is shown in Fig. 5(a). Fig. 5(b) is the measured error power versus iteration. The single iteration of the first loop takes about 0.2 ms and the single iteration of the second loop takes about 32 ms to obtain the gradients of both amplitude and phase adap-

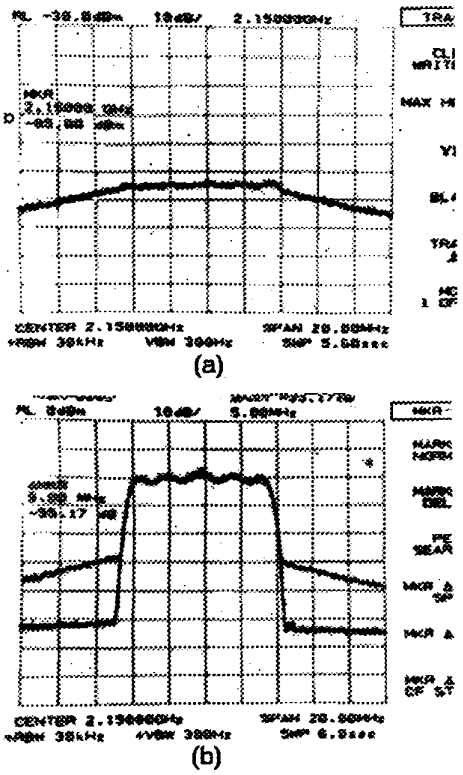

Fig. 6. WCDMA test results with chip rate of 8.192 Mcps and average output power of 27 dBm: (a) signal cancellation and (b) error cancellation

tations. At the 20th iteration, the measured error power of about 30 indicates about 53-55 dBc of IMD level. The adaptive delta-modulated power gradient algorithm shows a fast conversion speed and noise immunity.

Fig. 6 shows the measured results of the WCDMA signal with a chip rate of 8.192 Mcps and average output power of 27 dBm at a carrier frequency of 2.15 GHz. Fig. 6(a) is the signal cancellation result and Fig. 6(b) is the error cancellation result after adaptation. The signal is suppressed by about 30 dB near to the error level and error cancellation is more than 25 dB in this figure. Fig. 7 is the measured IMD at the frequency offset of 5 MHz while sweeping the carrier's center frequency of the WCDMA signal. It maintains an IMD level of 50 dBc for more than 90 MHz bandwidth.

V. Conclusion

In broad-band linearization with the feedforward method, broad-band detection and a fast adaptation algorithm in addition to accurate amplitude, phase, and delay matching are very important. In this paper, we have presented a broad-band detection method utilizing a guard band hopping pilot and its detection with an IF synchronous sampling correlator. The guard band hopping pilot allows a very high detection dynamic range and broad bandwidth. Its detection method, which is an IF

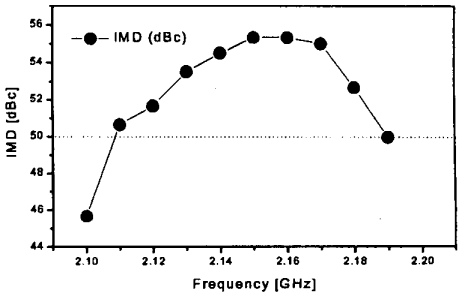

Fig. 7. Measured results of the band characteristics with WCDMA signal at 5 MHz offset

synchronous sampling correlation technique, can avoid the large main signal effect and DC offset problem perfectly.

An improved control algorithm has also been proposed for fast adaptation. The adaptive delta-modulated power gradient algorithm is employed to optimize both signal cancellation and error cancellation. Adaptive control results of the second loop show very fast convergence and little granularity.

The total system, including the RF part and control part, has been designed and implemented. The WCDMA signal test has been performed and test results show more than 50 dBc of IMD at 5 MHz offset over a 90 MHz band.

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