

Efficiency Enhancement of Linear Power Amplifier Using Load Modulation Technique

Bumman Kim, Youngoo Yang, Jaehyok Yi, Joongjin Nam, Young Yun Woo,
and Jeong Hyeon Cha

Department of Electronic and Electrical Engineering and Microwave
Application Research Center, POSTECH, Korea

Abstract — Efficiency enhancement of linear power amplifiers of CDMA base station using Doherty amplifier concept is proposed. The new design concept for the load modulation matching and its experimental optimization procedure are introduced. The matching circuit consists of different offset transmission lines in the carrier and peaking amplifiers for power match across broad power levels. For experimental validation, an average 30-W 2.14-GHz load modulation amplifier has been implemented using a high power silicon LDMOSFET. The load modulation amplifier (a combination of a carrier amplifier biased to class AB mode and a peaking amplifier biased to class C mode) has been compared with a conventional class AB operation by applying 9 channel forward-link broad-band CDMA signal. The results show a superior performance of the load modulation amplifier for both efficiency and linearity.

I. INTRODUCTION

Linear power amplifier for base station, especially adopting feed-forward technique, generally suffers from the excessive heating problem due to its poor efficiency. Also, as the power level of the amplifier increases, the size and cost are directly related to the efficiency. Therefore, high efficiency is a very important characteristic for the amplifier.

The microwave Doherty amplifier was first proposed to improve efficiency using the load modulation of a carrier amplifier through a peaking amplifier attached to a

quarter-wave impedance transformer [1], [2]. Because of the quarter-wave line and input splitter circuits, MMIC implementations of the Doherty amplifier have been limited to a very high frequency (over a few tens of GHz) [3]-[5]. However, it can deliver a higher efficiency without losing linearity or even with improved linearity. Therefore, MIC type Doherty amplifier may be suitable choice for the linear power amplifier for base station application at a few GHz. But, due to reactive components, package parasitics, and internal pre-matching circuits of the high power devices at microwave band, the load matching including imaginary part of the Doherty amplifier has been reported to be very difficult [2],[6].

In this paper, we report on the design concept of Doherty amplifier based on the new load matching technique to match the load impedances at both high and low power levels by inserting different offset lines in the carrier and peaking amplifiers. A MIC type amplifier adopting the improved match for the load modulation is implemented and the experimental results are described.

II. OPERATION AND DESIGN

Fundamental operation principle and efficiency enhancement mechanism of the Doherty amplifier has been well described in previous papers [1]-[6].

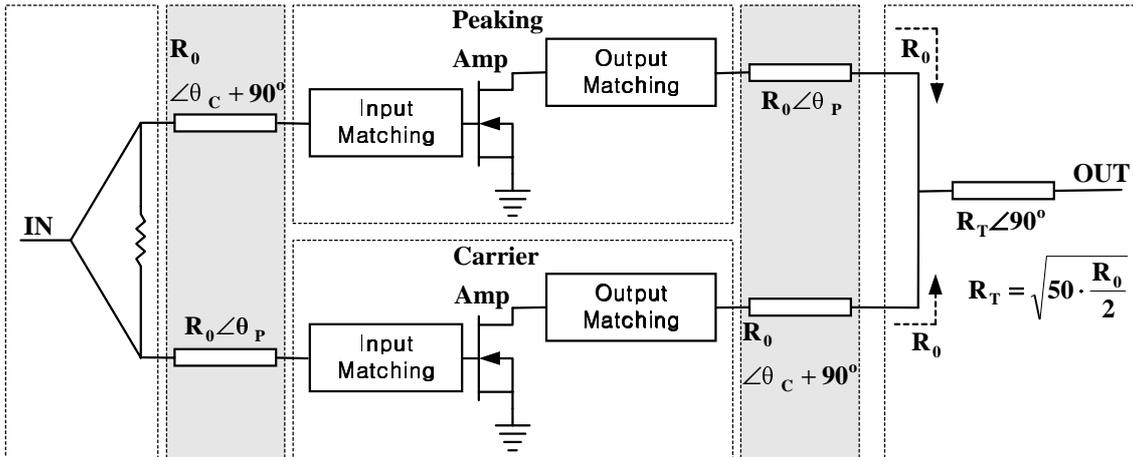


Fig. 1. Schematic diagram of the load modulation amplifier with offset transmission lines in the load matching circuits of the carrier and peaking amplifiers

Fig.1 shows the schematic diagram of our improved load modulation amplifier. It has the ability to match the loads of the carrier and peaking amplifiers across a broad power level. The input and output matching circuits are the optimized design for class AB power operation. The offset lines in the output are designed for the load match at a low power level. The offset lines in the input circuits are just to compensate the phase mismatch between two paths.

For the linear operation of class AB amplifier, the load impedance should be high at a low power level to compensate the low gain at near pinch-off region operation and is reduced at a higher power level as the gain expansion starts. That can be done for the carrier amplifier by less current pulling from the peaking amplifier at a low power level and more current pulling at a high power level. For the purpose, a class C mode peaking amplifier is employed. At a very high power level, the late gain expansion of the peaking amplifier can compensate the gain saturation of the carrier amplifier. Hence, the load modulation technique has a capability to deliver a linear output power with reduced AM-AM compression. But the relation and trade-off between the efficiency and linearity of the load modulation amplifier have not been clearly studied yet.

Fig. 2 shows circuit diagrams to

determine the offset phases of the carrier and peaking amplifiers. The load impedance of the carrier amplifier can be calculated in the cases for both a R_0 load termination, which is the case without load modulation at a high power level, and a $2R_0$ load termination, which is the case with load modulation at a low power level (see Fig. 2(a)). The load impedance for R_0 is fixed to $1.059 - j \cdot 1.782$ for power matching condition and the load impedances for $2R_0$ make circle around Z_{L,R_0} with varying offset angles from 0° to 180° , which is visualized in the lower part of Fig. 3. We have to experimentally optimize the optimum offset angle to have optimum efficiency and linearity. Optimized offset angle ($\theta_c + 90^\circ$) for the carrier amplifier is 157.56° . The matching for the peaking amplifier can be designed in a similar way. The measured small signal output impedance $Z_{O,P}$ of the peaking amplifier including input/output matching circuits varies due to the offset transmission line (see Fig. 2(b)). The optimum offset angle can be calculated for the output impedance $Z_{O,P}$ to have a high resistive value (362.05Ω at 247.56°), which is visualized in the upper part of Fig. 3.

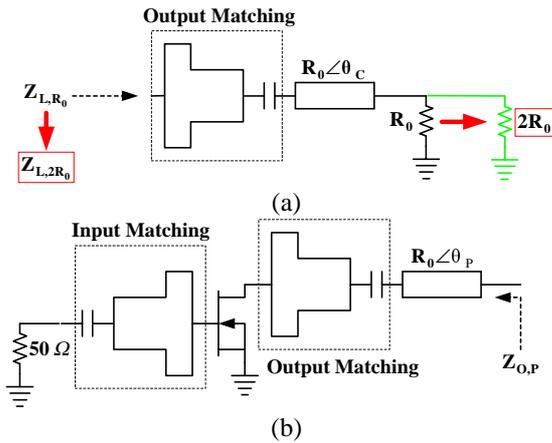


Fig. 2. Circuits to determine the length of the offset transmission lines: (a) for the carrier amplifier and (b) for the peaking amplifier

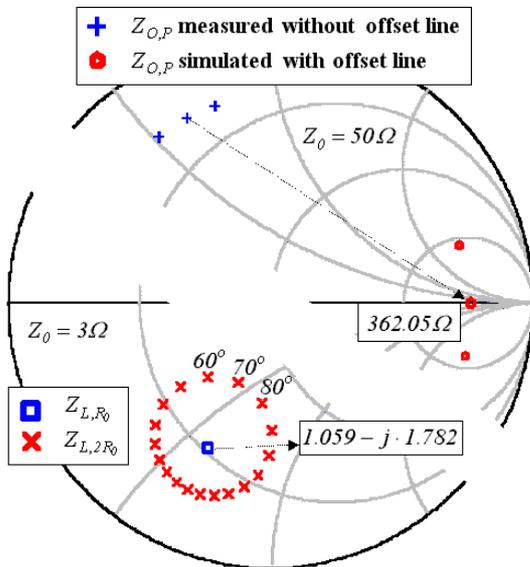


Fig. 3. Lower – Simulated load impedances of the carrier amplifier for an offset angle 0° to 180° at a 2.14-GHz. Upper – Measured and simulated output impedances of the peaking amplifier at 2.11, 2.14, and 2.17-GHz. with 247.56 offset line

III. EXPERIMENTS AND RESULTS

Fig. 4 shows the circuit diagram including drive amplifiers and photograph of the implemented 2.14-GHz 30-W load modulation amplifier. The same devices (Motorola's MRF21125, 125-W PEP silicon LD MOSFET) are used for both carrier and peaking amplifiers. The input and output of the amplifier are matched to 50Ω to have a load impedance (Z_L) of

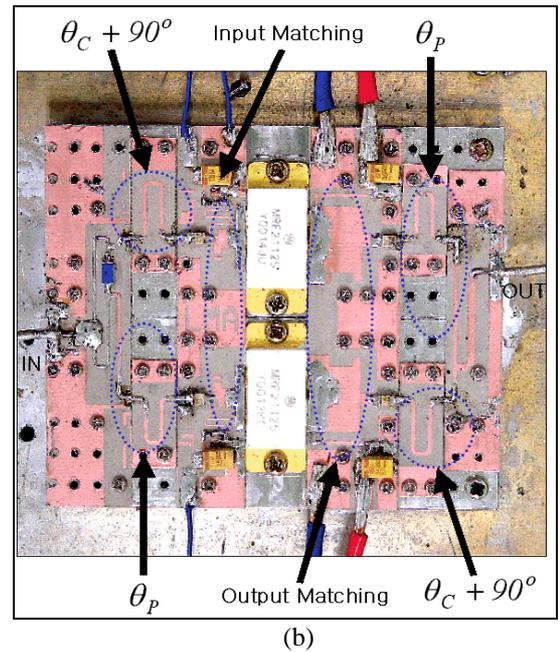
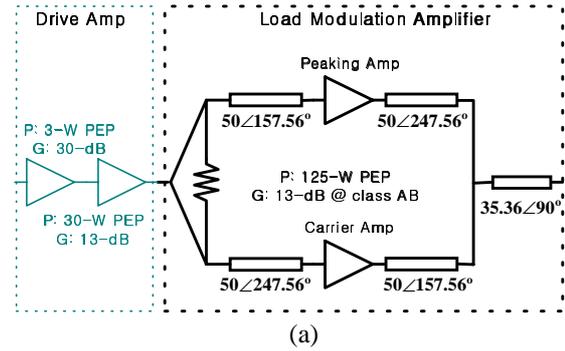
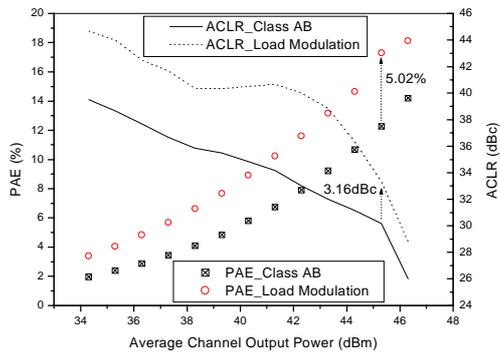
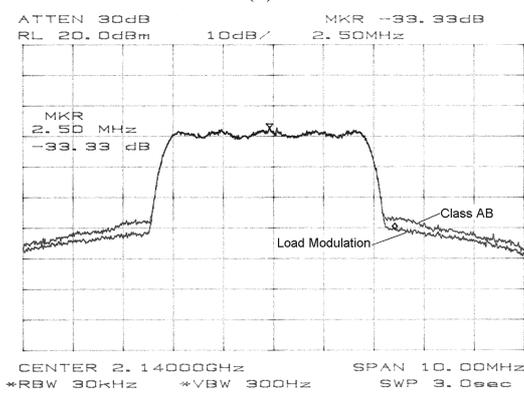


Fig. 4. Implemented 2.14-GHz 30-W load modulation amplifier: (a) circuit diagram and (b) photograph

$1.059 - j \cdot 1.782$. Input signal is split by Wilkinson divider and 50Ω lines are inserted at the input stage of the carrier and peaking amplifiers to compensate phase mismatch between the two paths due to load offset transmission lines (θ_P , θ_C). The experimental optimization of the offset lines and bias points to have optimum efficiency and linearity has been performed. The carrier amplifier is biased at class AB point ($V_{gs}=3.75$ -V and $I_{dsq}=1$ -A) and the peaking amplifier is biased at class C point ($V_{gs}=3.0$ -V and $I_{dsq}=0$ -A). It is compared with a conventional class AB operation ($V_{gs}=3.75$ -V and $I_{dsq}=1$ -A both).



(a)



(b)

Fig. 5. Measured results of the load modulation amplifier compared with conventional class AB operation: (a) PAE and ACLR, and (b) PSD plot

The efficiencies and linearities using 9 channel forward-link broad-band CDMA signal with a high peak-to-average ratio(11-dB) and a high data rates(4.096-Mcps) are compared with those of the conventional class AB mode operation. Fig. 5(a) shows the overall PAE and ACLR at 2.5-MHz offset point vs output power level. At an output power of 45.3dBm (33.9-W), we have a 5.02-% improvement of PAE and a 3.16-dB improvement of ACLR. Fig. 5(b) shows power spectral densities of the load modulation amplifier and class AB amplifier at 45.3-dBm.

IV. CONCLUSIONS

We presented a method to achieve high efficiency with an improved linearity using load modulation technique. A new matching technique using offset lines at the

loads of the carrier and peaking amplifier has been described. The results of measurement show the improvement of efficiency and linearity of the load modulation amplifier compared to the class AB mode operation. This technique will be suited to enhance an efficiency for the linear power amplifier of the base station because it requires very simple RF matching technique and bias adjustment.

ACKNOWLEDGEMENT

This work has been supported by the Agency of Defense Development and BK21 project of the ministry of education in Korea.

REFERENCES

- [1] W.H. Doherty, "A New High Efficiency Power Amplifier for Modulated Waves," *Proc. IRE*, Vol. 24, No. 9, pp. 1163-1182, 1936.
- [2] D.M. Upton, "A New Circuit Topology to Realize High Efficiency, High Linearity, and High Power Microwave Amplifiers," *RAWCON'98, Proceedings*, pp. 317-320, 1998.
- [3] C.P. McCarroll, et al, "A 20GHz Doherty Power Amplifier MMIC with High Efficiency and Low Distortion Designed for Broad Band Digital Communication Systems," *IEEE MTT-S Int. Microwave Sympo. Dig.*, pp. -, 2000.
- [4] K.W. Kobayashi, et al, "An 18-21GHz InP DHBT Linear Microwave Doherty Amplifier," *IEEE RFIC Sympo. Dig.*, pp. 179-182, 2000.
- [5] C.P. Campbell, "A Fully Integrated Ku-Band Doherty Amplifier MMIC," *IEEE Microwave and Guided Wave Letters*, Vol. 9, No. 3, 1999.
- [6] P.B. Kenington, "High-Linearity RF Amplifier Design," Artech House Inc., 2000.