Dual mode Low Noise Amplifier for WCDMA applications

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Abstract - *A monolithic dual mode LNA for WCDMA applications is fabricated by standard 0.35um, Bi-CMOS technology of ST Microelectronics. A modified bias circuit is applied to improve the linearity. The output matching components and load inductor of the LNA are integrated on chip. The measured performances of the LNA are 12.5dB Gain, 1.96dB Noise figure and 1dBm input IP3 with a total current consumption of 7.5mA for a 2.7V supply at high gain mode, -12dB Gain, 12.5dB Noise figure, 20dBm input IP3 and 2.2mA current consumption at low gain mode. The size of the LNA is 400um*450um.*

Keywords: low noise amplifier, dual mode, linearity, pre-distortion, low gain mode.

1 Introduction

A low noise amplifier (LNA) is a key component of RF front-end parts, together with mixer and voltage controlled oscillator (VCO). Particularly, a LNA determines the minimum detectable signal level of a receiver because it amplifies an input signal at the first stage of a receiver. In CDMA systems, the leakage signal from a transmitter appears at the receiver through the duplexer and the leakage power is higher than that of the input signal at the receiver [1]. Therefore, the LNA should have high linearity, covering the power.

The high leakage signal in the receiver can be saturated at the back of the high gain mode LNA, generating many non-linear components. Hence, the LNA should operate as a low gain mode at the power level in order to keep the dynamic range of the receiver. In section 2.2, the LNA for WCDMA applications achieves -12dB attenuation by low gain mode operation.

There are many methods to improve linearity of the LNA, for example, harmonic tuning method using a low frequency trap [2], third order G_m cancellation method using transistors with different G_m's [3], [4] and pre-distortion method [5]. As a pre-distorter, LNA using bias circuit is popularly used due to its good linearity without employing any extra circuits [6]. The bias circuit is composed of resistors and inductor, which will be described in section 2.1.

2 Circuit Description

2.1 Bias circuit

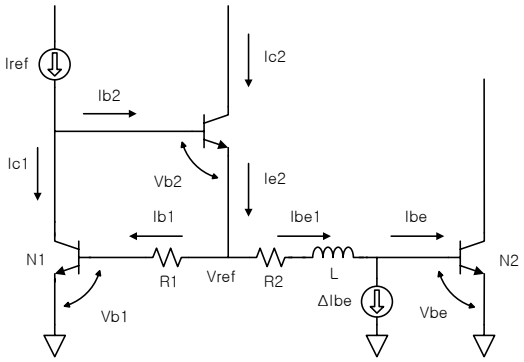


Figure 1. Bias circuit with resistors and inductors

As shown in figure 1, the bias circuit with resistors and inductor is used as a pre-distortion circuit in this work. The inductor improves NF and linearity due to the removal of low frequency harmonic components, and the resistors make the bias circuit immune to process variation and improve stability [7]. Therefore, the bias circuit with both resistors and inductor maximizes the merit above two cases.

To simplify the analysis, it is assumed that all transistors in the bias circuits have same the forward current gain β and saturation current of I_S. In order to divide correctly the current of the mirror circuit, the resistors ought to satisfy $R_1N_2 = R_2N_1$, and the relation of the currents satisfies $I_{be}N_1 = N_2I_{b1}$. In the case, V_{be} is given by

$$V_{be} = V_T \ln\left[\frac{\beta(\beta+1)I_{ref}}{I_S\left\{\beta(\beta+1)+1+\frac{N_2}{N_1}+\frac{\Delta I_{be}}{I_{b1}}\right\}}\right] - \Delta I_{be}R_2 \qquad (1)$$

Applying taylor series in the equation (1),

$$V_{be} = V_T \ln\frac{\beta(\beta+1)I_{ref}}{I_S M} - \left(\frac{V_T}{I_{b1}M} + R_2\right)\Delta I_{be} \qquad (2)$$

$$\text{with } M = \left\{ \beta(\beta+1)+1+\frac{N_2}{N_1} \right\}$$

Equation (2) is rewritten as

$$V_{be} = C_1 - (C_2 + R_2)\Delta I_{be} \qquad (3)$$

where C_1 and C_2 are constant. The equation (3) shows that, if R_2 is chosen as the minimum value that satisfies the correct current division, V_{be} is almost independent of ΔI_{be}. The LNA has good linear performance because its operating point is hardly changed.

In general, the linearity of the LNA can be increased by increasing the current of whole circuit. The one of the effective methods for improvement of the linearity is to increase current of the main transistor, not the whole circuit. It can be realized by using smaller R_2 for more drive current. Then, the relation of the resistors is modified as $R_1N_2 = \alpha R_2N_1$ where α is constant over 1, and the relation of the current become very complex. Nevertheless, V_{be} is derived similarly to the equation (3) except for the change of constant values, C_1 and C_2. The optimum resistors can be obtained by simulation using Agilent Advanced Design System (ADS). In consequence, the resistors of R_1 and R_2 are 1500 Ohm and 30 Ohm in our work.

2.2 Low gain mode

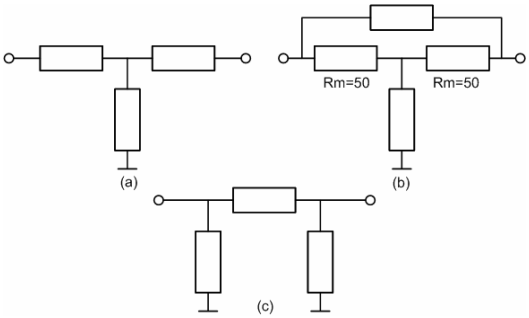


Figure 2. Resistor Attenuator topologies
a) T b) bridge-T c) ∏

When the LNA operates in a high gain mode, the mixer at the following stage can be saturated for a high input signal. The saturated signal generates non-linear components and decreases the linearity. For solving the problem, the LNA has to operate in either high gain mode or low gain mode according to the input signal level. The LNA should operate as an attenuator at the low gain mode. Attenuator topologies applicable to transistor-based integrated circuits are the T type, the bridge-T type and ∏ type as shown figure 2. T attenuators are the best suited for high source and load impedance level, but matching to 50Ohm is difficult. On the other hand, the bridge-T attenuators can be easily matched since the resistor R_m directly defines the impedance level. But they do not allow large attenuation values. The ∏ configuration has the benefits of large attenuation range and good matching to 50Ohm with realizable transistor sizes [8]. Therefore, the ∏ attenuator is used in this work. The attenuation value and reflection coefficients determine the size of the transistors.

2.3 Design and simulation results

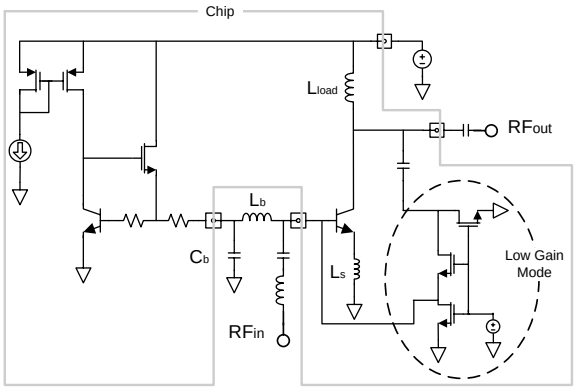
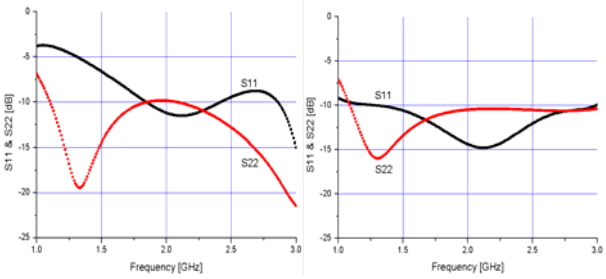


Figure 3. Dual mode LNA circuit

The general structure of LNA is either cascode structure or single transistor structure. The cascode structure is easy to match and has good stability due to its good input/output isolation, but NF is not good. Hence, the design shown in figure 3 is based on a single transistor structure for better NF.



(a) high gain mode (b) low gain mode

Figure 4. Reflection coefficients

Table 1. Simulation results

Mode	Gain [dB]	NF [dB]	IIP3 [dBm]	VSWR [dB]	Current [mA]
High	14.5	1.6	0.9	-11/-10	7.5
Low	-11	11.5	22	-14/-10	2.2

The basic circuit is designed by ADS. In addition, the post-simulation after the layout is carried out by Cadence's SpectraRF. The supply voltage is 2.7V for both

modes. The simulation results are given in table 1. At the high gain mode, total current of the LNA is 7.5mA, VSWR is under 2:1, NF is 1.6dB and the input IP3 is 0.9dBm and at the low gain mode, total current is 2.2mA, VSWR is under 2:1, NF is 11.5dB and the input IP3 is 22dBm.

2.4 Measured data

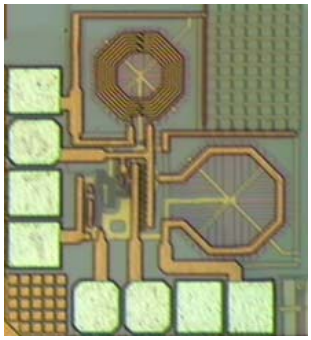


Figure 5. The layout photograph of the LNA

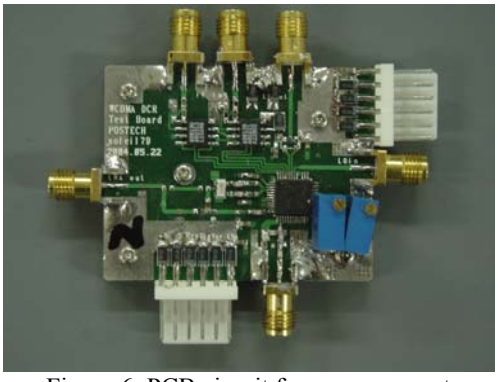


Figure 6. PCB circuit for measurement

The microphotograph of the circuit is shown in figure 5, whose size is 400*450um^2 and the PCB circuit for measurement is shown in figure 6.

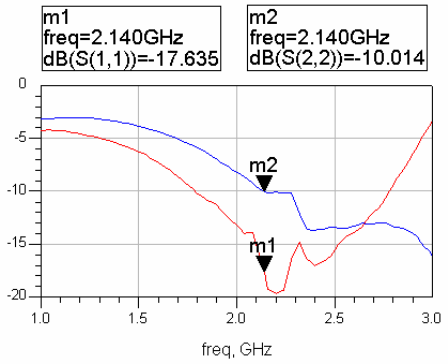


Figure 7. The reflection coefficients in high gain mode

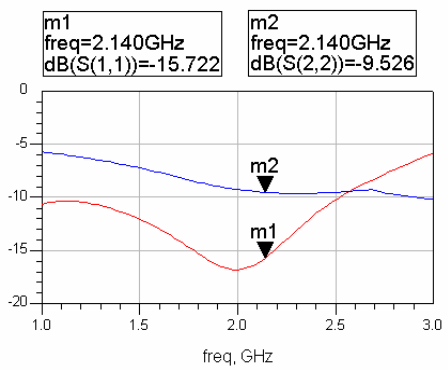
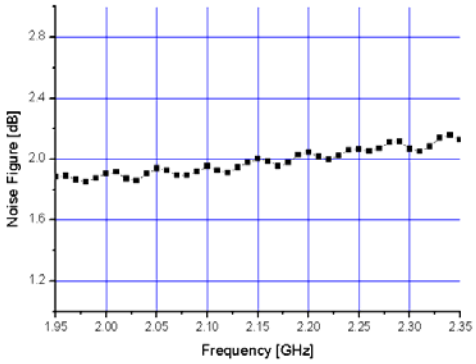
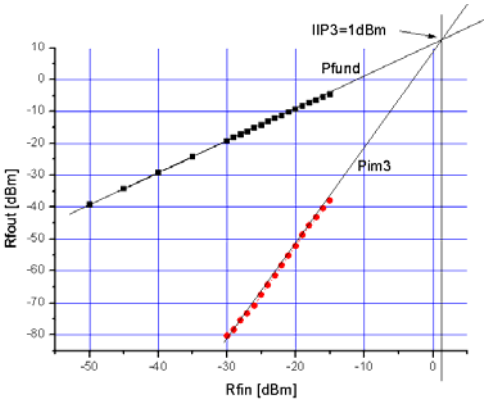


Figure 8. The reflection coefficients in low gain mode

The reflection coefficients are measured using an HP 8510C network analyzers, and the results are shown in figures 7 and 8. At the high gain mode, the total current of the LNA is 7.5mA and the input/output VSWR is -17.6dB /-10.0dB and at the low gain mode, total current is 2.2mA and the input/output VSWR is -15.7dB/-9.5dB.



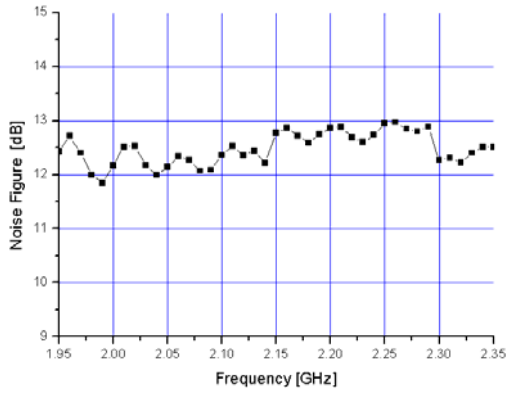
(a) NF



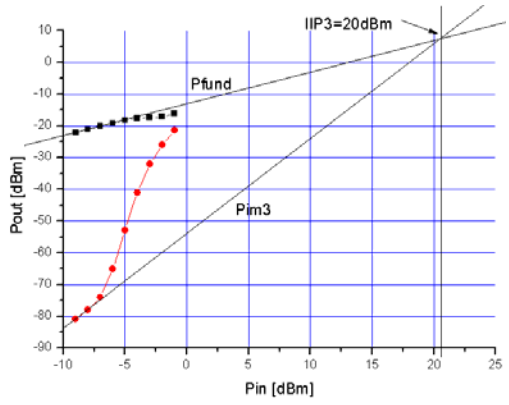
(b) Gain Curve

Figure 9. The NF and Gain curves in high gain mode

Figure 9 shows that the gain is 12.5dB and NF, measured by an Agilent N8975A Noise Figure Analyzers (NFA), is 1.96dB and input IP3 (100kHz tone spacing) is 1dBm at the high gain mode.



(a) NF



(b) Gain Curve

Figure 10. The NF and Gain curves in low gain mode

Figure 10 shows that the gain is -12dB, NF is 12.5dB and the input IP3 is 20dBm at the low gain mode. Comparisons of the LNA in simulation data and measured data are given in table 2. The measured data show that the gain of the LNA is reduced in comparison with the simulation data due to the loss of the connector and printed circuit board. Also the gain is reduced by the bonding inductors and the process variation of the inductor added to emitter for stability

Table 2. Simulation & Measured data

Mode	High gain mode		Low gain mode	
	Simulation	Measured	Simulation	Measured
Gain [dB]	14.5	12.5	-11	-12
NF [dB]	1.6	1.96	11.5	12.5
IIP3 [dBm]	0.9	1	22	20
VSWR [dB] (Input/Output)	-11/-10	-17/-10	-14/-10	-15/-9
Current	7.5	7.5	2.2	2.2

3 Conclusions

We have developed a dual mode LNA with good linearity. The novel bias circuit with inductor and resistors which have asymmetric values contributes to the improvement of linearity of the LNA, and maintains low current consumption compared with symmetric values. At the high gain mode, the gain is 12.5dB, NF is 1.96dB and the input IP3 is 1dBm and at the low gain mode, the gain is -12dB, NF is 12.5dB and the input IP3 is 20dBm, and the gain difference is over 24dB.

Acknowledgement

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