Ultra High-Speed 0.25-μm Emitter InP-InGaAs SHBTs with f_{max} of 687 GHz

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Abstract - We have developed novel but simple process techniques for high speed InP SHBTs. For parasitic reduction, the collector layer is undercut using an etch-stop layer, the base pad is isolated, and the emitter metal is widened using thick plated gold. For transit time reduction, the SHBT employs InGaAs base with graded In-composition and InGaAlAs emitter setback with graded Al-composition. Maximum extrapolated f_{max} of about 687 GHz with f_T of 215 GHz is achieved for 0.25 × 8 μm^2 emitter area devices at I_C = 8 mA and V_{CE} = 1.5 V. These data clearly show that the optimized conventional process can offer direct implementation of InP HBT for high-speed electronic circuit fabrication.

Introduction

The fundamental material properties of InP are exceptionally well suited to high-speed HBTs for digital, microwave, and opto-electronic applications. The InP-based HBTs promise higher current gain cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) as the devices are vertically and laterally scaled down. However, the increase in f_T by vertical scaling of epilayer may come at the expense of f_{max} if parasitic components are not carefully controlled. Among the parasitic components, base collector capacitance (C_{bc}) is the most importance parameter as the collector layer is vertically scaled down. A large part of C_{bc} originates from the extrinsic base area in the mesa structured HBT. A simple collector undercut is the most widely used technique to reduce C_{bc} of InP Double-HBTs (DHBTs) due to the selective etching nature [1]- [3]. The air filling gap between the base layer underneath the base contacts and a subcollector has the lowest relative dielectric constant of unity. In the case of Single-HBTs (SHBTs), however, the base layer is also etched during the undercut process because the selective etch cannot be employed. Several undercut techniques have been employed to reduce C_{bc} in SHBTs [4] [5] but yields for the processes are usually bad due to the complicated processes, especially for scaled-down devices.

In this paper, we report a high speed SHBT based on a conventional mesa structure with the 0.25 μm emitter width and the development of novel but simple process techniques for reduction of not only C_{bc} but also other parasitics for realization of the high speed InP SHBTs. To reduce C_{bc}, collector layer is undercut using an etch-stop layer in the SHBT, similar to the undercut process in the DHBT and a base-pad-isolation structure is utilized, which can eliminate the capacitance at the base-pad area. The base resistance (R_b) is minimized by maximizing the base doping (8.0 × 10^{19} cm^{-3}), placing the base ohmic contact as close to the emitter junction as possible and optimizing the base contact resistivity (ρ_{BC}). Additionally, the emitter parasitic resistance and inductance are minimized by using emitter metal widening and air-bridge structures with plated thick gold. These optimized conventional processes deliver extremely high speed InP SHBTs.

Design and Fabrication

The epitaxial layer of the HBTs is grown by a Solid Source Molecular Beam Epitaxy on a Fe-doped semi-insulating (100) InP substrate. The layer structure includes, from the top, InGaAs emitter contact layer, InGaAlAs graded layer, InP emitter layer (700 Å, Si-doped to 7.0 × 10^{17} cm^{-3}), InGaAs base layer with Indium mole fraction graded from of 0.46 to 0.53 (400 Å, C-doped to 8.0 × 10^{19} cm^{-3} with 20 Å spacer), InGaAs collector layer (2500 Å, Si-doped to 2.0 × 10^{16} cm^{-3}), and InGaAs subcollector layer(6000 Å, Si-doped to 1.0 × 10^{19} cm^{-3}).

An important addition is two InP etch-stop layers for the undercut process of SHBTs. Due to the etch-stop layers, the undercut process similar to the DHBT can be employed without a base layer etch problem [6]. Therefore, the base contact resistance is kept low. Fig. 1 compares the f_{max} of the new undercut process and conventional undercut process devices calculated using our own models. As shown, f_{max} of

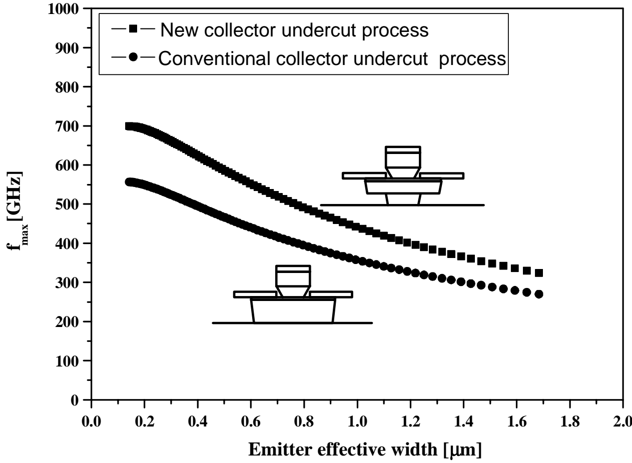

Fig. 1. Comparison of the new collector undercut device and conventional device for scaled down devices

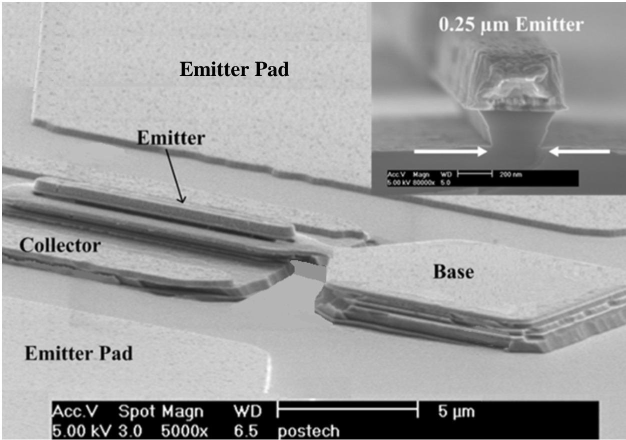

Fig. 2. SEM pictures for the fabricated HBT with a 0.25 × 8 μm^2 emitter area

above 700 GHz can be achieved using the new process for the deep submicron scaled device.

The devices are fabricated using a standard mesa process. Emitters are defined using the contact lithography, resulting in a minimum emitter metal width of about 0.5 μm. The emitter is slightly undercut, resulting in an effective 0.25 μm size. The self-aligned Pt/Ti/Pt/Au base metal having 1 μm width is evaporated. The base and collector layers are etched with a citric-based etchant. In this etching process, the collector undercut process is also carried out. Next, a Ti/Au emitter widening metal is evaporated. The subcollector is etched for device isolation. In this etching process, the active base area and the base area for the interconnecting base pad are isolated. Next, Ti/Pt/Au collector metal and pad metal are evaporated. Lastly, Au air-bridge formation is followed. The whole process flow and the detailed process can be referred to our paper [7].

SEM pictures of the fabricated HBT are shown in Fig. 2. For the high speed InP HBTs, the base-to-emitter spacing measured by SEM picture is about 0.13 μm. Also the base resistance (R_b) is minimized by maximizing the base doping (8.0 × 10^{19} cm^{-3}) and optimizing the base contact resistivity. Additionally, the emitter parasitic resistance and inductance are minimized by using emitter metal widening and an air bridge structure using plated thick gold.

Device Measurement Results

A. DC performance

I-V curves of the HBT with 0.25 × 8 μm^2 emitter area are measured and depicted in Fig. 3. As shown, the common-emitter dc current gain (β) and breakdown voltage of the fabricated HBTs are about 23 and above 4 V, respectively at a collector current density of 1 × 10^5 A/cm^2. Breakdown voltage of the HBTs at an open base, BV_{CEO}, is very high, above 5 V. The base sheet resistance (R_{SB}) of 472 Ω/□ (hole mobility ≅ 41.38cm^2/V·s for 400 Å thick C-doped to 8.0 × 10^{19} cm^{-3} base) and specific contact resistivity (ρ_{BC}) of 1.65 × 10^{-7} Ω•cm^2 are measured using transmission line measurement (TLM). The transfer length L_T, expressed as $(\rho_{BC}/R_{SB})^{1/2}$, is 0.19 μm and the base contact resistance is maintained low.

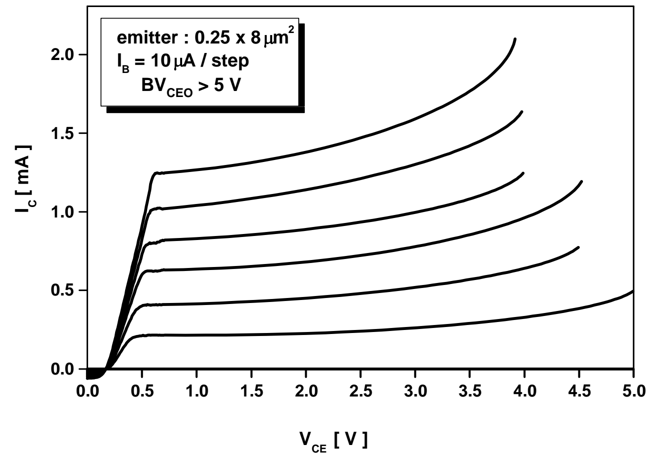

Fig. 3. Common emitter I_C-V_{CE} characteristics of the fabricated HBT with a 0.25 × 8 μm^2 emitter area

B. Microwave performance

The microwave performances of the HBT are characterized by on-wafer S-parameter measurements for 0.5-40 GHz and 50-75 GHz bands using an Agilent 8510C network analyzer calibrated by thru-reflect-line (TRL) method.

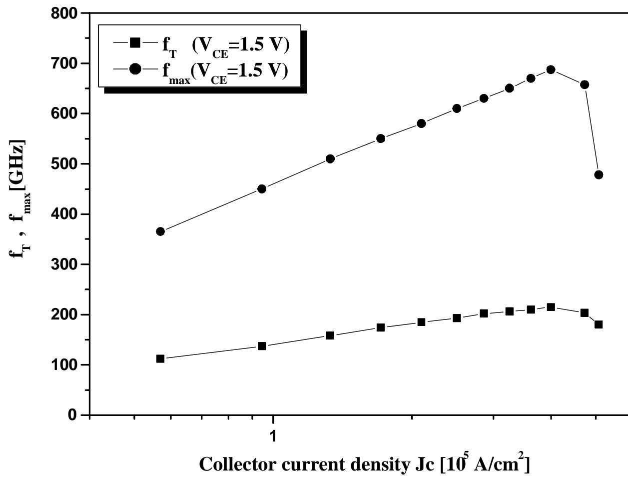

Fig. 4. Dependence f_T and f_{max} on collector current density of the fabricated HBT with a 0.25 × 8 μm^2 emitter area

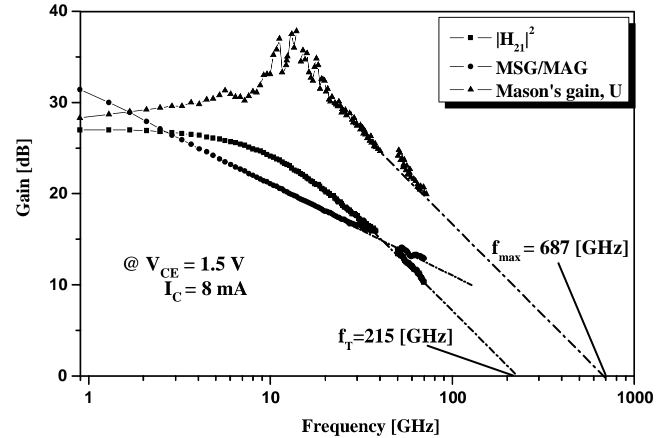

Fig. 5. Frequency dependencies of $|h_{21}|^2$, MSG/MAG, and Mason's gain at I_C = 8 mA and V_{CE} = 1.5 V.

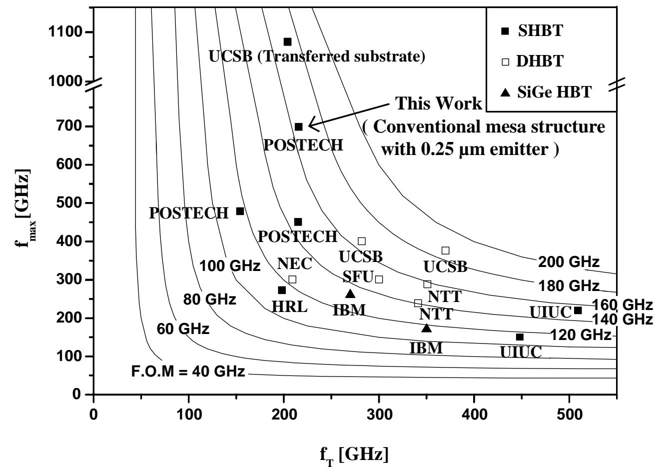

Fig. 6. Overview of f_T and f_{max} data for high Speed HBTs. The figure-of-merit (F.O.M) for D-type flip/flop ICs defined as $f_T \cdot f_{max}/(f_T+f_{max})$

Fig. 4 shows the dependence of f_T and f_{max} on collector current density at 1.5 V collector bias. The frequency dependence of the current gain, Mason's unilateral gain, and maximum stable gain/maximum available gain are shown in Fig. 5. The Mason's unilateral gain curve for pad-deembedding case is smooth and follows the –20 dB/decade frequency dependence very well. The pad-deembedding is inevitable for the characterization of the small size device because the pad parasitic components are not negligible compared with the intrinsic device components. The estimated f_T and f_{max} of the HBT are 215 GHz and 687 GHz, respectively, at I_C = 8 mA and V_{CE} = 1.5 V. From the measured S-parameters, small-signal model parameters of the device are extracted based on an HBT equivalent hybrid-π model and are evaluated. An excellent forward transit time (τ_B+τ_C) of 0.63 ps, associated with the 40-nm base/250-nm collector device, is achieved by the Indium mole fraction graded base with about 40 meV of potential drop [8]. Despite the conventional structure, the time constant $R_b \cdot (C_{bc,i}+C_{bc,x})$ is very low, about 17 fs, due to the base contact optimization, the base-pad isolation and new collector undercut. These improved structure results in a very high-speed SHBT. Fig. 6 compares the f_T and f_{max} of our HBTs with those taken from literature. It can be seen that excellent f_{max} is obtained by using the proposed novel but simple process techniques for parasitic reduction. Also, based on the figure-of-merit for D-type Flip-Flop ICs defined as $f_T \cdot f_{max}/(f_T+f_{max})$ [9], Postech SHBT with 0.25 μm emitter area deliveries the top performance among InP-based HBTs.

Conclusions

High-speed InP/InGaAs SHBTs are fabricated by using the Postech process. For the parasitic reduction, the collector layer is undercut using the etch-stop layer, base pad is isolated, and emitter metal is widened using thick plated gold. A high frequency performance of f_T = 215 GHz and f_{max} = 687 GHz is obtained from the HBT with a 0.25 × 8 μm^2 emitter area. This is the highest f_{max} ever reported for a mesa HBTs, as far as the authors know. As the device is scaled down further, especially vertical scaled down, the device RF performance will be enhanced further. These data clearly indicate that this conventional process can be a practical technique for implementation of the InP HBT for high-speed electronic circuits.

Acknowledgement

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Industry and Energy

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