CDMA Handset Power Amplifier with a Switched Output Matching Circuit for Low/High Power Mode Operations

Seungwoo Kim, Jongwoo Lee, Jinho Shin*, and Bumman Kim

Department of Electronic and Electrical Engineering and Microwave Application Research Center, Pohang University of Science and Technology, Kyoungbuk, 790-784, Republic of Korea
*FCI Inc., 6-8 Sunae-Dong Pundang Gu, Sungnam City, Kyounggi-Do, 463-020, Republic of Korea

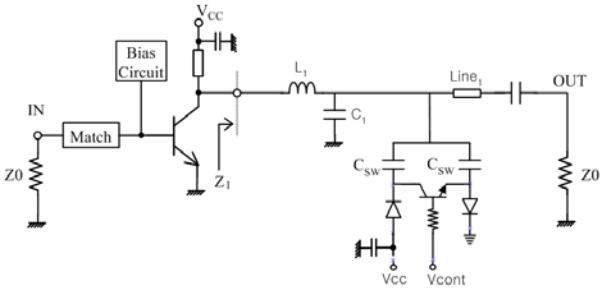
Abstract **This paper presents a switched output matching circuit for low/high power modes using a novel structure switch. By adjusting the output matching circuit for the power levels, the efficiency at a low-power region is improved significantly without compromising linearity and efficiency at a high-power region. This switched power amplifier provides 13% power-added efficiency(PAE) with adjacent-channel-power-ratio(ACPR) less than –48 dBc at an output power level of 16 dBm and 41% PAE with ACPR less than –43 dBc at 28 dBm.**

I. INTRODUCTION

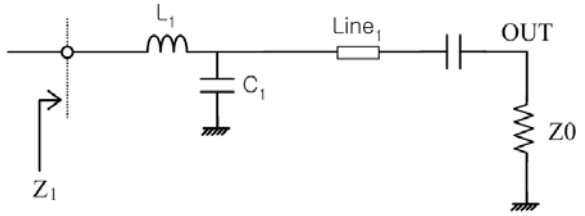
CDMA mobile communication systems impose stringent requirements on power amplifiers for efficiency and linearity. The simultaneous achievement of high efficiency and linearity makes the power amplifier design difficult since there is a strong trade-off between the two. Moreover, the efficiency of the handset power amplifier at a low-power region is of prime interest due to battery lifetime because the handset operating power level is mostly less than 17 dBm [1]-[3] while the maximum power is about 28dBm. So far several efficiency enhancement techniques have been proposed, such as Doherty-type amplifiers [4]-[6] and bias control-type amplifiers[7]. One simple method to achieve a compromised result is to adopt a class-AB biasing scheme. However, simple class-AB biasing has its own limits in efficiency. We are proposing a switched-type output matching circuit using a novel structure switch. By adjusting the output matching circuit for low and high power modes, the efficiency at a low-power region can be improved without compromising any linearity and efficiency for the high-power region. Using the control signal that is already available from the baseband controller of CDMA handsets, the bias point and output matching of the amplifier are controlled, depending on the TX power requirements.

II. DESIGN AND FABRICATION

Figure 1(a) shows a schematic of the switched output matching circuit for the power amplifier. The output circuit is composed of output matching and switching components. Figures 1 (b) and (c) show the switch off and on state equivalent circuits. Figure 2 shows the Class AB load lines and bias points for the two switch modes.



(a)



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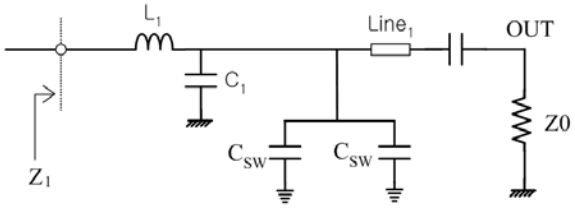

(c)

Fig. 1 (a) Schematic of a power amplifier with switched output matching circuit, (b) Equivalent output circuit for switch-off state, (c) Equivalent output circuit for switch-on state.

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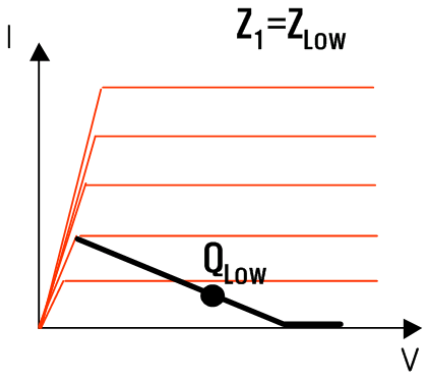
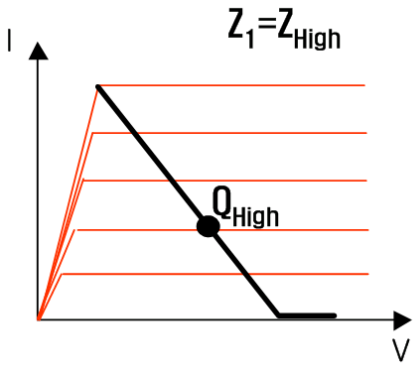


(a)



(b)

Fig. 2 Class AB load line and bias point. (a) Low power mode. (b) High power mode

To obtain an enhanced efficiency at a low power mode, impedance Z_1 must be increased and the bias current must be decreased. To achieve the requirements, we employ a switched output matching circuit with base bias control.

For efficient load impedance modulation, a low loss switch is an extremely important design issue. Figure 3 shows the novel structure switch we have employed. The switch has several merits such as a high power handling capability, a low switch control current(<10 μA),a nearly zero level even harmonic generation by the two diode out-phasing arrangement. This diode assisted switch shows a lower insertion loss than the transistor switch since the RF path is separated from the lossy DC path. The DC path includes a lossy transistor for a low control current of the switch. Additionally, the proposed switch does not need an RF choke inductor. Figure 4 shows the impedance transformation trajectory on the smith chart according to the switch state. For the switch-off state, load impedance Z0 is transformed to a low mode impedance level $Z_1=Z_{Low}$ by transmission line $Line_1$(Z0 to Z_a), shunt capacitor C_1 (Z_a to Z_b) and series inductor L_1 (Z_b to Z_{Low}) as shown figure 1(b). For the switch-on state, load impedance Z0 is converted to high impedance level $Z_1=Z_{High}$ by transmission line $Line_1$(Z0 to Z_a), two shunt capacitor C_{SW}(Z_a to Z_c) of switch structure, shunt capacitor C_1(Z_c to Z_d) and series inductor L_1(Z_d to Z_{High}) as shown in figure 1(c).

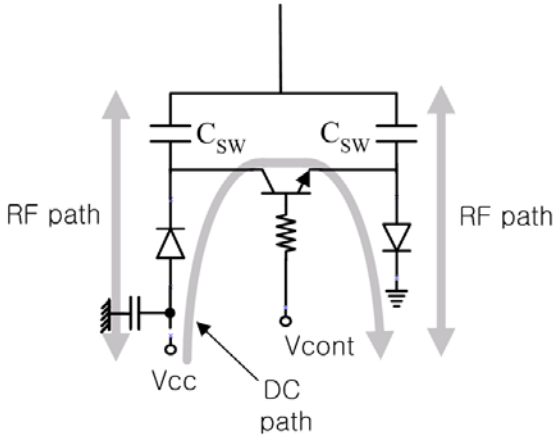


Fig. 3. RF path and DC path of the novel structure switch.

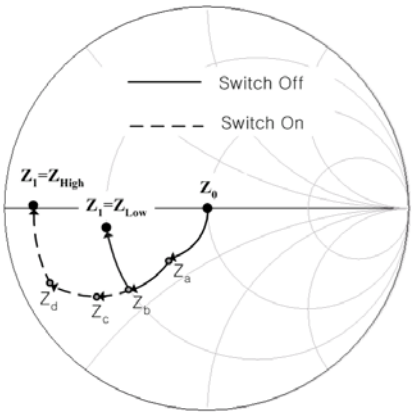


Fig. 4. Impedance transformation trajectories from Z0 to Z_{Low} and Z0 to Z_{High}

A circuit block diagram of the switched power amplifier module (PAM) is shown in figure 5 and the die micrograph is shown in figure 6. The 1.0x1.0 mm^2 die is mounted directly on FR4 PCB. A 2x40 um^2 x 10 unit-cell HBT is used for the drive stage, a 2x40 um^2 x 64 unit-cell HBT is used for output stage, and 2x40 um^2 x 20 unit-cell HBT is used for the switch. To reduce RF power loss, output matching circuit and C_{SW} are off-chip components, as shown in figure 5.

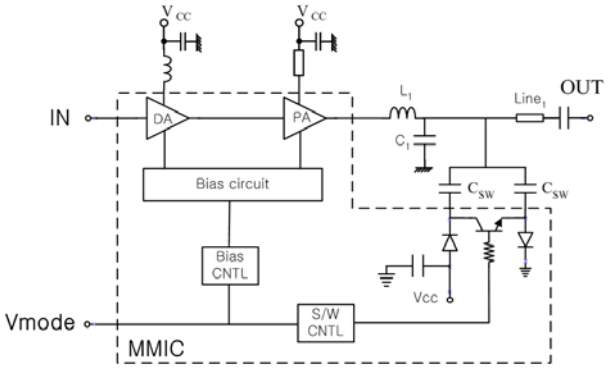


Fig. 5 Block diagram of the power amplifier with switched-type output matching.

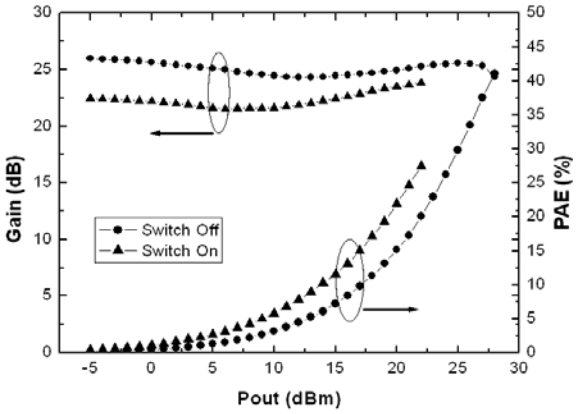


Fig. 7 Measured gain and PAE versus output power.

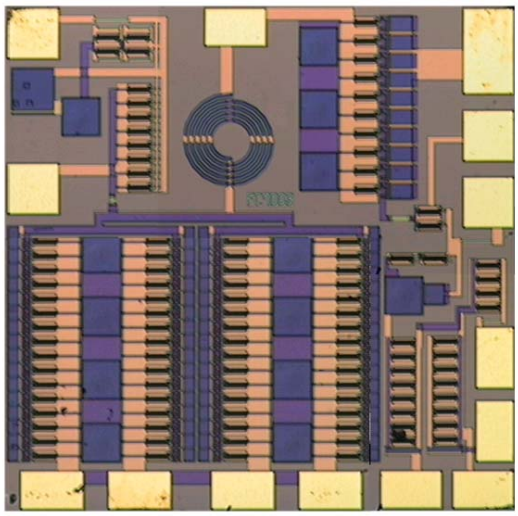


Fig. 6. Die micrograph.

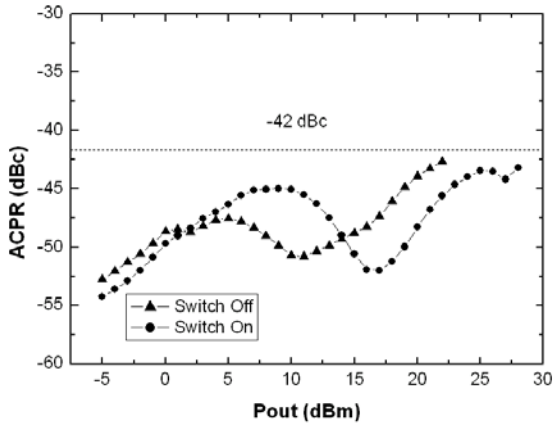


Fig. 8 Measured ACPR versus output power.

III. Measurements and Discussions

Figures 7 and 8 show gain, PAE, and ACPR of the amplifier at Vcc=3.4 volt for reverse-link IS-95A signal at a chip rate of 1.2288 Mcps at Korean cellular band (center frequency=836.5 MHz). The low-power mode is selected to operate at Vmode=0 volt and the high-power mode at Vmode=2.85 volt. For the low-power mode, PAE of 13 % and ACPR of –48 dBc are achieved at an output power of 16 dBm. In the high-power mode, PAE of 41 % and ACPR of –43 dBc are achieved at the output power of 28 dBm.

IV. Conclusion

To enhance the low power efficiency of the amplifier for CDMA handset application, the load modulation technique using a switch-type output matching has been proposed and demonstrated. By employing a novel structural switch, the proposed amplifier could operate in two different modes successfully: “High impedance” mode for a low power operation and “Low impedance” mode for a high power operation. In this way, the efficiency at a low power region could be optimized and this switched power amplifier delivers 13% PAE with ACPR less than –48 dBc at an output power level of 16 dBm and 41% PAE with ACPR less than –43 dBc at 28 dBm.

Acknowledgement

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REFERENCES

[1] J. F. Sevic, "Statistical Characterization of RF Power Amplifier Efficiency for CDMA Wireless Communication Systems," *IEEE Wireless Communications Conference*, pp. 110-113, 1997.

[2] P. M. Asbeck, and L. E. Larson, "Synergistic Design of DSP and Power Amplifiers for Wireless Communications," *Proc. APMC-2000*, Dec. 2000.

[3] T. Fowler, K. Burger, N. S. Cheng, A. Samelis, E. Enobakhare, and S. Rohlfing, "Efficiency Improvement Techniques at Low Power Levels for Linear CDMA and WCDMA Power Amplifiers," *IEEE RFIC Symposium Digest*, pp. 41-44, 2002.

[4] M. Iwamoto, A. Williams, P. F. Chen, A. Metzger, C. Wang, L. E. Larson, and P. M. Asbeck, "An Extended Doherty Amplifier with High Efficiency Over a Wide Power Range," *IEEE MTT-S Digest*, Jun. 2001.

[5] Y. Yang, J. Yi, Y. Y. Woo, and B. Kim, "Optimum Design for Linearity and Efficiency of a Microwave Doherty Amplifier using a New Load Matching Technique," *Microwave Journal*, pp. 20-36, Dec. 2001

[6] J. Cha, Y. Yang, B. Shin, and B. Kim, "An Adaptive Bias Controlled Power Amplifier with a Load-Modulated Combining Scheme for High Efficiency and Linearity," *IEEE MTT-S Digest*, Jun. 2003.

[7] K. Yang, G. I. Haddad, and J. R. East, "High-Efficiency Class-A Power Amplifiers with a Dual-Bias-Control Scheme," *IEEE Trans. Microwave Theory Tech.*, vol. 47, no. 8, pp. 1426-1432, Aug. 1999.