

Development of Linear Channel-Selection Filter for Direct Conversion Receivers

Sangsu Jin, Seonghan Ryu, Huijung Kim, and Bumman Kim

Department of E.E.E., POSTECH
Pohang, Korea
codeone@postech.ac.kr

Jong-Ryul Lee

Future Communications IC
Sungnam, Korea
jrlee@fci.co.kr

Abstract - An active RC 2nd order Butterworth filter suitable for a baseband channel-selection filter for a direct conversion receiver is presented. The linearity of the 2nd order Butterworth filter is analyzed. In order to improve the linearity of the filter, the operational amplifiers should have a high linear gain and low 3rd harmonic, and the filter should be designed with a low gain. This second order Butterworth filter achieves -14dBV in-channel (400kHz, 500kHz) IIP3, +29dBV out-channel (10MHz, 20.2MHz) IIP3 and -15.6 nV/ $\sqrt{\text{Hz}}$ input-referred noise and dissipates 10.8mW from a 2.7-V supply. The analysis and experimental results are in good agreement

Keywords: Analog integrated filter, passive matrix frequency tuning, linearity analysis, operational amplifier (OPAMP), active-RC filter, channel-selection filter.

1 Introduction

Direct conversion receivers (DCR) convert directly the carrier frequency of the desired signal to the zero frequency in the first mixer, and this architecture eliminates all intermediate frequency circuitry in conventional superheterodyne receivers. Thus, the manufacturing cost can be reduced by minimizing the number of required components and the die area of integrated circuits [1]. Because the baseband part of DCR deals with low frequency around DC, they do not require high-Q filtering. Therefore, the DCR filter can be integrated in IC form.

The role of a channel-selection filter in DCR is to select the desired signal following RF mixer without any distortion and to reject the out-of-band signal. If harmonic blockers pass through the filter without attenuation, a baseband circuit may be saturated by the large blocker. Then, the intermodulation products generated inside of the baseband can degrade the bit error rate (BER). Consequently, the channel-selection filter should have a good linearity and shape channel-selection [2]. It is a difficult task to satisfy these requirements and is a key point in the design of the integrated channel-selection filter for DCR. In order to achieve highly linear performance in the integrated filter, active RC filter is employed quite often [3, 4].

This paper shows the design methodology for linear filter and utilizing the analysis, the filter is designed and implemented. In section II, the analysis of the linearity of filters related to OPAMP properties and passive components used in filters are discussed. In section III, the design of the filter having good linear performance is discussed. Implementation and measurement results are provided in Section IV. Finally, conclusions of this work is made in section V

2 Linearity Analysis

For the balanced design, the second harmonic does not exist if there are not any process variations. Thus, the third harmonic is the important criterion of the linearity and analysis of the third harmonic gives us a good way to improve the linearity.

An input of the equation (1) is applied to a nonlinear circuit, then output of the equation (2) is generated. In the equation (2), coefficients $a_0, a_1, a_2,$ and a_3 represent the dc, linear gain, second harmonic, and third harmonic conversion factors, respectively.

$$x(t) = U \cos(\omega t) \quad (1)$$

$$y(t) = (a_0 + \frac{a_2}{2} U^2) + (a_1 + \frac{3}{4} a_3 U^2) U \cos(\omega t) + \frac{a_2}{2} U^2 \cos(2\omega t) + \frac{a_3}{4} U^3 \cos(3\omega t) + \dots \quad (2)$$

Applying negative feedback to this nonlinear circuit, we can model the equivalent circuit of figure 1 [5].

$$H_1(s_1) = \frac{a_1}{1 + a_1 f(s_1)} \quad (3a)$$

$$H_2(s_1, s_2) = \frac{1}{1 + f(s_1) a_1} \times \frac{a_2}{1 + f(s_2) a_1} \times \frac{1}{1 + f(s_1 + s_2) a_1} \quad (3b)$$

$$H_3(s_1, s_2, s_3) = \frac{1}{1 + a_1 f(s_1)} \times \frac{a_3}{1 + a_1 f(s_2)} \times \frac{1}{1 + a_1 f(s_3)} \times \frac{1}{1 + a_1 f(s_1 + s_2 + s_3)} \quad (3c)$$

Coefficients $H_1, H_2,$ and H_3 in equation (3) represent Volterra Kernels of equivalent linear, second, and third harmonic gains of feedback circuit using volterra series,

respectively. Coefficient f represents the transfer function of unilateral feedback network [6].

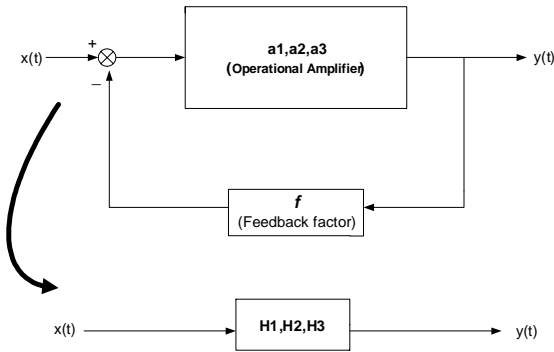


Figure 1. Equivalent model of a feedback circuit.

A second order active RC filter can be modeled using this approach as shown in figure 2, where the filter is composed of two integrators.

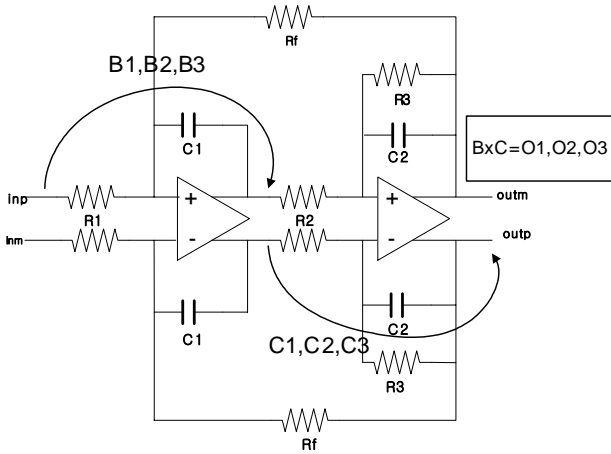


Figure 2. Modeling of a 2nd order filter.

In order to find the transfer functions of each integrator, feedback factors of each integrator $f_{B1}(s)$ and $f_{C1}(s)$ should be known.

$$f_{B1}(s_1) = sR_1C_1 + \frac{R_1R_3}{R_f(R_2 + s_1R_3R_2C_2)} \quad (4a)$$

$$f_{C1}(s_1) = \frac{R_2}{R_3} + s_1C_2R_2 \quad (4b)$$

Although the first stage feedback loop includes the second stage feedback loop, nonlinear properties of that feedback loop are neglected. Because the feedback loop does not generate any harmonics. The transfer functions of the linear gain, second, and third harmonics of each integrator can be represented by equation (3). The transfer function properties of each integrator are denoted by B1, B2, B3

and C1, C2, C3. Coefficients O1, O2, and O3 in equation (5) representing the transfer functions of the second order filter are obtained by cascading the two integrators.

$$O_1(s_1) = B_1(s_1) \times C_1(s_1) \quad (5a)$$

$$O_2(s_1, s_2) = C_1(s_1 + s_2) \times B_2(s_1, s_2) + C_2(s_1, s_2) \times B_1(s_1) \times B_1(s_2) \quad (5b)$$

$$O_3(s_1, s_2, s_3) = C_3(s_1, s_2, s_3) \times B_1(s_1) \times B_1(s_2) \times B_1(s_3) + C_1(s_1 + s_2 + s_3) \times B_3(s_1, s_2, s_3) \quad (5c)$$

IIP3 of the filter should be defined by

$$IIP3i(\text{dBV}) = IMDi * 0.5 + \text{input}(\text{dBV}) \quad (6)$$

where

$$\text{input}(\text{dBV}) = 20 * \log(V_{\text{input}}) \quad (7a)$$

$$IM3(\text{dBV}) = 20 * \log\left(\frac{3}{4} * O_3(s_1, s_1, -s_2) * V_{\text{input}}^3\right) \quad (7b)$$

$$IMDi(\text{dBV}) = \text{input}(\text{dBV}) - (IM3 - \text{Gain}) \quad (7c)$$

Figure 3 shows the comparison between the analysis based on equation (5) using MATLAB and simulation using Agilent Advanced Design System (ADS). The calculated linear gain of the filter denoted by O1 matches very closely to the simulation results. However, the third harmonic denoted by O3 differs from the simulation with increasing frequency. The difference between the simulation and analysis are caused by neglecting the harmonics over fifth order in the calculation, assuming perfect cancellation of even order harmonics in differential mode operation, and neglecting the nonlinear characteristics of the feedback loops.

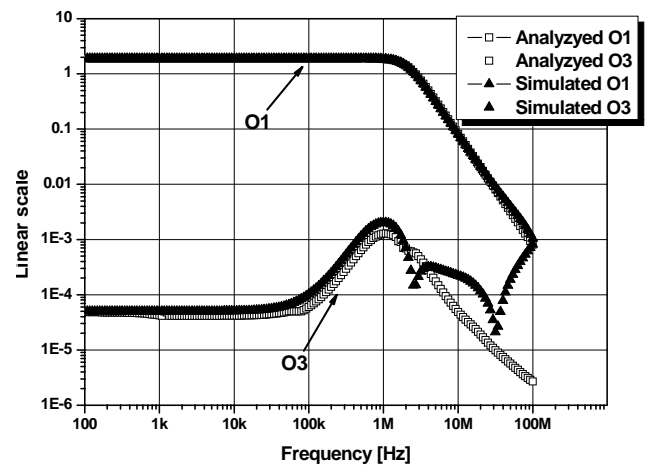


Figure 3. Comparison of analysis results.

Based on the result of the analysis, we can see that the linearity of the filter can be improved by implementing an OPAMP with a high linear gain and low third harmonic. The high feedback factor at the price of lower gain also enhances the linearity. Also, increasing the bandwidth of

the linear gain of an OPAMP improves a linearity of the filter as lower third intermodulation (IM3) can be achieved at a high frequency. However, methods of transistor scaling and consuming more currents for increasing bandwidth of an OPAMP are in trade-off.

3 Filter Design

Based on the analysis of section II, a second order active RC Butterworth filter is designed as shown in figure 2. This filter has the cut-off frequency of 2.1 MHz with 5dB transfer gain. Its role is a pre-filter in front of the fourth order elliptic filter for WCDMA applications. The equation (8) represents the transfer function of the filter.

$$H(s) = \frac{1}{R_1 R_2 C_1 C_2} \frac{1}{s^2 + s \left(\frac{1}{C_1 R_3} + \frac{1}{C_1 C_2 R_f R_2} \right)} \quad (8)$$

and $\omega_n^2 = \frac{1}{C_1 C_2 R_f R_2}$, DC-Gain = $\frac{R_f}{R_1}$

The transfer gain, cut-off frequency, and noise performance are defined by both resistors and capacitors. Because noise performance is determined by passive resistors, it is necessary to select appropriate values of resistors [7, 8]. The schematic of the OPAMP used in the filter is shown in figure 4. It is implemented by differential mode and the common mode voltage at the output load is defined by common mode feedback circuit (CMFB) [9]. Current consumption of each OPAMP is 0.75mA and common mode voltage is 1.5V.

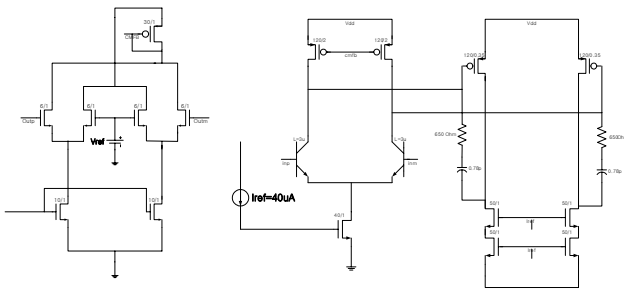


Figure 4. Fully differential OPAMP circuit with CMFB.

The cut-off frequency of an active RC type filter is defined by passive component values. Due to the variations in Bi-CMOS process the actual resistance and capacitance values of the integrated components may differ from the nominal values. These variations mean the variation of the cut-off frequency in the filter. Tuning circuit to compensate these variations has to be made tunable in active RC filter. A capacitor and resistor matrices shown in figure 5, make each value controllable

with possible tuning range of $\pm 20\%$ of the reference values

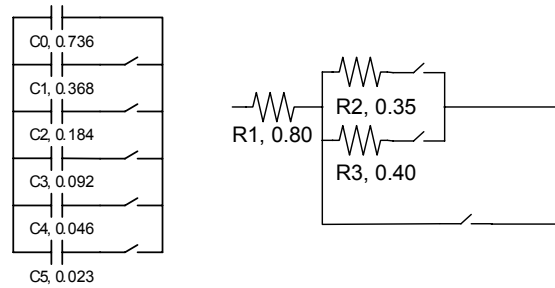


Figure 5. Passive matrices.

Figure 6 shows the chip photo using STM 0.35um Bi-CMOS technology. The chip consists of two filters for I-Q path and the size is 520um*310um. The capacitor and resistor matrices occupied 70% of the chip area

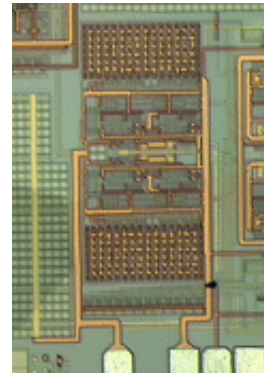


Figure 6. Microphotograph of the chip.

4 Measurement results.

For measurement, the passive transformer is used to convert the input and output signals from single ends to differential modes, and vice versa. The supply voltage is 2.7V. Figure 7 shows the measured tunable frequency response of the filter. The filter satisfies the cut-off frequency of 2.1MHz for WCDMA systems with the tunable frequency range of about 1.5MHz ~ 3.7MHz with total gain of 5dB.

The linearity of the filter is measured for both in-channel and out-channel IIP3. To measure the in-channel linearity, two tones of 300kHz and 500kHz, and out-channel linearity, 10MHz and 20.2MHz, are used. Figure 8 shows the measured and simulated IIP3 results of the filter according to input power variations. The measured performance is summarized in Table I.

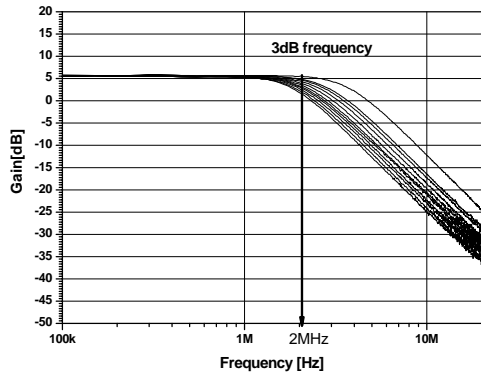


Figure 7. Passband response of the filter.

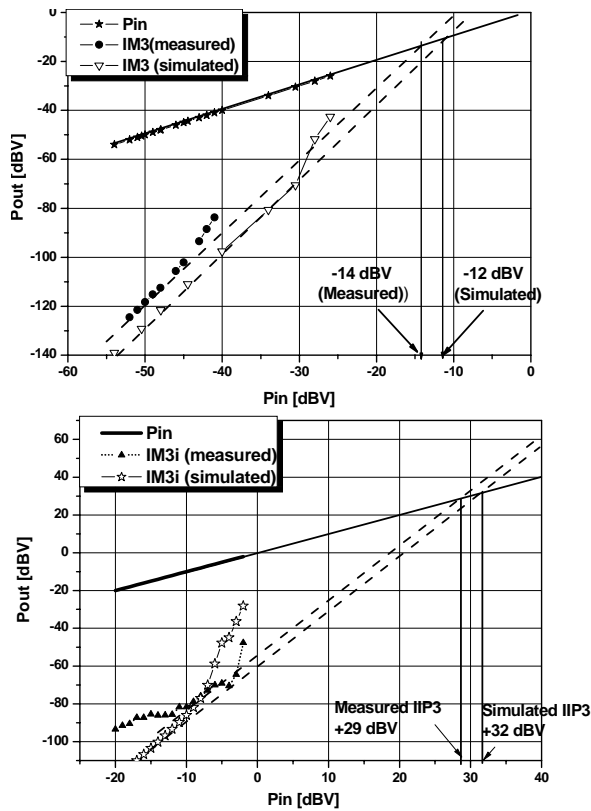


Figure 8. In-channel and Out-channel IIP3.

Table I. Summary of the filter performance.

Supply voltage	2.7V
Current consumption 2 nd -Butterworth filter	4 mA (I-Q included)
Cut-off frequency	2.1 MHz
In-band gain	5 dB
In-channel IIP3	-14 dBV
Out-channel IIP3	29 dBV
Input-referred noise	15.6 nV/ $\sqrt{\text{Hz}}$
Out-of-band rejection (@ 10MHz)	26 dB

5 Conclusion.

A second-order active RC channel-selection filter for DCR is presented. The filter meets the bandwidth specification of WCDMA standard using RC components tuning. The important performance of linearity of the filter are analyzed and measured. In this paper, it is confirmed that the linearity of the active RC filter is dependent on the performance of the OPAMP. Based on these results, it shows that, to improve the linearity of the filter, the transfer gain of the filter should be made lower, linear gain properties of the OPAMP higher, 3rd-harmonics of the OPAMP smaller, and the OPAMP bandwidth wider.

Acknowledgement

The authors are grateful for the support of IDEC and BK21 program.

References

- [1] Hollman, T., Lindfors, S., Lansirinne, M., Jussila, J., and Halonen, K.A.I., "A 2.7-V CMOS dual-mode baseband filter for PDC and WCDMA," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1148 - 1153, July 2001.
- [2] Groenewold, G., "Optimal dynamic range integrators," *Circuits and Systems I: Fundamental Theory and Applications*, *IEEE Transactions on*, vol. 39, pp. 614 - 627, Aug. 1992.
- [3] Yoshizawa, A. and Tsvividis, Y.P., "Anti-blocker design techniques for MOSFET-C filters for direct conversion receivers," *Solid-State Circuits, IEEE Journal of*, vol. 37, pp. 357 - 364, Mar. 2002.
- [4] Tsvividis, Y.P., "Continuous-time filters in telecommunication chips," *communications Magazine, IEEE*, vol. 39, pp. 132 - 137, Apr. 2001.
- [5] Willy Sansen, "Distortion in Elementary Transistor Circuits," *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, pp. 315-325, Mar. 1999.
- [6] Piet Wambacq and Willy, Sansen, *Distortion Analysis of Analog Integrated Circuit*. The Netherlands: Kluwer Academic Publishers, 2001.
- [7] H. Bachler and W. Guggenbuhl, "Noise analysis and comparison of second-order networks containing a single amplifier," *IEEE Trans. on Circuits and Systems*, vol. 27, pp. 85-91, Feb. 1980.
- [8] P. Bowron and K. A. Mezher, "Noise analysis of second-order analogue active filter," *IEE Proc. Circuits, Devices and Systems*, vol. 141, pp. 350-356, Oct. 1994.
- [9] Lah, L., Choma, J., and Jr. Draper, J., "A continuous-time common-mode feedback circuit (CMFB) for high-impedance current-mode applications," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 47, pp. 363 - 369, Apr. 2000.