Current Status of Millimeter-Wave Transistor Technology

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Abstract: The current status of millimeter-wave transistor technology is reviewed. We mainly present recent results for InP HBT and InP HEMT, including the current status of POSTECH's InP-based HBT. Si-based high speed transistors such as SiGe HBT and RF CMOS are also discussed. Due to the recent progress of the scaling on HBTs to submicron dimensions, InP HBTs deliver superior high frequency performances to any other transistor technologies.

I. Introduction

In recent years, the millimeter-wave band has gained increased interest for system applications due to its wide frequency spectrum, high data rate, and compact sized hardware solutions. Application areas based on the advanced transistor technologies are extended to commercial fields including fiber-optic network, mobile wide-band cellular systems, fixed wireless broad-band access systems, wireless local area networks, and wireless vehicle and traffic information systems[1,2].

The majority of millimeter-wave circuits have been implemented in InP-based or GaAs-based transistor technologies. HEMTs have historically been used for high-speed applications because of their relatively high current gain cut-off frequency (f_T) and maximum oscillation frequency (f_{max}). However, in the recent year, InP-based HBTs deliver superior performance to any other transistors. Highly scaled Si-based transistors such as SiGe HBT and CMOS will challenge InP-based transistors for millimeter-wave markets, accompanied by the ability to integrate a high degree of functionality on a single chip[3]. This paper is aimed at addressing the recent progress of high speed device technologies for millimeter-wave applications.

II. Current Status and Technology Trends of Millimeter-Wave Transistors

The ever-increasing demand for faster devices pushes the operation frequency of transistor steadily in higher frequencies. In 1990's, InP based PHEMT is the device of the choice for millimeter-wave operation. The key parameters for the high frequency operation are the reduced short channel effect for nano-scale gate by maintaining a large aspect ratio of gate and modulation charge and the suppression of the parasitic resistances and capacitances. A 25nm gate InGaAs/InAlAs PHEMT demonstrates f_T of 562GHz by Fujitsu group [4]. Although the f_T is very high, f_{max} is rather moderate, about 330GHz, due to the large output conductance related to a small aspect ratio of 1.6. The high f_{max} has been demonstrated from a 100nm gate PHEMT. f_{max} is about 600GHz but with moderate f_T of 160GHz[5]. These data clearly indicate that we need a new material structure with thinner channel to maintain a large aspect ratio for nano-scale gates. A 60 nm gate metamorphic HEMT presents a good performance with f_T of 260 GHz and f_{max} of 490 GHz, which is comparable to lattice matched InP-based HEMT with the cost advantage of a GaAs substrate [6].

Significant progress has been made for InP based HBT in 2000's. Sub-micron scaling techniques of HBTs have been developed. As the devices are scaled down, the base and emitter parasitic resistances become important and should be minimized and the collector capacitance has been reduced using the various novel techniques. The epi-layer structure is further refined including compositional and/or doping graded layer for field-assisted fast transport. There are trade-offs between base transit time/base resistance and collector transit time and collector capacitance. Rodwell group in UCSB demonstrated an InP based SHBT with f_{max} of 1.08 THz and f_T of 204GHz [10]. They build a 0.4x6um^2 InAlAs/InGaAs SHBT using transferred-substrate technique. They could minimize the collector capacitance using their structure. It is the highest f_{max} ever reported from any transistors. But the process is very complicated and hard to be a manufacturable technique. In POSTECH, we have developed our own process technique for reduced collector capacitance using novel undercut technique and emitter resistance by emitter metal widening and thick air-bridge processes [11]. Recently, a 0.25um InP/InGaAs SHBT delivers f_{max} of about 600GHz with f_T of 200GHz. It is the highest f_{max} from the standard processed HBTs. M. Feng in UIUC group scales vertically the base and collector layers for reduced transit time using 25nm base and 75nm collector layers [8]. 0.35x12um^2 InP/InGaAs SHBT delivers a f_T of 506GHz with f_{max} of 219GHz. SHBT has a higher speed but breakdown voltage of InGaAs layer is lower, and DHBT using InP collector layer has been studied extensively. The best performances among InP DHBTs are f_{max} of 450GHz with f_T of 282GHz and f_T of 370GHz with f_{max} of 375GHz [15].

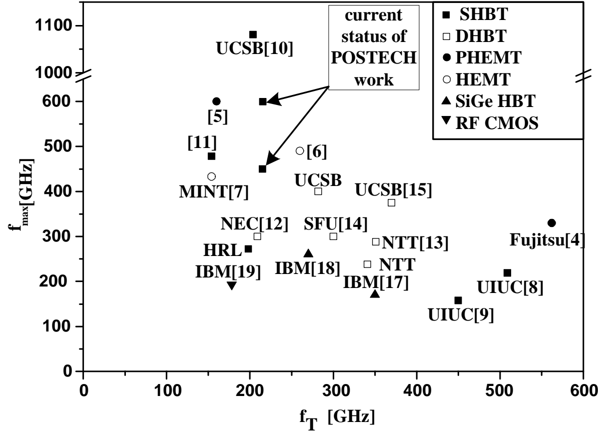

Fig. 1. Comparison of the f_T and f_{max} for the reported high speed transistors

Si based transistors have been progressed very rapidly. IBM group pushes SiGe HBT's well into millimeter wave region. The main trust is the well developed process including self-align using double poly-Si and sub-micron scaling. A 0.12x2.5um^2 HBT delivers a f_T of 350GHz with f_{max} of 170GHz. Simultaneous optimization for f_T and f_{max} results in values of 270 and 260GHz, respectively [17]. SiGe HBT is an excellent high speed device but poor than InP HBT due to the poor transport property and conductive substrate issues. Nano-scaling MOSFET becomes another candidate for a low cost mm-wave device. A combination of optimized device design and aggressive gate oxide scaling has been applied to get mm-band transistors. A 39nm NMOS delivers f_{max} of 193 and f_T of 178GHz [19].

These high frequency device technologies are compared in Fig. 1. They are in various development stages and will be viable commercial products as the system requirements grow in the near future.

III. High Speed Device Structure Issues and Speed Optimization

In this section, structural issues and speed optimization of HEMTs, HBTs, and Si-based transistors are discussed.

A. InP-based PHEMTs

The upper frequency at which the PHEMT operates is limited by the electron transit time from the source to the drain. Therefore, to increase the operation frequency, it is necessary to reduce the gate length. However, as the gate length approaches deep sub-micron, it is necessary to reduce the other parasitic delays in the device and take into account short channel effects to maintain the high frequency performance of the HEMT.

Several important factors contribute to the high speed operation of HEMTs. Firstly, the design and growth of pseudomorphic epi-structure are the key factor for the success of getting the good devices. The channel structures can achieve higher electron mobility, yielding higher g_m. Together with short gate length, novel gate-recess technique such as two-step gate-recess is also important, which can suppress the extension of the effective gate length due to the higher electron density in the side-etched region[23]. Fig. 2 shows a typical PHEMT.

As the gate length is reduced, the distance between the gate and channel (2DEG) has to be reduced so that the channel aspect ratio of the device is maintained high. f_{max} is defined as follows[24]:

$$f_{\max} = \frac{f_T}{\sqrt{4 g_{ds}\left(R_{in} + \dfrac{R_s + R_g}{1+g_m R_s}\right) + \dfrac{4}{5}\dfrac{C_{gd}}{C_{gs}}\left(1+\dfrac{2.5C_{gd}}{C_{gs}}\right)\left(1+g_m R_s\right)^2}}$$

In order to improve the f_{max}, output conductance (g_{ds}), the crucial parameter, should be reduced by the high channel aspect ratio, which suppresses the short channel effect. Reduction of R_g and R_s depends mainly on the process technology such as T-shaped gate electrode and recess structure. Therefore, the high f_{max} of PHEMTs can be achieved mainly by vertical scaling suitable to the short gate.

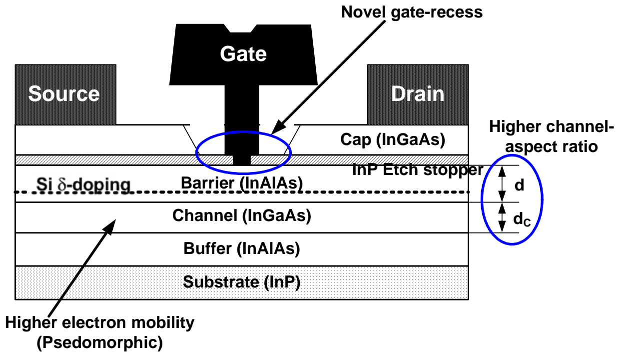

Fig. 2. Schematic of high speed HEMT (InP PHEMT)

The expression of f_T, which includes the effects of parasitics, is given below:

$$f_T = \frac{g_m/2\pi}{\left[C_{gs}+C_{gd}\right]\left[1+(R_s+R_g)g_{ds}\right]+C_{gd}g_m(R_s+R_d)}$$

In order to increase f_T, it is clear from above equation that it is also necessary to reduce the source and drain resistances as well as shorter gate length. This can be achieved by a self-aligned gate, which reduces the gate-source and gate-drain spacings. Thus, the high f_T of HEMTs can be obtained by lateral scaling. The suppression of short channel effect by higher channel aspect ratio is also useful.

B. InP-based HBTs

Two measures of the high frequency performance of HBT are given as:

$$\frac{1}{2\pi f_T} = \tau_B + \tau_C + \frac{C_{JE} + C_{BC}}{g_m} + C_{BC}(R_E + R_C)$$

$$f_{\max} = \sqrt{\frac{f_T}{8\pi R_B C_{BC}}}$$

The schematic cross-section and high speed optimization issues are depicted in Fig. 3. To achieve high f_T and f_{max}, the HBT design must: achieve low base and collector transit times for high f_T, balance the reduction in collector transit time with the reduction in breakdown voltage(BV_{CEO}) and an increase in C_{BC}, minimize the base resistance(R_B), minimize the extrinsic C_{BC}, and minimize the emitter contact resistance (R_E).

The general approach to improve the f_T is to use thin base/collector layer design [8, 9]. However, the approach can only be used at the expense of the reduced f_{max} due to the increased R_B and C_{BC}, and may not be suitable for such applications demanding both high f_T and f_{max}.

In this point of view, bandgap engineering (or grading scheme) is another important issue for higher f_T, especially for DHBTs. So far various design schemes have been proposed to avoid the current blocking effect, such as those using a composite collector[21], pn-pair doping [22], InGaAsP graded layers[13], optimization of ballistic carrier transport, and staggered band lineup of InP/GaAsSb/InP[14]. Compositional and/or doping graded base layer is also helpful for reducing base transit time.

The emitter resistance and inductance should be minimized to reduce the parasitic delay. The base resistance is the most important issue for higher f_{max} and has three components: contact resistance, gap resistance, and intrinsic spread resistance. Minimum base resistance can be achieved by highly doped base layer, scaling of emitter width, self-aligned, and optimization of base ohmic contact. The C_{BC} reduction, independent of base contact width, is compulsory technique for high speed HBTs for both high f_T and f_{max}[10, 11].

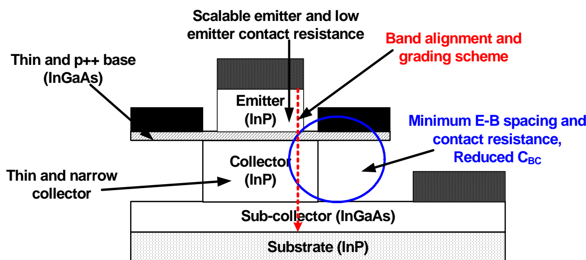

Fig. 3. Schematic of high speed HBT (InP DHBT)

Fig. 4 shows several SEM photographs of the major features of POSTECH's InP-based HBT. We have developed our own process technique for reduced C_{BC} using novel undercut and base-pad isolation techniques, which allow maintaining a low base contact resistance and thick base air-bridge. We have also employed emitter metal widening using polyimide for reducing emitter resistance and thick emitter air-bridge for reduce thermal resistance and inductance. A 0.25um InP/InGaAs SHBT delivers f_{max} of about 600 GHz with f_T of about 200 GHz. It is the highest f_{max} from the standard mesa structured HBTs.

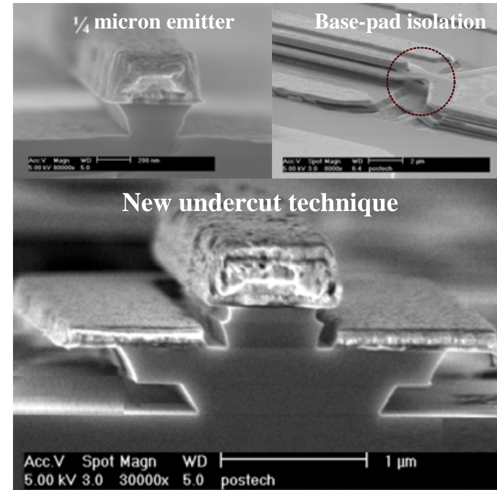

Fig. 4. Important features of POSTECH's InP HBT

C. Si-based Transistors

SiGe HBT can operate at millimeter-wave band with an excellent phase noise performance. Fig. 5 shows the schematic of a modern high speed SiGe HBT. Deep trenches combined with shallow ones provide device isolation and reduce C_{BC}, while a buried sub-collector layer and an n- epitaxial layer with selectively implanted collector form the collector region. A SiGe:C base layer is heavily doped with well confined profile and a boron doped raised extrinsic base is self-aligned to in-situ phosphorus doped emitter for reduced base and emitter resistances.

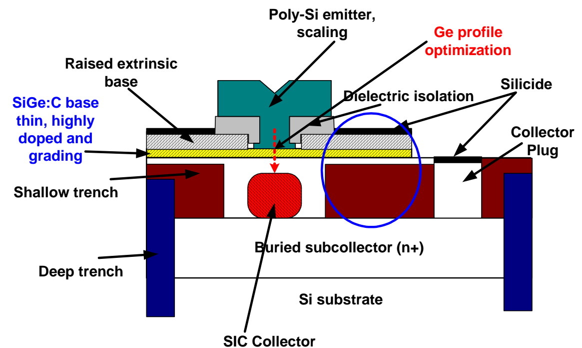

Fig. 5. Schematic of high speed SiGe HBT

Higher f_T and f_{max} can be achieved by the similar optimization of III-V HBTs. Generally, C_{BC} is minimized through careful SIC(Selectively Implanted Collector) design, minimizing lateral dimensions, and

focusing on the emitter perimeter and pedestal regions, which contribute the bulk of this capacitance. While R_B minimization benefits from emitter width reduction, extrinsic portion of the base can be reduced by increasing doping level in this region and by narrowing the gap of the extrinsic base from the emitter. The Ge-profile optimization of SiGe base layer is a key factor for the reduction of transit time and current blocking effect.

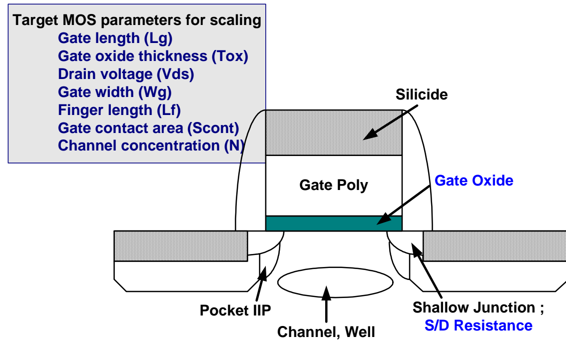

Fig. 6. The schematic of RF CMOS and scaling parameters

Nano-scaling MOSFET becomes another candidate for a low cost millimeter-wave device. One of the biggest advantages of the Si-based transistor technology is the potential to use the high integration capability of Si technology. The optimization of high speed CMOS is quite similar to that of HEMTs. The f_T mainly depends on lateral scaling of CMOS including gate length and source/drain resistance, etc. The silicide and metal gates with low gate sheet resistances are also introduced for higher f_{max}. An optimized pocket IIP is also employed to reduce the short channel effect as well as thinner gate-channel distance.

IV. SUMMARY

In recent years, aggressive scaling and improved process technique advances the device technology well into the millimeter-wave region. The high speed HEMT and CMOS are obtained by lateral scaling for shorter gate lengths combined with vertical scaling for large aspect ratio and progressive improvements in source/drain resistances. The best performance has been achieved from nano-scale FETs. The high speed HBTs are obtained by vertical scaling (thinner base and collector layers) combined with lateral scaling (narrower collector and emitter junctions), increased current density, and progressive improvements in emitter and base resistances. For the current HBT technology, submicron devices deliver the best performance. The accumulated performance data clearly show that HBT is better for high speed operation than FETs and InP is the best material for the purpose. Highly scaled InP-based HBTs with submicron emitter,0.2~0.4um range, are superior to any other transistors and are now being used for commercial millimeter-wave applications.

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