Realization of High-Speed InP SHBTs using Novel but Simple Techniques for Parasitic Reduction

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Abstract

We have developed novel but simple process techniques for high speed InP SHBTs. For parasitic reduction, the collector layer is undercut using etch-stop layer, base pad is isolated, and emitter metal is widened using thick plated gold. Typical common emitter dc current gain (β) and BV_{CEO} are about 25 and above 3.5 V, respectively at a collector current density of 1×10^5 A/cm^2. Maximum extrapolated f_{max} of 450 GHz with f_T of 215 GHz is achieved for 0.5×8 μm^2 emitter area devices at I_C = 17 mA and V_{CE} = 1.5 V. These data clearly show that the optimized conventional process can offer the direct implementation of InP HBT for high-speed electronic circuit fabrication.

I. Introduction

InP-based HBT has shown a great potential for high-speed digital, microwave, and opto-electronic applications because of their intrinsic advantages over other competing materials for high speed HBT implementation. In the HBT, reduction of base collector capacitance (C_{bc}) is very important for high speed operation. A large part of C_{bc} is originated from the extrinsic base area in the mesa structured HBT. The extrinsic C_{bc} can be reduced by ion implantation isolation. But a deep isolation is required for small C_{bc} because of the large dielectric constant of the material [1]. On the other hand, simple collector undercut is the most widely used technique to reduce C_{bc} of InP Double-HBTs (DHBTs) due to the selective etching nature [2]- [4] since the air filling of the gap between the base layer underneath the base contacts and the subcollector has the lowest relative dielectric constant of unity. In the case of Single-HBTs (SHBTs), however, the base layer is also etched during the undercut process because the selective etch cannot be employed. Several undercut techniques have been employed to reduce C_{bc} of SHBTs [5] [6] but yields are usually bad due to the complicated processes, especially for scaled-down devices.

This paper reports on the development of novel but simple process techniques for reduction of not only C_{bc} but also other parasitics for realization of high speed InP SHBTs. To reduce C_{bc}, collector layer is undercut using etch-stop layer in the SHBT, similar to the undercut process in the DHBT and a base-pad-isolation structure is also utilized, which can eliminate the capacitance at the base-pad area. The base resistance (R_b) is minimized by maximizing the base doping (8.0×10^{19} cm^{-3}), placing the base ohmic contact as close to the emitter junction as possible and optimizing the base contact resistivity (ρ_{BC}). Additionally, the emitter parasitic resistance and inductance are minimized by using emitter metal widening and air-bridge structures with plated thick gold. These optimized conventional processes deliver extremely high speed InP SHBTs.

II. Device Structure and Fabrication

TABLE 1
EPITAXIAL LAYER STRUCTURE OF FABRICATED HBTs

Layer	Composition	Doping (cm^{-3})	Thickness (Å)
Emitter-cap	In(x)GaAs : x=0.53	>1×10^{19}	1000
	In(x)Ga(y)Al(1-x-y)As x=0.53, y=0.19~0.47	>1×10^{19}	200
	InP	1×10^{19}	900
Emitter	InP	7×10^{17}	700
Spacer	InGaAs : x=0.46	Undoped	20
Base	In(x)GaAs x=0.46~0.53	8×10^{19}	400
Collector	InGaAs : x=0.53	2×10^{16}	1000
Insertion	InP	2×10^{16}	50
Collector	InGaAs : x=0.53	2×10^{16}	1500
Etch-stop	InP	>1×10^{19}	100
Subcollector	InGaAs : x=0.53	>1×10^{19}	6000

The epitaxial layer of the HBTs is grown by Solid Source Molecular Beam Epitaxy on a Fe-doped semi-insulating (100) InP substrate. The layer structure includes, from the top, InGaAs emitter contact layer, InGaAlAs graded layer, InP emitter layer (700 Å, Si-doped to 7.0×10^{17} cm^{-3}), InGaAs base layer with Indium mole fraction graded from of 0.46 to 0.53 (400 Å, C-doped to 8.0×10^{19} cm^{-3} with 20 Å spacer), InGaAs collector layer (2500 Å, Si-doped to 2.0×10^{16} cm^{-3}), and InGaAs subcollector layer(6000 Å, Si-doped to 1.0×10^{19} cm^{-3}). The details are outlined in Table 1.

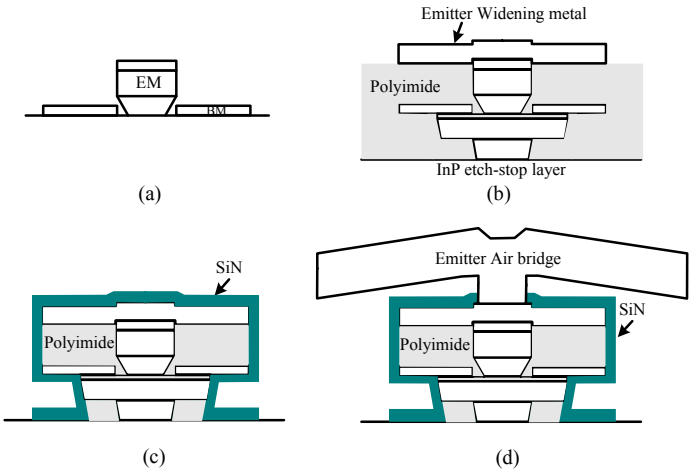

Fig. 1. Process flow (a) Self-aligned base metal, (b) Emitter metal widening, (c) SiN passivation, (d) Emitter air bridge

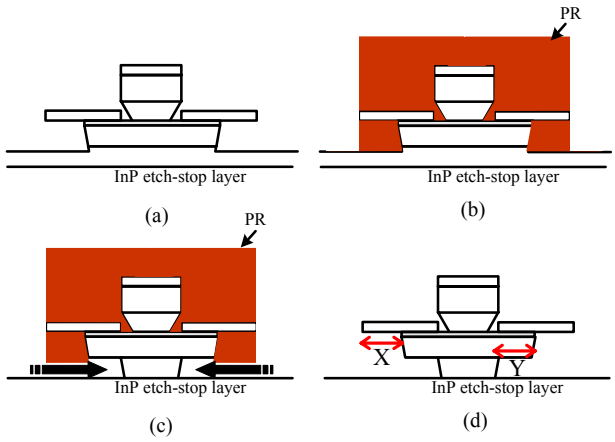

Fig. 2. New collector undercut process flow (a) 1st BC etching, (b) PR protection, (c) 2nd BC etching (d) PR strip

The conduction band discontinuity (ΔE_C) between InGaAs emitter-cap layer and InP emitter layer is suppressed by using the compositional graded InGaAlAs layer. Also, the potential drop across the Indium mole fraction graded base is 40 meV, which corresponds to an electric field intensity of 10 kV/cm. The calculated base transit time (τ_b) is reduced by about 40 % [7]. Lastly, an important addition is two InP etch-stop layers for undercut process in SHBTs. Due to the etch-stop layers, the undercut process similar to the DHBT can be employed without having any base layer etch problem. Therefore, the base contact resistance is maintained low.

Fabrication started with the evaporation of Ti/Pt/Au emitter contact metals having 0.8 µm width. Emitter etch, which is one of the most delicate steps, is carried out by selective etch of citric-based and subsequent hydrochloric-based wet processes, and the emitter is slightly undercut. After the emitter etch, a self-aligned Pt/Ti/Pt/Au base metal is evaporated [Fig. 1(a)]. The emitter is protected by photo-resist using base contact mask and the base and collector layers are then etched with a citric-based etchant. In this etching process, the collector undercut process is performed. Next, Polyimide is coated, and then flatly etched without mask using O_2 RIE until the emitter metal is exposed. Next, a Ti/Au emitter widening metal is evaporated [Fig. 1(b)], and second polyimide etch is performed until the epilayer is exposed. Next, the SiN is deposited. The SiN is mask etched and the residual polyimide is removed by ashering [Fig. 1(c)]. The subcollector is etched for device isolation. In this etching process, the active base area and the base area for interconnecting base pad are isolated. Next, Ti/Pt/Au collector metal and pad metal are evaporated. Lastly, Au air-bridge formation is followed [Fig. 1(d)] [8].

Fig. 2 and 3 show the new undercut process and the base-pad isolation structure for minimizing R_b and C_{bc}. In Fig. 2(d), X is determined by trade-off of R_b and C_{bc} and Y is adjusted to

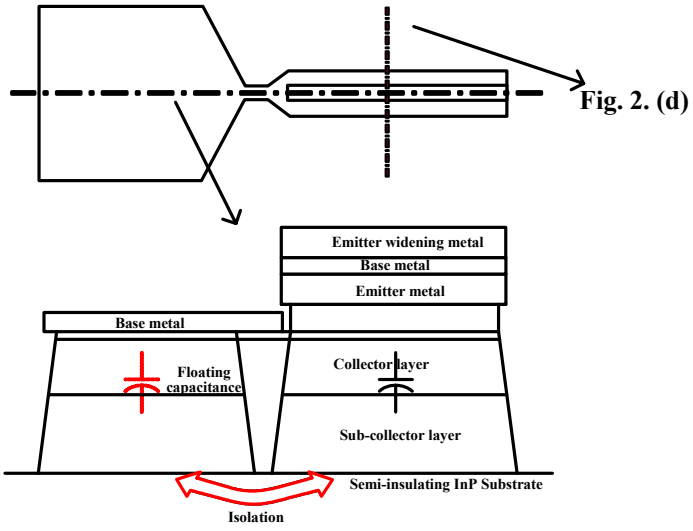

Fig. 3. Base pad isolation structure (vertical section)

have similar widths for emitter-base and base-collector junctions. SEM pictures of the fabricated HBT are shown in Fig. 4. Also base resistance (R_b) is minimized by maximizing the base doping (8.0×10^{19} cm^{-3}), placing the base ohmic contact as close to the emitter junction as possible and optimizing the base contact resistivity. Additionally, the emitter parasitic resistance and inductance are minimized by using emitter metal widening and air bridge structure using plated thick gold. For high speed InP HBTs, the emitter and base metal widths are 0.8 µm (effectively 0.5 µm) and 1 µm, respectively. The base-to-emitter spacing measured from SEM picture is about 0.15 µm.

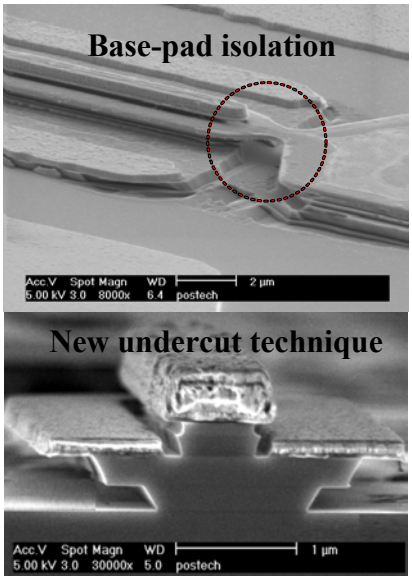

Fig. 4. SEM pictures for the fabricated HBT

III. Device Measurement Results

A. DC performance

I-V curves of the HBT with 0.5 × 8 μm^2 emitter area are measured and depicted in Fig. 5. As shown, the common-emitter dc current gain (β) and breakdown voltage of the fabricated HBTs are about 25 and above 3.5 V, respectively at a collector current density of 1 × 10^5 A/cm^2. Breakdown voltage of the HBTs at an open base, BV_{CEO}, is very high, above 5 V. The base sheet resistance (R_{SB}) of 472 Ω/□ and specific contact resistivity (ρ_{BC}) of 1.65 × 10^{-7} Ω•cm^2 are measured using transmission line measurement (TLM). The transfer length L_T, expressed as $(\rho_{BC}/R_{SB})^{1/2}$, is 0.19 μm and the base contact resistance is maintained low.

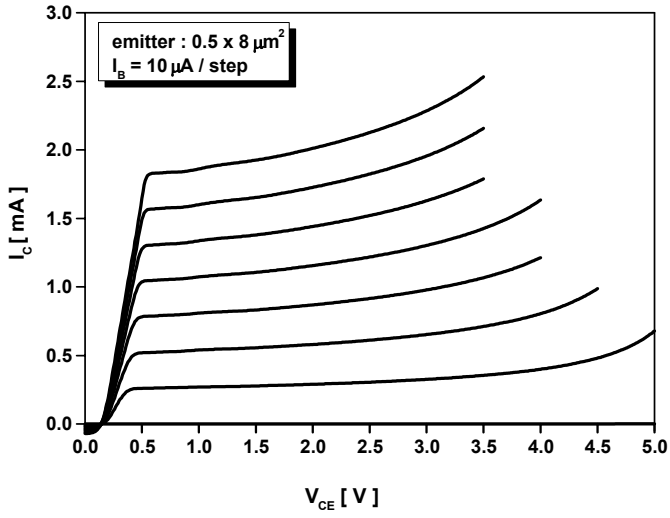

Fig. 5. Common emitter I_C-V_{CE} characteristics of the fabricated HBT with a 0.5 × 8 μm^2 emitter area

B. Microwave performance

The microwave performances of the HBT are characterized by on-wafer S-parameter measurements from 0.5 to 40 GHz using an Agilent 8510C network analyzer calibrated by thru-reflect-line (TRL) method. Frequency dependence of current gain, Mason's unilateral gain, and maximum stable gain/maximum available gain are shown in Fig. 6. The Mason's unilateral gain curve for pad-deembedding case is smooth and follows the –20 dB/decade frequency dependence very well. The pad-deembedding is inevitable for the characterization of the small size device because the pad parasitic components are not negligible, compared with the intrinsic device components. The estimated f_T and f_{max} of the HBT are 215 GHz and 450 GHz, respectively at I_C = 17 mA and V_{CE} = 1.5 V. Fig. 7 shows the dependence of f_T and f_{max} on collector current density (J_C) at V_{CE} = 1.5 V.

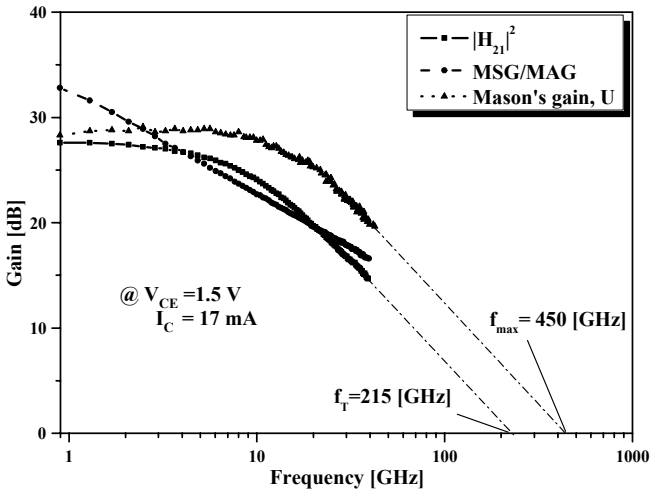

Fig. 6. Frequency dependencies of $|h_{21}|^2$, MSG/MAG, and Mason's gain at I_C = 17 mA and V_{CE} = 1.5 V

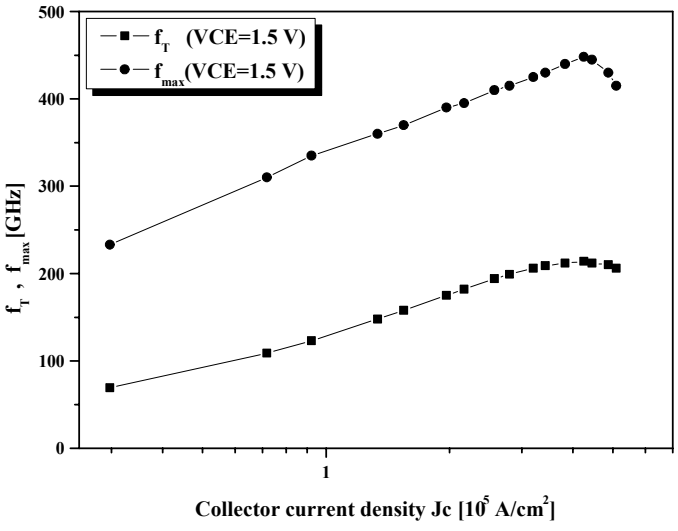

Fig. 7. Dependence of f_T and f_{max} on collector current density of the fabricated HBT with a 0.5 × 8 μm^2 emitter area

TABLE 2

Extracted values of small signal parameters of the fabricated HBT with a 0.5 × 8 μm^2 emitter area at I_C = 17 mA and V_{CE} = 1.5 V

R_b [Ω]	R_π [Ω]	$C_{bc,i}$ [fF]	C_π [pF]	g_m [S]	$\tau_B+\tau_C$ [ps]
10.0	**37.87**	**2.2**	**0.43**	**0.66**	**0.57**

From the measured S-parameters, small-signal model parameters of the device are extracted based on an HBT equivalent hybrid-π model and the extracted values of the key parameters are listed in Table 2. Despite the conventional structure, the time constant $R_bC_{bc,i}$ is very low, about 22.18 fs, due to the base-pad isolation and new collector undercut. These improved structure results in the very high-speed SHBT.

IV. Conclusions

High-speed InP/InGaAs SHBTs are fabricated by using the Postech process. For parasitic reduction, the collector layer is undercut using etch-stop layer, base pad is isolated, and emitter metal is widened using thick plated gold. High frequency performance of f_T = 215 GHz and f_{max} = 450 GHz is obtained from the HBT with a 0.5 × 8 μm^2 emitter area. As the device is scaled down, the device RF performance will be further improved. These data clearly indicate that this conventional process can be a practical technique for implementation of InP HBT to high-speed electronic circuits.

Acknowledgement

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