A Low Phase Noise 2 GHz VCO using 0.13 μm CMOS process

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***Abstract*— A 2 GHz LC VCO with a large improvement in phase noise is designed and implemented in 0.13μm CMOS process. It has phase noise of -100.7 dBc/Hz, -130.6 dBc/Hz, and -140.8 dBc/Hz at 100 kHz, 1 MHz, and 3 MHz offset frequencies from the carrier, respectively. The phase noise reduction of about 10 dB is observed for all controllable voltage range, as compared with a comparable conventional VCO. This VCO consumes 3.29 mA from a 1.8 V supply with the silicon area of 500 μm x 850 μm.**

I. Introduction

In a RF transceiver design, one of the most important and challenging building blocks is a voltage controlled oscillator (VCO). Recently, many reports have presented various circuit techniques for the phase noise optimization, such as harmonic tuning [1], [2] and noise filtering [3]. This paper attempts to minimize the phase noise of a standard differential cross-coupled LC VCO by using such optimization techniques. Our optimized 2 GHz CMOS VCO delivers about 10 dB lower measured phase noise than a standard one for both close-in phase noise at 10 kHz offset and a higher offset phase noise at 3 MHz.

II. VCO Design Techniques

A. Physical Model of the Oscillator Phase Noise

To minimize the phase noise of LC VCO, it must be preceded to understand the phase noise mechanism. The well-known phase noise model for an oscillator is Leeson's proportionality [4].

$$L(\omega_m) \propto \frac{4FkTR}{V_0^2}[\frac{\omega_0}{2Q\omega_m}]^2 \quad (1)$$

However, this proportionality did not provide the exact solution for the phase noise; it is scaled by a noise factor F. Recently, Rael et al. [5] have extracted the F of an LC oscillator from the noise model of mixers with a switched differential pair. The noise factor is given by

$$F = 2 + \frac{8\gamma RI_T}{\pi V_0} + \gamma\frac{8}{9}g_{mbias}R \quad (2)$$

where I_T is the bias current, γ is the channel noise coefficient of the FET, V_0 is the voltage across the resonator, R is the load resistance, and g_{mbias} is the transconductance of the current source FET. This equation describes the thermally induced phase noise arising from the resonator, differential pair and tail bias current.

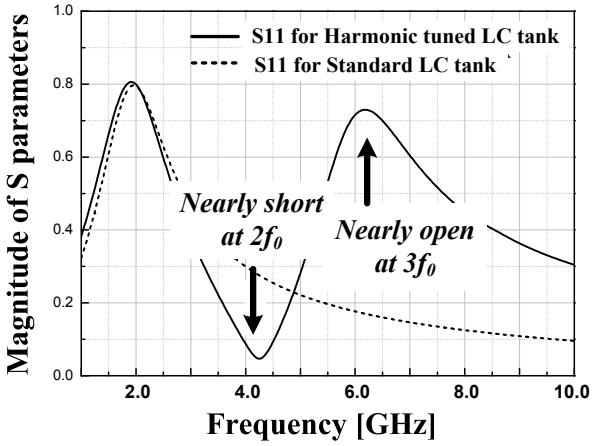

Fig. 1. S11 parameter of harmonic tuned tank

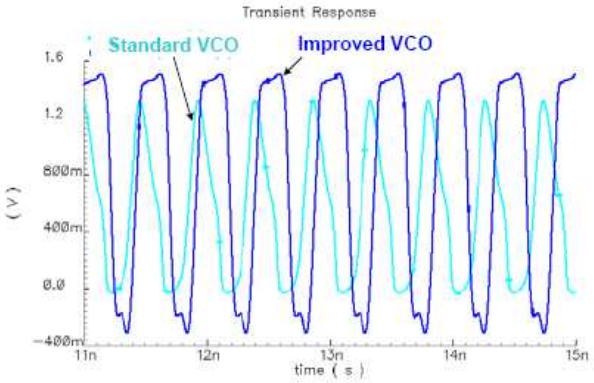

Fig. 2. Time-domain voltage waveforms of the standard and improved VCOs

B. Harmonic Tuning Technique

The harmonic tuning technique can make the slope of the output voltage wave at the zero crossing steeper, increasing effectively the voltage across the resonator, V_0 and reduce the second term of F [1], [2]. Because the required wave consists of the fundamental and its odd harmonics, the resonator

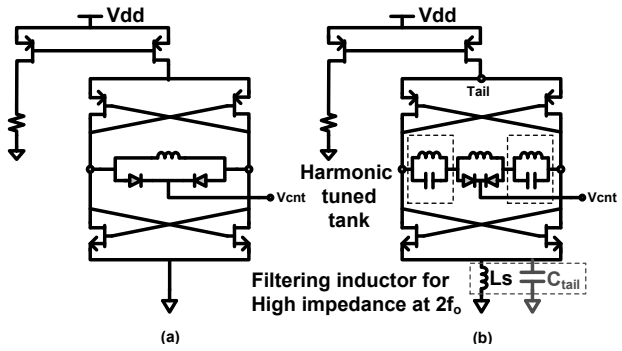

Fig. 3. Schematic of (a) Standard VCO, (b) Optimized VCO

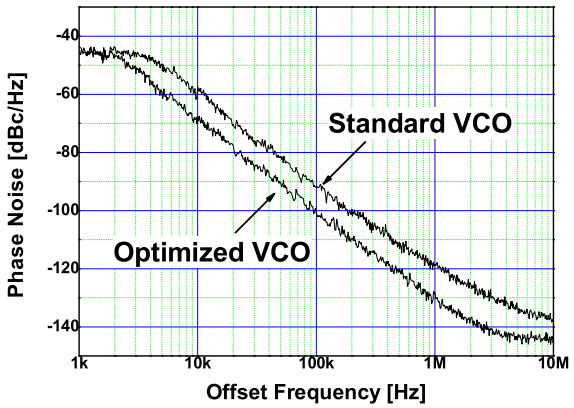

Fig. 4. Measured phase noise at 2 GHz

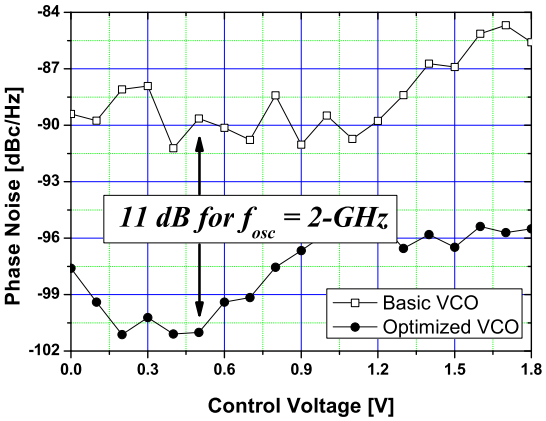

Fig. 5. Control voltage dependent phase noise reduction

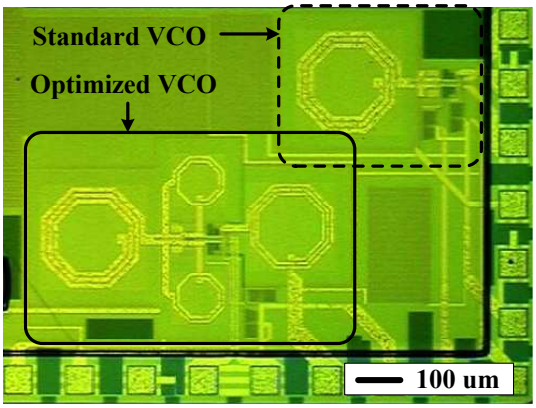

Fig. 6. Microphotograph of the fabricated chip

should be open at the fundamental frequency and the third harmonic and short at the second harmonic. With the harmonic tuning resonator, the oscillator output voltage wave becomes rectangular shape, as shown in Fig. 1, 2. The rectangular switching also reduces the phase noise because the noise from the resonator loss is converted to the phase noise by modulation at the zero crossing instants of the differential switching pair [2].

The amazing effect of this harmonic tuning does not stop there. The harmonic tuned resonator provides short at the second harmonic, so that the tail voltage fluctuation is stabilized. It reduces the tail current noise at the $2nd$ harmonic of the oscillation frequency, which can be down-converted to the phase noise by mixing.

C. Noise Filtering Technique

In the standard top-biased VCO, the common source node of NMOS switching pair is connected to the ground. It forces the one of NMOSs into the triode region as the rising differential oscillation voltage crosses V_t. Thus, the average resonator Q-factor over a full oscillaton cycle is reduced, which degrades the overall phase noise. The filtering by an inductor and the parasitic capacitor at the common source delivers high impedance at $2f_0$, and stops the differential-pair FETs in triode from loading the resonator [3].

III. Measurement Results

The standard and optimized VCOs shown in Fig. 3 are fabricated in $0.13\ \mu m$ CMOS process. They show very similar DC and RF characteristics; both VCOs consume 3.29 mA from the 1.8 V supply and the oscillation power is about -6 dBm. Fig. 4 shows the phase noise measurement results for both VCOs using a HP4352S VCO/PLL signal test system. At the target oscillation frequency of 2 GHz, the phase noise of the optimized oscillator is improved more than 10 dB over a comparable reference one. The VCO achieves phase noise of -100.7 dBc/Hz, -130.6 dBc/Hz, and -140.8 dBc/Hz at 100 kHz, 1 MHz, and 3 MHz offset frequencies from the carrier, respectively. The phase noise reduction is observed over a wide controllable voltage range, which is confirmed in Fig. 5. The microphotograph of the fabricated chip is shown in Fig. 6 with 300 μm x 500 μm and 500 μm x 850 μm areas for the standard and optimized VCO's, respectively. Using the definition of a normalized figure of merit (FOM), we have compared the performance of our VCO with other oscillators:

$$FOM = 10 \cdot log((\frac{f_0}{\Delta f})^2 \cdot \frac{1}{L(\Delta f) \cdot P}) \qquad (3)$$

The FOM of the optimized VCO described above is -188.9dB. Table I compares the FOMs of our VCO with that of the state-

TABLE I

SUMMARY OF THE PERFORMANCE OF THE STATE-OF-THE-ART VCOS

Reference	Technology [μm]	f_0 [GHz]	Phase Noise [dBc/Hz]	Δf [MHz]	Power [mW]	FOM [dB]
N.Fong [6]	0.13 SOI	3.065-5.612	-114.5	1	2	-186.5
T.Y.Kim [7]	0.18	5.13-5.33	-126	1	17.25	-188.2
P.Adreanj [8]	0.35	2.0-2.37	-139	3	12.6	-185.3
This work	0.13	1.911-2.165	-130.6	1	5.92	-188.9

of-the-art VCOs ever reported.

IV. CONCLUSIONS

A 1.8 V, 3.29 mA, 2 GHz CMOS LC VCO using 0.13 μm CMOS process has been presented. The optimized VCO using harmonic tuning resonator and noise filtering circuit achieves a phase noise of -130.6 dBc/Hz at 1 MHz offset. The optimized VCO delivers a phase noise reduction of about 10dB in a wide range of voltage-controllable oscillation frequencies, in comparison to the standard VCO.

ACKNOWLEDGEMENT

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