0.18 μm CMOS Power Amplifier with High Efficiency and Linearity

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***Abstract*— We present a 2.45 GHz CMOS power amplifier (PA) with high efficiency and linearity. A 0.18 μm standard CMOS process with low-loss Cu-metal is employed. With optimun design of the power cell for class AB operation, the PA delivers a 21.1 dBm of output power with 18.9 dB of power gain and 37 % of PAE at P_{1dB}. To effectively linearize the PA, a simple and area effective second harmonic tank is integrated on the chip and optimum biasing point is selected. Linearity measurements from 2-tone test show that IMD3 and IMD5 are maintained under -40 dBc and -50 dBc for an output power backed-off more than 5 dB from P_{1dB}. These results clearly show that CMOS PA is a fully compliant candidate with high speed data communication covering the OFDM systems.**

***Index Terms*— Power amplifier (PA), PAE, Linearity, harmonic termination, g_{m3} cancelation, IMD3, IMD5.**

I. Introduction

Nowadays, CMOS process, which has the high level integration ability and low cost advantage, becomes a technology of choice for single-chip RF transceivers [1]. But the CMOS PA is still a bottle-neck for one-chip solution. Since CMOS process has the inherent resistive substrate coupling and poor device reliability for high voltage operation, WLAN PA, which operates at a comparably low power level and time division duplexing (TDD) mode, has drawn earlier attention. But a tight error vector magnitude (EVM) specification of the high data rate and over 10 dB peak to average power ratio (PAR) of the OFDM signal require extremely high linearity over broad power range below P_{1dB}. These requirements impede getting high power-added efficiency (PAE), lowering the battery life. In this paper, we present a highly linear and efficient CMOS PA targeted for the 2.45 GHz WLAN and introduce the circuit design and linearity enhancement technique.

II. Implementation of CMOS PA

Since the power cell of a linear CMOS PA generally uses NMOS with very large gate width, it consists of sufficiently spaced multiple unit power cells to protect heat-sinking problem. Fig. 1 shows the simplified cross section of a unit power cell. Its gate-width and unit-finger size should be carefully determined considering the thermal generation and non-uniform current distribution by the gate-resistance. As shown, p+ guard-ring surrounds the active part for the substrate contact and device isolation. The substrate contact is connected with source right inside of the unit-cell to minimize the potential difference between the source and substrate. The number of unit cell for the driver and power stage should be determined considering the power-level, gain, matching and linearity, etc. The design procedure of the amplifier has been carried out through the iteration of ADS simulation.

III. Circuit design methodology

In designing a linear PA, a class AB with well-controlled harmonics is a good choice for high efficiency (PAE) and linearity. In this work, the 2-stage PA adopts a class AB operation for both driver and power stage, whose simplified schematic of the circuit is shown in Fig. 2. In normal CMOS operation, the dominant harmonic distortion comes from the non-linear transconductance (g_m) [2] and the corresponding nonlinear current can be expressed as follow.

$$i_{trans} = g_{m1}v_{gs} + g_{m2}v_{gs}^2 + g_{m3}v_{gs}^3 \qquad (1)$$

From (1), the second harmonic generated from the second order term is feed-backed and regenerates the third harmonic. As shown in Fig. 2, the second harmonic is terminated with $2f_o$ resonance circuit composed of area effective MIM capacitor and bonding wire inductor. By placing it at the end of the drain and isolating from the drain matching circuit, the detuning effect of the matching is reduced effectively. The third harmonic generation from the third order term can be avoided by choosing the optimum bias point. Fig. 3 shows the g_m expansion coefficients of the unit power cell of this work and g_{m3} zero-crossing point is marked. By setting the bias around this point, the third harmonic generation from the third order term is significantly reduced. With second harmonic termination at the drain and optimum biasing for the g_m linearization, the linearity of PA is significantly improved.

IV. Experimental results

Fig. 4 shows a photograph of the fabricated CMOS PA whose chip area is 1 μm x 0.74 μm. To verify the chip,

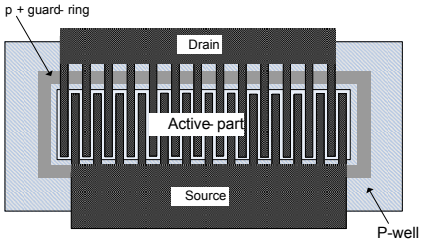

Fig. 1. The basic structure of the unit cell.

an evaluation board is fabricated using FR-4 PCB and the chip is directly mounted on ground plate of the evaluation board. The off-chip matching components are realized on the evaluation board. Because the bonding wire is used for matching and 2fo termination circuit, the tunning of the inductance is done by adjusting the length of the wire based on the data of EM-field simulation. To measure the RF performances, two-tone test has been performed at 2.45 GHz center frequency and 2 MHz tone-spacing. Fig. 5 shows the power measurement results of the amplifier. From the graph, P_{1dB} and power gain of the PA are 21.1 dBm and 18.9 dB, respectively with 37% of PAE at P_{1dB}. To our knowledge, the 37 % PAE at P_{1dB} is the world best record for 0.18 μm standard sigle-ended CMOS PA and it is competitive data to GaAs based PA. Fig. 6 shows that IMD3 and IMD5 of the PA are maintained under -40 dBc and -50 dBc for an output power backed-off more than 5 dB from P_{1dB}. This excellent linearity result verifies that the second harmonic termination at the drain and biasing at g_{m3} zero-crossing point are well suited.

V. Conclusions

A linear PA at 2.45 GHz is implemented using a 0.18-μm CMOS process. Optimum cell design is carried out and PA linearization is adopted with an area-effective second harmonic termination circuit and optimum biasing. The PA carries a P_{1dB} of 21.1 dBm, 18.9 dB of power gain and 37 % of PAE at the point. The PA has a good linearity below -40 dBc for IMD3 and -50 dBc for IMD5 for an output power backed-off more than 5 dB from P_{1dB}. These results clearly show that CMOS power amplifier is a fully compliant candidate with high speed data communication covering OFDM systems.

References

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[2] Sanghoon. Kang, Byunggi Choi, and B. Kim, "Linearity Analysis of CMOS for RF Application," *IEEE Trans. Microwave Theory Tech.*, Vol. 51, No. 3, pp. 972-977, Mar. 2003.

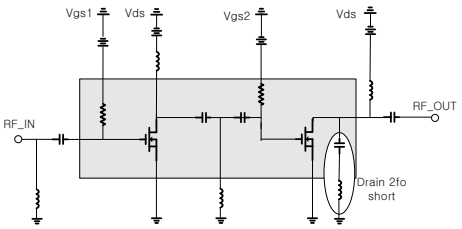

Fig. 2. The simplified schematic of single-ended CMOS PA

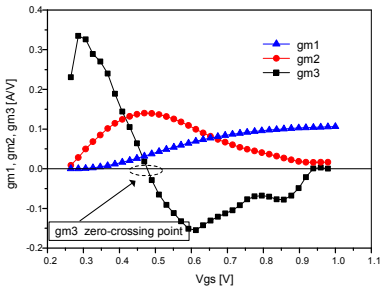

Fig. 3. The non-linear coefficients of g_m.

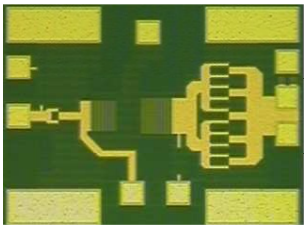

Fig. 4. The photograph of the chip (1 mm x 0.74 mm)

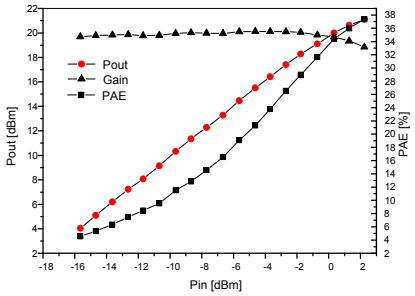

Fig. 5. The measured RF performance of P_{out}, gain and PAE.

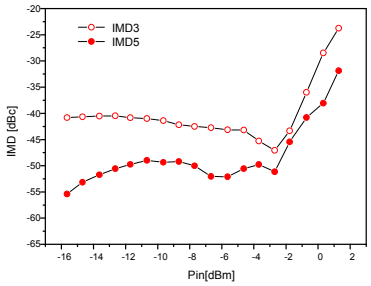

Fig. 6. The measured RF performance of IMD3 and IMD5