A single-chip multi-mode RF front-end circuit and module for W-CDMA, PCS, and GPS applications

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***Abstract*— A single-chip, multi-mode RF front-end circuit for W-CDMA, PCS, and GPS is implemented for direct conversion receiver. Each circuit includes a LNA, Mixer and I/Q distributor. The IIP2 of this module (not in GPS band) is over + 45 dBm with R_{LOAD} tuning circuits. The noise figures are less than 3.5 dB in both W-CDMA and PCS bands, and 3.8 dB in GPS band. The silicon area is 5.06 mm^2 including the PADs. For a small size implementation, the circuit is integrated into a module whose size is 18 mm by 19 mm including SAW filters. The current consumptions from a 2.7 V supply in W-CDMA, PCS, and GPS modes are 37 mA, 37 mA, and 23 mA, respectively.**

I. Introduction

Due to the coexistence of the second and third generation cellular systems, there are increasing demands for multi-mode mobile terminals with small size RF solutions. A multi-mode direct conversion receiver is the best candidate for this trend [1]. The multi-mode RF receiver consists of an RF part and base-band circuits and in this paper, the RF part circuit is reported. The RF front-end circuit is targeted at W-CDMA, PCS and GPS applications and designed differential circuits for each standard specification. Each system demands different bandwidth, linearity and noise figure specifications and it clearly affects the system budget distribution at each block. In this paper, several circuit design techniques are used in each building block to implement the front-end circuits. Fig. 1 shows the PCS/W-CDMA/GPS band receiver block diagram. A low noise amplifier (LNA), frequency down conversion mixer and LO distributor are included in each band. For the IM2 power tuning technique, one of the main issues in the DCR, R-matrix tuning method is employed [2], [3].

In this paper, section II covers issues related to the design of the RF front-end circuit, especially the IIP2 tuning circuit and the measurement results of the each block. The experimental results of the total RF front-end circuit are given in Section III, and the summary is given in Section IV.

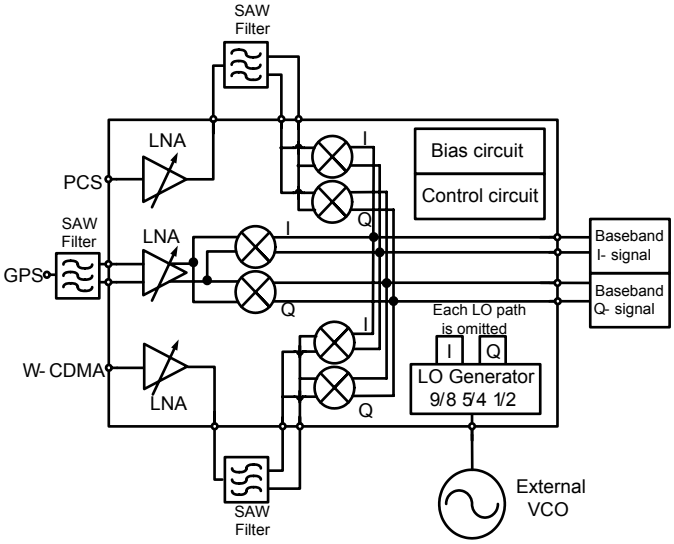

Fig. 1. Multi-band RF front-end block diagram.

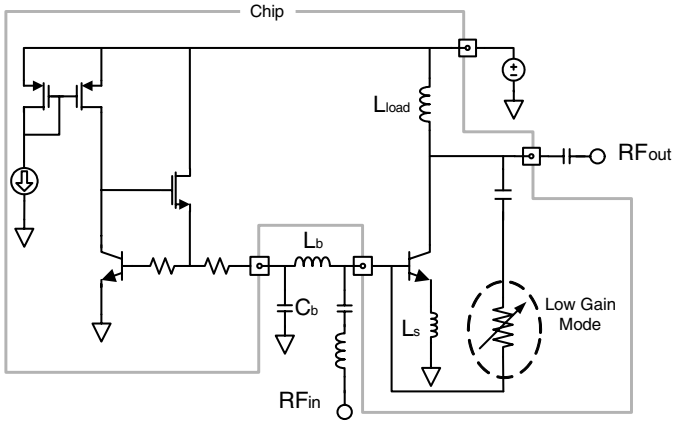

Fig. 2. W-CDMA and PCS band LNAs.

II. Implementation

A. LNAs for W-CDMA and PCS bands

The LNAs simultaneously amplify a small desired signal and adjacent channel signals which may be much larger. Its gain should be sufficient to overcome the noise of the subsequent circuits and noise figure sufficiently low to amplify a minimum signal. Due to the large dynamic range (DR) of input signal, the gain of the LNA should be adjusted to cover the DR without saturating the subsequent circuits at the high input power. Therefore, the LNAs are designed to operate at the three modes of high, medium, and low gains. In a CDMA system, since Rx and Tx part are operated simultaneously, IIP3 of the LNA should be sufficiently high to prevent any distortion by a large leakage power from Tx [4], [5], [6]. Thus, the gains, DR, noise figure (NF), IIP3 are the key specifications of the LNAs. The LNA shown in Fig. 2 uses a single-ended topology to reduce the number of on-chip inductors, NF and power consumption. To reduce the noise

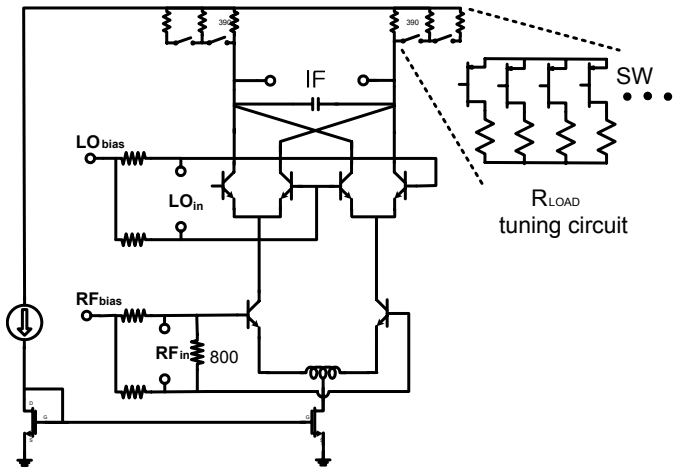

Fig. 3. W-CDMA and PCS band mixers.

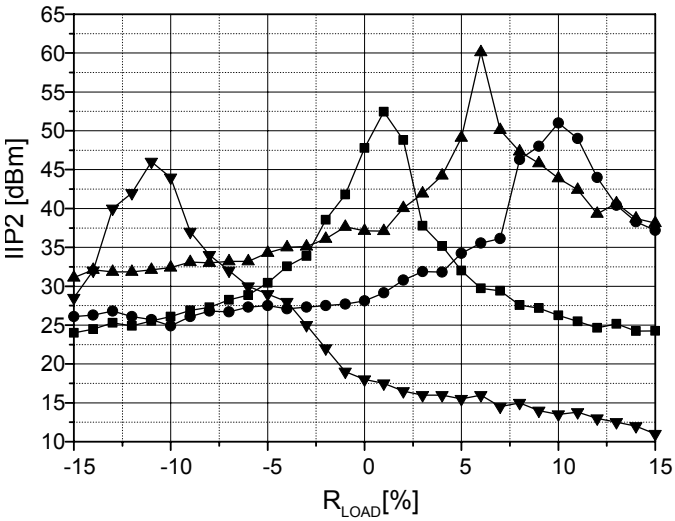

Fig. 4. IIP2 tuning result of total module.

from bias circuits, L_b and C_b are used to filter out the noise. In the high gain mode, a common-emitter HBT is employed for a gain block with the inductive degeneration L_s for linearity. In the low and medium gain modes, the LNA based on MOS attenuator delivers two step losses. These loss values are determined according to each radio specification.

B. PCS & W-CDMA Mixer

The frequency down-conversion mixer, shown in Fig. 3, is based on a double balanced Gilbert-cell using bipolar transistors. An inductive degeneration is used in the transconductor to achieve the linearity (IIP3= +5dBm), noise (DSB NF=15dBm) and impedance matching at the cost of large size. One of the main issues in the DCR is the second-order intermodulation around DC, which can be easily removed by a channel-selection IF SAW filter in the heterodyne architecture in the contrary. The main source of the second harmonic in the DCR is the down-conversion mixer [5], [7], [8]. There are many techniques to improve IIP2 performance such as accurately balanced layout, reducing the nonlinearity of active transconductance and switching cell, and R_{LOAD} trimming [3], [7], [8], [9]. In this paper, R-matrix which is 6-bit binary weighted structure is employed for the effective tuning of the IM2 power. The R-matrix is controlled by a simple 3-bit ADC and the total tuning range is 15% and the minimum tuning resolution is about 1%. The tuning range and resolution are determined by the simulation results based on the known process variations. The mismatch effect of R_{LOAD} by the tuning is so small that it has a negligible effect on the other performance such as gain, NF and IIP3. Fig. 4 shows the IIP2 performance of the total RF front-end circuit according to R_{LOAD} tuning. There is over 15 dBm improvement of the IIP2 performance without any variations on the gain, NF, and IIP3.

C. RF block for GPS band

GPS system is a little different from the other ones. Its input signal is very small, under thermal noise level, but its receiver needs less linearity than other systems [10]. Due to the characteristics, the GPS system can be very compact. The LNA and mixer are designed to differential types, which are resistant to common mode noise. With a SAW filter acting as a passive balun at the RF input port, it is easily matched to the antenna port. The differential type LNA has a sufficient gain and strong immunity to the common mode noise, but it is noisy and unstable. Fig. 5 shows the designed GPS band LNA. Mixer structure is almost identical to the W-CDMA and PCS mixers, but without the R-matrix tuning structure. As mentions earlier, the IIP2 specification of the GPS system is so loose that the IIP2 tuning mechanism is not necessary.

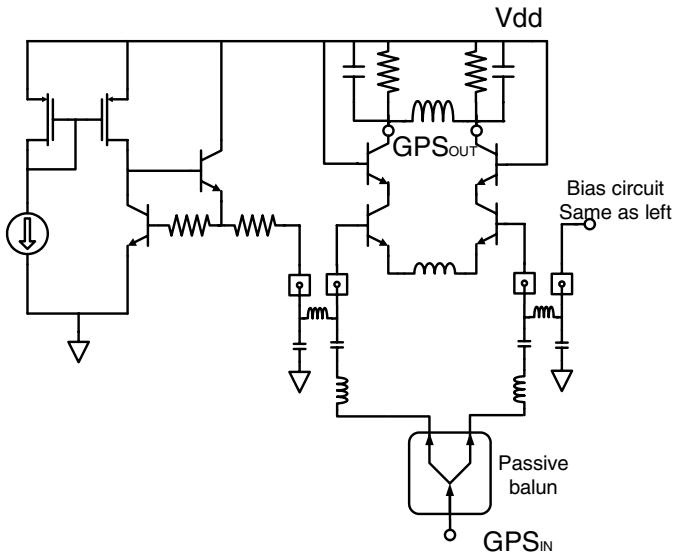

Fig. 5. GPS band LNA.

D. I/Q distributor

In DCR, LO re-radiation degrades the minimum detection signal level and causes the DC-offset through self-mixing [1], [7]. Thus, the LO isolation is very important and it can be easily achieved by using external VCO frequency different from the down conversion mixer LO frequency. Fig. 6 shows the I/Q distributor block diagram for W-CDMA and PCS. The LO frequencies of the mixer are $\frac{5}{4}$, $\frac{9}{8}$, and $\frac{1}{2}$ times by the external VCO frequencies in W-CDMA, PCS, and GPS band, respectively. For a compact design, the W-CDMA and PCS LO distributors use the same circuit except for one block of the divider circuit controlled by switch. The poly phase filter minimizes the amplitude and phase mismatches of I and Q signals. The GPS band I/Q distributor shown in Fig. 7 consists

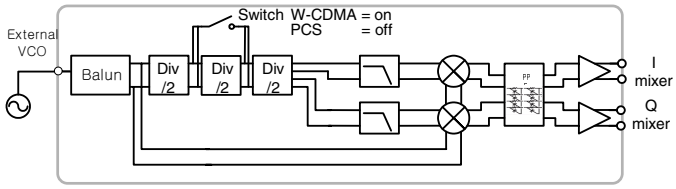

Fig. 6. I/Q distributor block diagram in W-CDMA and PCS bands.

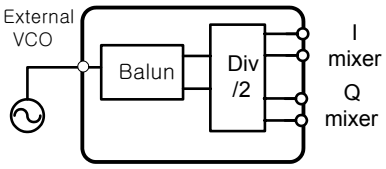

Fig. 7. I/Q distributor block diagram in GPS band.

of the active balun and a divided by 2 circuit. A more detailed frequency scheme is shown in Table I. The key performances of the I/Q distributor are the I/Q balance and the emissions power level of the RF front-end circuit. So, the measurement results of these factors are mentioned in next section.

III. Measurement

The designed RF front-end circuit is fabricated using a 0.35μm single-poly five-metal Bi-CMOS process. Fig. 8 shows a microphotograph of the chip with active area of 5.06 mm^2 including PADs. For the test, the chip is mounted in a MLF44 package, and attached to a PCB module including SAW filter. The RF front-end module is shown in Fig. 9 and its size is 18mm by 19mm. All RF input is single-ended and at the output, a low noise, low distortion differential to single converter (AD8130) converts the differential I and Q mixer output to a single-end signal. There are not any passive components for matching or filter in the test board as shown in Fig. 10. The measured performances of the RF front-end module including the SAW filter with 1dB loss are summarized in Table II. The test results are quite similar to the simulation results of the total block with the I/Q distributor. The input return loss of the RF front-end circuit illustrated in Fig. 11 show a good in-band match for each operation mode. The IIP3 for each mode is measured according to the each standard specification, for example, the IIP3 of a W-CDMA circuit measured at 10M and 20.2M spacing from the carrier frequency. The measured LO leakage at the input port ranges from -80 to -90 dBm. In the quadrature demodulation receiver, the channel balance is very important. Although the DCR does not suffer from image frequency, the errors in the channel amplitude and phase affect the receiver bit-error rate. In all samples, the amplitude

TABLE I
The Frequency Scheme of The I/Q Distributor

Band	parameter	Min. frequency	Max. frequency
PCS Band (9/8)	External VCO	1630	1665
	Rx LO	1840	1870
W - CDMA (5/4)	External VCO	1688	1736
	Rx LO	2110	2170
GPS Band (1/2)	External VCO	3150.84	
	Rx LO	1575.42 (L1 band)	

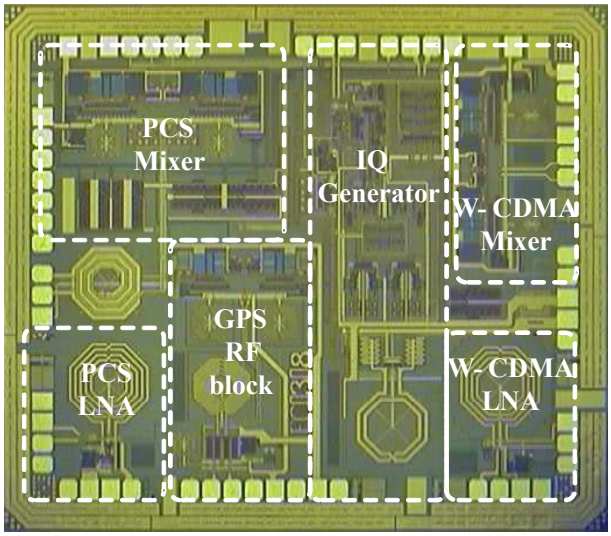

Fig. 8. Chip photograph.

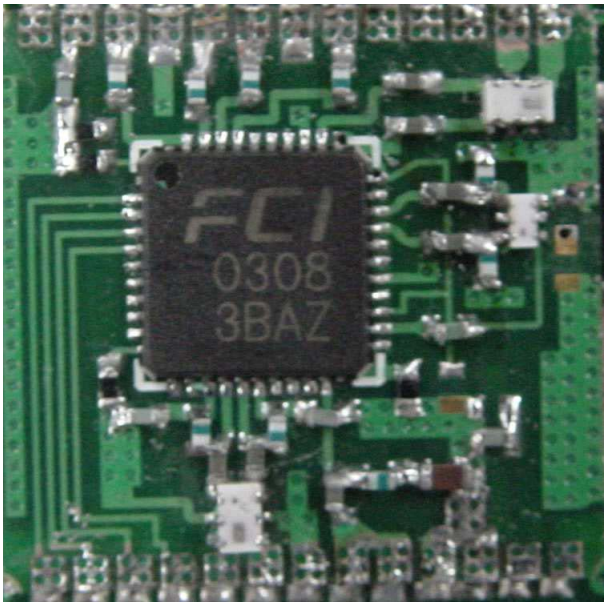

Fig. 9. Module photograph (18 mm*19 mm).

mismatch is less than 0.1 dB and the phase mismatch is less than 5 degrees.

IV. Conclusion

A single-chip multi-mode RF front-end circuit and module for W-CDMA, PCS, and GPS applications are developed. All band performances are suited for the DCR of each wireless system specifications. The LNA, mixer and I/Q distributor for each band are integrated in a 0.35μm single-poly five-metal Bi-CMOS process. For small size RF solution, the multi-band module is integrated in 18 mm by 19 mm size.

V. Acknowledgement

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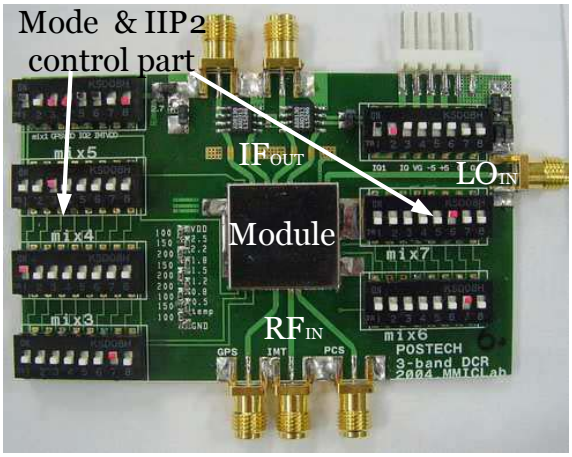

Fig. 10. Test board.

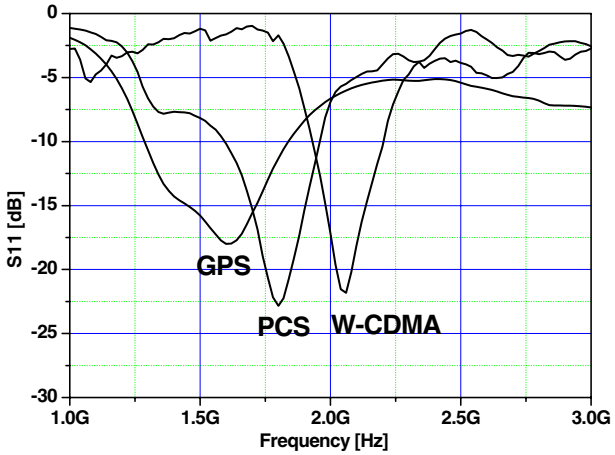

Fig. 11. Input return loss in all bands.

TABLE II
SUMMARIZED PERFORMANCE OF THE RECEIVER

Band	Performance	Results
PCS	Gain [dB]	29..2.7..1.4
	IIP3 [dBm]	-19
	NF [dB]	3
	Current [mA]	43
W-CDMA	Gain [dB]	25..-1..-3.7
	IIP3 [dBm]	-13
	NF [dB]	3.5
	Current [mA]	43
GPS	Gain [dB]	25
	IIP3 [dBm]	-16
	NF [dB]	3.4
	Current [mA]	30
LO leakage power at input port [dBm]		-80~-90
Amplitude[dB] / Phase[degree] mismatch		Under 0.1 / 5

Inc. for their assistance with the chip fabrication and packaging.

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