Advanced Design Methods of Doherty Amplifier for Wide Bandwidth, High Efficiency Base Station Power Amplifiers

Jangheon Kim[1], Jeonghyeon Cha[1], Ildu Kim[1], Sang Yeon Noh[2], Cheon Seok Park[2], and Bumman Kim[1]

[1]Department of Electrical Engineering, Pohang University of Science and Technology,
Gyeongbuk, 790-784, Korea, Tel: +82-54-279-5584, Fax: +82-54-279-8115
E-Mail: rage3k@postech.ac.kr, bmkim@postech.ac.kr
[2]R&D Center, Wave Electronics Co., Ltd., Gyeonggi, 441-814, Korea
Tel: +82-31-269-0010, Fax: +82-31-291-9640

***Abstract*— We have proposed advanced design methods of Doherty amplifier for high efficiency base station power amplifiers with wide bandwidth. First, we develop Doherty amplifier with uneven power drive which is provided more input power to the peaking cell than the carrier cell for full power operation and appropriate load modulation. Second, we optimize the matching circuits of the carrier and peaking cells individually to enhance the linearity and efficiency. Third, we optimize the bias circuit to solve an asymmetric ACLR(Adjacent Channel Leakage Ratio) characteristics for wideband signals such as WCDMA 4FA. The proposed design methods are applied to implement Doherty amplifier using a MRF5P21180. For a 2.14 GHz WCDMA 4FA signal, the amplifier is optimized at 25 W average output power. The drain efficiency and ACLR measured at the power are 33 % and -41 dBc, which represent about 1.3 % and 3 dB improvements, respectively, compared to the Doherty amplifier with even power drive. Additionally, the PEP of the amplifier is about 180 W, while that of the comparable Doherty amplifier is about 165 W. The difference of ACLR with the bias circuit optimization between lower and upper ACLR is reduced below 2 dB at whole average output power range.**

I. Introduction

The current wireless communication systems are progressed to increase the bandwidth and number of carriers for high data rate capabilities. Besides, these systems are intended to minimize the size and the cost. In order to accomplish these requirements, the techniques that can improve the linearity and efficiency of the base station power amplifier and overcome the wideband effect are hot issues in the research community. Doherty amplifier having the high linearity and efficiency across the wideband signal has been studied extensively for the application [1] - [5].

A 2.14 GHz high power Doherty amplifier with wideband and high power has been reported [1] - [4]. The reference [1] delivers excellent efficiency performances, but have a problem to improve the linearity over broad power levels. The problem is caused by the undesired characteristics, such as the memory effect related to wide bandwidth and incomplete modulation due to the under-driving of the peaking amplifier. Usually, in a conventional Doherty amplifier, the load impedances of both cells cannot be fully modulated to the optimum impedance and the peaking cell cannot generate full power because of the class C bias. Thus, the bias adaptation technique is a good approach to solve the problem. However, it increases the complexity due to the external control circuitry and enhances the memory effect [7], [8].

In this paper, we propose advanced design methods to solve the memory effect for wideband signal and the under-modulation problem of the conventional Doherty amplifier. The data described in this paper show clearly that Doherty amplifier based on the proposed methods is far superior to previous Doherty amplifiers.

II. Advanced Design Methods of Doherty Amplifier

The fundamental operation principle of Doherty amplifier has been well described in previous literature [6]. The amplifiers have two cells with identical size devices, matching circuits, and input drives. Because the peaking cell has been biased lower than the carrier cell, the current level of the peaking cell at the maximum input drive can not reach the maximum allowable current level. Thus, the load impedances of both cells can not be fully modulated to the optimized impedance, and they are larger than the optimum values. As a result, the conventional Doherty amplifier has been heavily saturated, and it degrades linearity and produces far less power.

In our earlier works, we have demonstrated that the linearity of the amplifier is improved by IM3 cancellation from the two cells at proper gate biases [5]. For high power and wideband applications, it is difficult to improve the linearity of Doherty amplifier due to the memory effect [1]. Therefore, we propose the following three design methods for wide bandwidth, high linearity, and high power applications;

1) Uneven power drive.
2) Individually optimized matching circuits.
3) The bias circuit optimization.

First, the uneven power drive, applying more power to the peaking cell, can open the peaking cell fully and modulate the optimum load impedances completely. The amplifiers with uneven power drive operate more linearly and produce more power than that with an even drive. Second, in an improper load modulation, the power matching circuits of both cells should be appropriately designed to have low load impedances for better linearity. Due to the lower bias point of the peaking cell, the power matching circuit of the peaking cell should be designed to have lower load impedance than that of the carrier

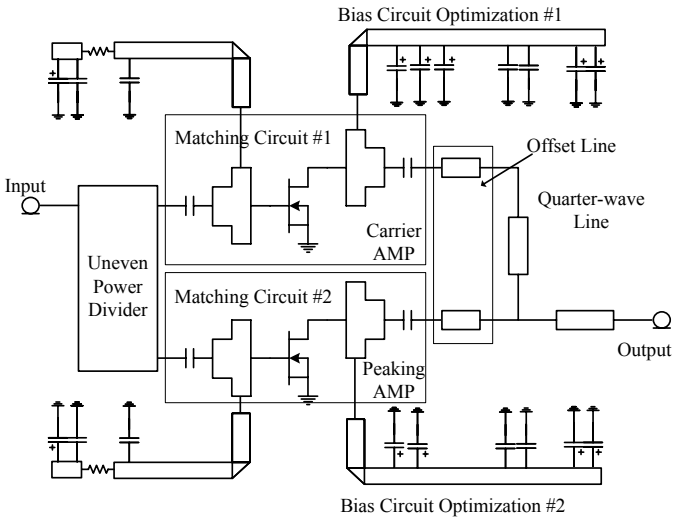

Fig. 1. Schematic diagram of the Doherty amplifier applying the advanced design methods.

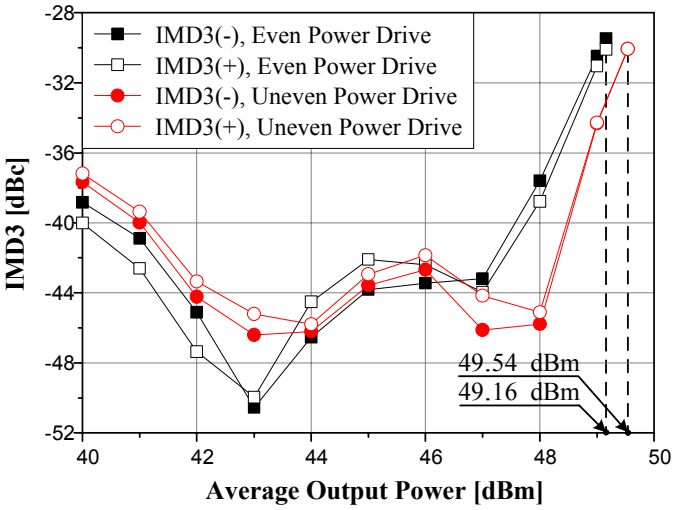

Fig. 2. Two-tone measurement results of Doherty amplifier with even and uneven power drives.

cell. Moreover, the matching circuits of both cells should be individually optimized to induce the IM cancellation over whole power ranges for wideband signals.

Third, the bias circuit should be designed to minimize the memory effect [9] - [11]. The linearizing techniques such as Doherty amplifier and PD, which improve the linearity using the IM cancellation mechanism, are restricted to a low cancellation limit because the memory effect brings about the different low and upper spurious emissions. To reduce the memory effect, the bias circuit is optimized using a quarter-wave bias line and decoupling capacitors for each frequency. The tantalum capacitors are inserted within a quarter-wave bias line for the short at the envelope frequencies. Additionally, the biases of both cells are properly adjusted for maintaining the optimized linearity and efficiency.

III. Implementations and Measurement Results

In the previous section, we have proposed advanced design methods with uneven power drive, individually optimized matching, and bias circuit optimization. A 2.14 GHz Doherty amplifier is implemented using Motorola's MRF5P21180 LDMOSFET. Fig. 1 shows a schematic diagram of the implemented Doherty amplifier applying the advanced methods. The uneven power drive is implemented using an Anaren's 1A1305-5(5 dB directional coupler) which delivers 4 dB more input power to the peaking cell than the carrier cell. The individual matching of the Doherty amplifier is further optimized to achieve high efficiency and linearity at 25 W(44 dBm) average output power. In the experiments, the suitable offset line is 80.4° , and the transformed output impedance is 502 Ω. Quiescent biases for the carrier cell and peaking cell are set to V_C = 3.938 V(1.1 A) and V_P = 1.713 V at V_{DD} = 27 V, respectively. We optimize the bias circuit to minimize the memory effect and improve the linearity and efficiency. For the performance comparison, we fabricate Doherty amplifier with even power drive also, and the amplifier is optimized using the individual matching and bias circuit to get the linearity and efficiency as high as possible.

Fig. 2 shows the measured IMD3 of the Doherty amplifier with even and uneven power drives for a two-tone signal. We measure a peak envelope power(PEP) using two-tone signal

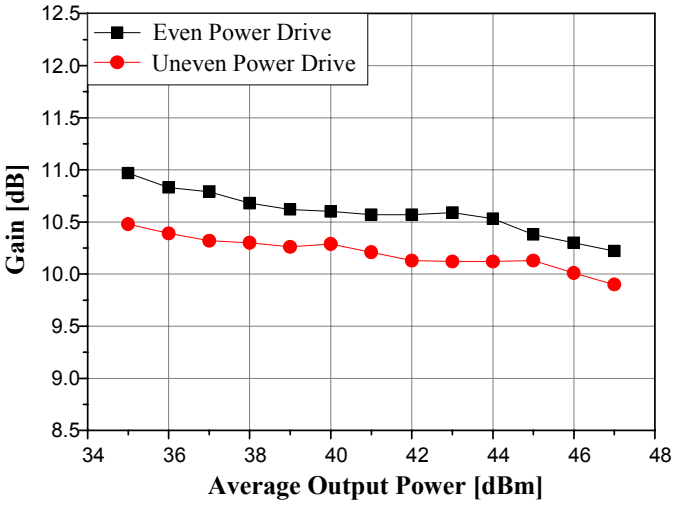

Fig. 3. Measured power gain performance of Doherty amplifier with even and uneven power drives for WCDMA 4FA signal.

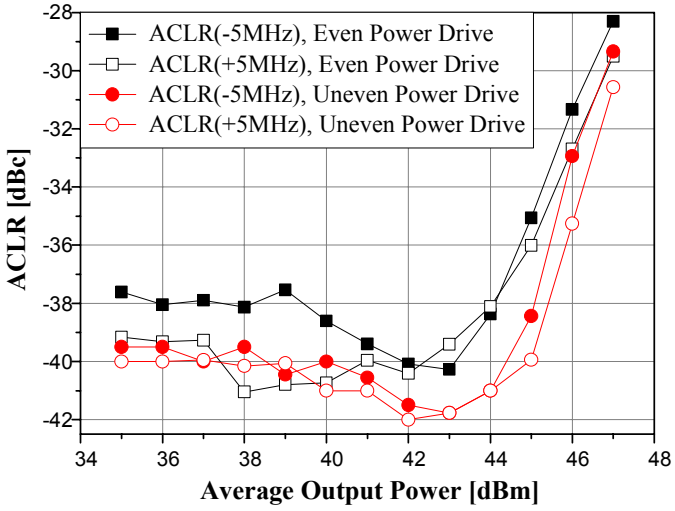

Fig. 4. Measured ACLR performance of Doherty amplifier with even and uneven power drives for WCDMA 4FA signal.

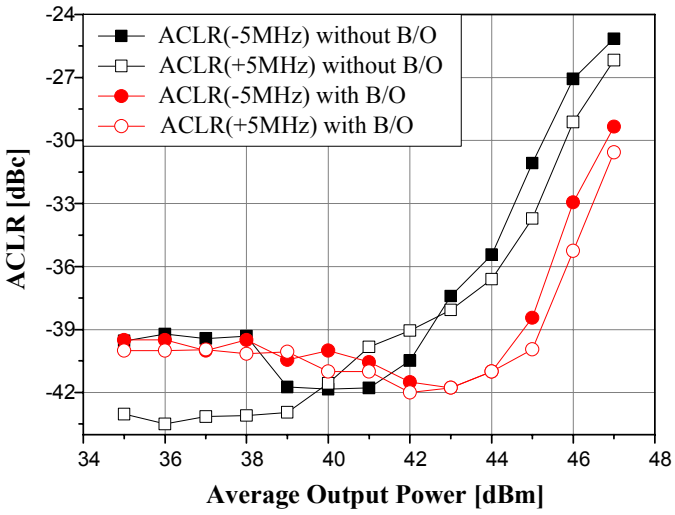

Fig. 5. Measured ACLR performance of the Doherty amplifier according to the bias circuit optimization(B/O).

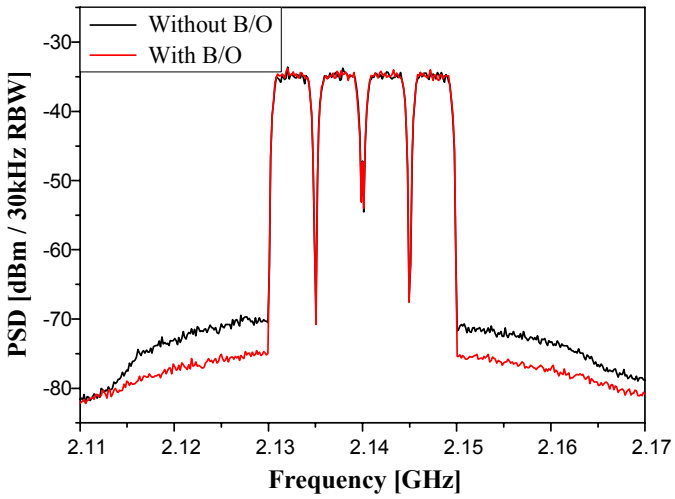

Fig. 6. Output spectrum of the Doherty amplifier with uneven power drive at an average output power of 44 dBm according to the bias circuit optimization(B/O) for WCDMA 4FA signal.

with 1 MHz tone spacing. The PEP of the amplifier with uneven drive is improved by 15 W, from 165 W to 180 W, compared to even case. This result implies that the Doherty amplifier with uneven power drive generates full power from both cells.

Fig. 3 shows the power gain characteristics over average output powers using WCDMA 4FA signal. The uneven power drive delivers more input power to the peaking cell than carrier cell and the power gain of the overall Doherty amplifier is lower because the peaking cell is off-state at a low power region, and the peaking cell has lower gain than the carrier cell at a high power region. We have experienced that the power gain of the uneven case is degraded by about 0.5 dB compared to the even drive case.

Fig. 4 shows the measured ACLR's of Doherty amplifier for the even and uneven cases. In comparison with the even case, the Doherty amplifier with uneven power drive delivers significantly improved ACLR performance, by 3 dB at the average output power of 44 dBm. Additionally, the Doherty amplifier applying the proposed design methods delivers significantly improved linearity performance compared to the

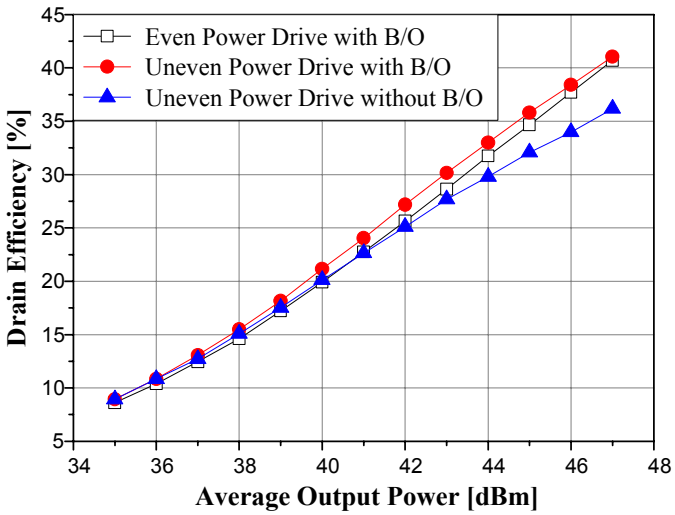

Fig. 7. Measured drain efficiency of the Doherty amplifier with even and uneven power drives according to the bias circuit optimization(B/O) for WCDMA 4FA signal.

TABLE I

MEASURED PERFORMANCE AT AVERAGE OUTPUT POWER = 44 dBm FOR 2.14 GHZ WCDMA 4FA SIGNAL AND PEP

	Gain $[dB]$	Efficiency $[\%]$	ACLR $[dBc]$ -5MHz / +5MHz	PEP $[W]$
Even Drive	10.5	31.7	-38.3 / -38.1	∼165
Uneven Drive	10.1	33	-41.0 / -41.0	∼180

previous results [1].

Fig. 5 shows the measured ACLR performance of the uneven case according to the bias circuit optimization. The drain bias circuit is incorporated a quarter-wave line and several decoupling capacitors which consist of 10 pF for the RF and 22 uF, 10 uF, 1 uF, 1 nF, 150 nF for the envelope frequency. The tantalum capacitors(22 uF, 1 uF) located within a quarter-wave bias line are especially important to minimize the memory effect, while the impedance at the RF is reduced by these capacitors. Thus, we have optimized the bias circuit along with the matching circuit considering these effects. As a result, the bias circuit becomes an active matching circuit, and the difference of ACLR with the bias circuit optimization between lower and upper ACLR is reduced below 2 dB at the whole average output powers. Fig. 6 shows the spectrum of Doherty amplifier with uneven power drive at an average output power of 44 dBm according to the bias circuit optimization.

Fig. 7 shows the drain efficiencies of Doherty amplifier with even and uneven power drive for WCDMA 4FA signal. The drain efficiency of uneven case is slightly improved over the even case.

These results represent that the Doherty amplifier with uneven power drive based on the individually optimized matching circuit and the bias optimization provides highly efficient and linear operation due to the appropriate load modulation, and the results are summarized in Table I. We can also see that the proposed design technology is required

to achieve Doherty amplifier with the high performances over a wideband signal.

IV. Conclusions

We have proposed advanced design methods for the highly efficient and linear Doherty amplifier operation across a wide bandwidth and have implemented the Doherty amplifier using Motorola LDMOS MRF5P21180. The amplifier utilizes the uneven power drive, individually optimized matching, and bias circuit optimization. For a 2.14 GHz WCDMA 4FA signal, the Doherty amplifier has ACLR of -41 dBc and the drain efficiency of 33 % at average output power of 44 dBm. The difference of ACLR with the bias circuit optimization between lower and upper ACLR is reduced below 2 dB at whole average output powers.

These experimental results clearly demonstrate the superior performance of the Doherty amplifier applying the advanced design methods. The proposed design methods are the most suitable to design Doherty amplifier for wide bandwidth and high power operation.

Acknowledgement

This work is supported by Brain Korea 21 projects of the ministry of education in Korea.

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