CDMA Handset Power Amplifier with Diode Load Modulator

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***Abstract* — A new monolithic PA for 836 MHz CDMA cellular phone is developed using a simple diode based load modulator at the output matching circuit. The modulation network allows power level dependent load impedances for better power-added efficiencies. Especially, the PAE at the lower output power range, less than 10 dBm where most of handset operation arises, is increased more than 80%.**

***Index Terms* — Load modulator, power amplifiers.**

I. Introduction

The efficiency of a handset power amplifier at a low power region is of supreme interest due to battery lifetime because the handset operating power level is low mostly, less than 10 dBm[1]-[3] while the maximum output power is about 28 dBm. Various approaches have been reported to get an increased efficiency at the low power region. A Doherty type PA improves the efficiency using load modulation method[4]-[6]. But this type circuit is suitable only for a hybrid type power amplifier because of the large sized impedance transforming circuit. Another MMIC PA utilizes a dc-dc converter to dynamically change the supply voltage[7]. The dynamic voltage control method can improve the efficiency at a power back-off region to somewhat degree. But the main amplifier becomes larger in size and degrades efficiency greatly due to the insertion loss of the current supplying path including the fast dc-dc converter. The switching load modulator[8] has several merits compared with conventional ones[9]-[13] because of its lower loss and simpler control circuit. But all previously proposed impedance modulators[8]-[13] have two problems. First, they require output power level detection circuit. Second, they require additional bias voltage control circuit. We have proposed a novel impedance modulation circuit. The diode based circuit turns on automatically as the power level increases and which allows power level dependent load impedance for a better power-added efficiency, especially at a low power level.

II. Amplifier Design and Theoretical Analysis

Figure 1 shows a schematic of the proposed amplifier which has two stages (T1-T2). On-chip inter-stage matching networks are designed for maximum gain under large signal conditions and a part of the output matching is an off-chip. The diode based load modulation block includes an on-chip capacitor series connected with the diode to reduce the insertion loss of the diode and RF choke for DC path.

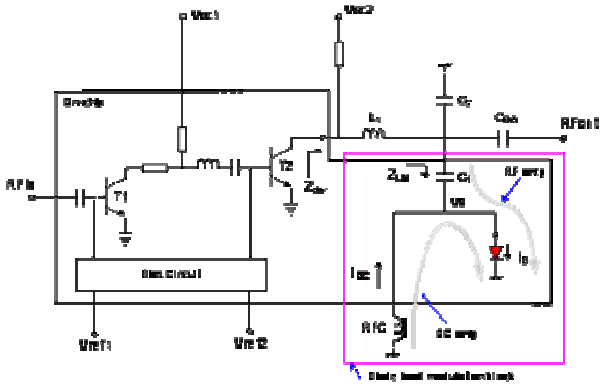

Fig. 1. Schematic of the CDMA power amplifier with diode load modulator

The diode is implemented using BC junction of HBT to bear a high power operation. Without the DC current path, a large signal swing can't be built through the diode. If RF voltage signal $v_D = V_0 \cos \omega t$ is supplied to the diode, the diode current can be represented as follows.

$$i_D = I_s e^{\frac{V_0 \cos \omega t}{nV_T}} \tag{1}$$

Where n and I_s represent the ideality factor and saturation current of the diode, respectively. The i_D is a periodic function because the exponential function has periodic argument. Therefore, i_D can be expanded into Fourier series and the fundamental and DC components of the current i_D are represented as follows.

$$i_1 = 2I_s I_1(\frac{V_0}{nV_T})\cos \omega t \tag{2}$$

$$i_{DC} = I_s I_1(\frac{V_0}{nV_T}) \tag{3}$$

where the function $I_0(x)$ and $I_1(x)$ represent the modified Bessel functions of the first kind with order 0 and 1, respectively. The impedance for fundamental frequency can be obtained easily using above equations as follow.

$$Z_1 = \frac{V_0}{2I_s I_1(\frac{V_0}{nV_T})} \tag{4}$$

where Z_1 is a monotonously decreasing function of V_0.

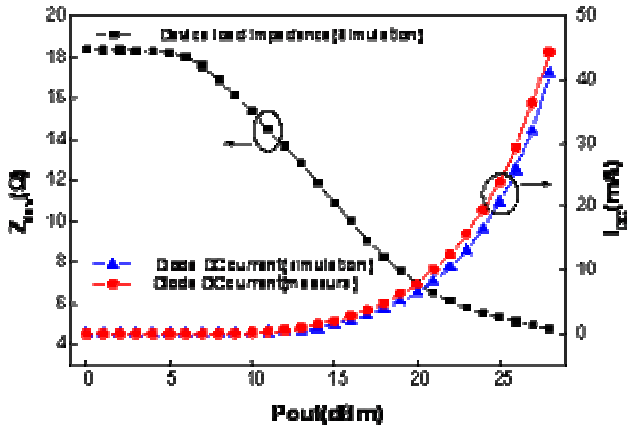

Fig. 2. Device load impedance and diode DC current versus output power

Therefore, the impedance Z_{LM} of the load modulation block gradually approaches the impedance of C_1 as the output power level increases. This is the load modulation we want. In reality, Z_{LM} is modified a little because of the diode capacitance but the intrinsic characteristic remains unchanged. The simulated results for the load impedance Z_{dev} and diode DC current I_{DC} in figure 1 versus output power are shown in figure 2. As shown, there is a significant load modulation, high impedance at a low power level and low impedance at a high power level. The PA for the CDMA handset operates usually in the light class AB - almost class A - because the system requires highly linear performance. Therefore, the analysis of class A can be used for the analysis of the CDMA amplifiers as a matter of convenience. To evaluate the performance of the modulation circuit, we compare the efficiencies of the two amplifiers with/without load modulation. We have analyzed them using a right trapezoid I-V model which is closer to the real device I-V than a rectangular I-V model. In the figure 3, V_{p0} and I_{p0} represent the peak magnitudes of voltage and current signals, respectively, when the PA operates in its maximum output power level. V_{p0} and I_{p0} can be represented by $V_{p0} = Z_{L0} I_{p0}$, where Z_{L0} is the optimum load impedance at the maximum output power level. V_{k0} and I_{k0} represent the knee voltage and current of the PA at the maximum output power level. V_k and I_k are given by $V_k = R_{on} I_k$, where R_{on} is the device on-resistance. The efficiencies of the PA operations at the optimum bias with conventional matching circuit, η_{bias}, and at the optimum bias with the load modulation circuit, $\eta_{bias\&mod}$ can be calculated using figure 3(a) and 3(b) as follows.

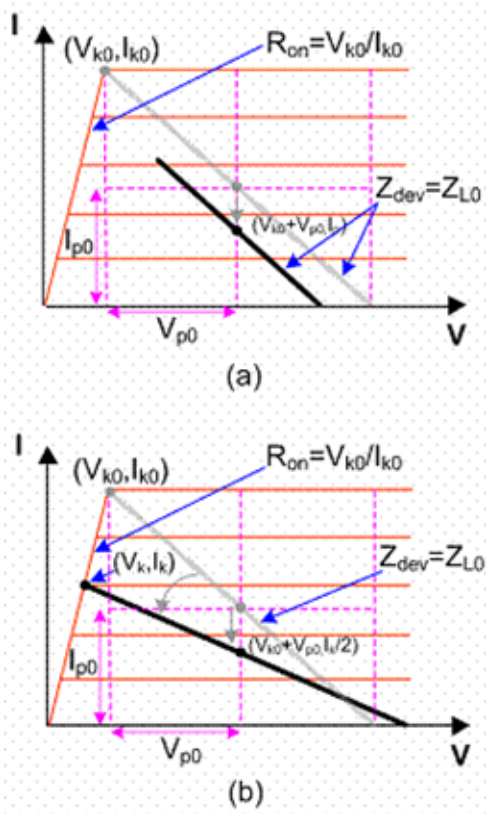

Fig. 3. (a) Class A load line with bias control (b) Class A load line with load modulation and bias control

$$\eta_{bia} = \frac{1}{2\sqrt{\alpha}(1+2q)} \tag{6}$$

$$\eta_{bias\&mod} = \frac{2}{\alpha(2+1/q-\sqrt{(2+1/q)^2-8/qa}} \tag{7}$$

$$r_\eta = \eta_{bias\&mod} / \eta_{bias} = \frac{4}{\sqrt{\alpha}(2+1/q-\sqrt{(2+1/q)^2-8/qa}} \tag{8}$$

where $q = R_{on}/Z_{L0}$, and α represents power back-off level against the maximum output power. The ratio r_η of the two efficiencies versus power back-off level is shown in figure 4. As expected, the efficiency of the amplifier with bias control and load modulation shows a far better efficiency than the other case as q and α increase. The device which has large q

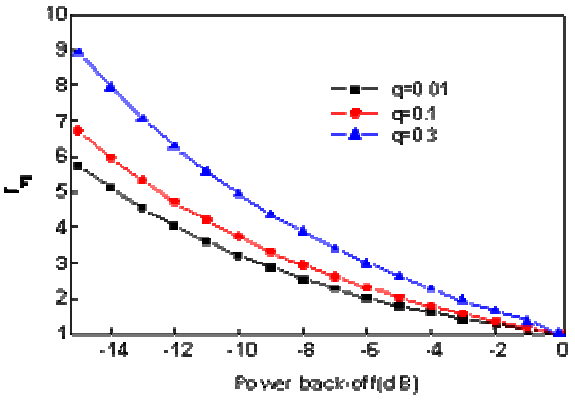

Fig. 4. Calculated efficiency ratio versus power back-off level

means that its knee voltage and/or R_{on} are large and voltage swing is small by its small breakdown voltage such as CMOS devices. The large α means that the operation power level is low compared with the maximum operation power level. Therefore, the power amplifier with load modulator is especially effective for the devices which has a large knee voltage and/or R_{on} and small breakdown voltage. In addition, it is very effective for the all kinds of devices when they operate at high back-off level compared with their maximum power level.

III. Experimental Results

The device is fabricated using HBT3-PA 45 GHz f_T InGaP emitter Heterojunction Bipolar Transistor (HBT) process of Skyworks, CA. It features HBTs, Schottky diodes, base-collector junction diodes typically used for ESD protection, TaN resistors (50 Ω /sq), MIM capacitors ($0.555fF/um^2$), inductors, vias and bonding pads. A die photograph of the fabricated amplifier is shown in figure 5. The chip size is $1.1 \times 1.2mm^2$. A $56um^2$ 24 unit-cell HBT is used for the drive stage, a $56um^2$ 96 unit-cell HBT is used for the output stage, and $24um^2$ 48 unit-cell BC diode is used for the load modulation block. In order to achieve better tunability for the prototype, the output matching circuit is implemented using off-chip components. Measurements are performed on a 400 um-thick FR4 printed circuit board and a chip-on-board assembly is exploited. The gain loss due to the parasitic emitter inductance is minimized by using a large number of down-bonding wires. The bias point is adjusted according to the power level using the control signal available from the base-band controller of CDMA handset. Figures 6 and 7 show PAE, gain, and ACPR of the amplifier at Vcc=3.4 V for reverselink IS-95 A signal with chip rate of 1.2288Mcps at Korean cellular band (center frequency=836.5 MHz). In the case of the bias control with the load modulation, PAE of 14% which is 3.5% better than the case without modulation, and

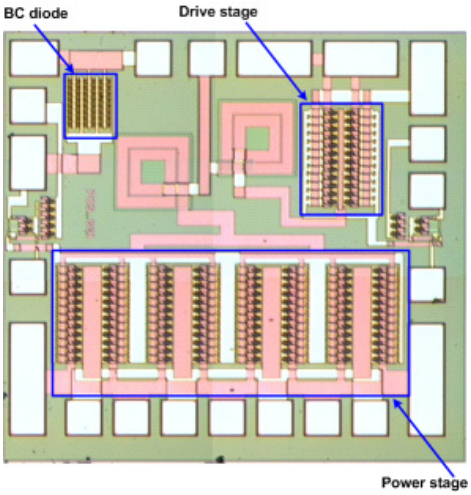

Fig. 5. Die micrograph

ACPR of -46dBc are achieved at an output power of 16 dBm. Especially, the PAE at the lower output power range, less than 10 dBm where most of handset operation arises, is increased more than 80% as shown in figure 6. It is lower than the theoretical value shown in figure 4. The reason is that the modulated impedance level supplied at the low power level is not large enough to satisfy theoretically required impedance level which is around one hundred Ω. The upper impedance level is limited by the terminal impedance 50 Ω. In conclusion, we have proposed a diode based load modulation circuit suitable for monolithic PA and demonstrated the performances. A theoretical analysis is carried out for comparison of the efficiencies of the base bias-controlled amplifiers with/without the load modulation. The PAE of the amplifier is remarkably improved over whole output power range while satisfying the stringent ACPR requirements of the CDMA handset systems. The improvement is especially significant at a low power level.

V. Conclusion

In conclusion, we have proposed truly automatic impedance modulator which doesn't require any power detection circuit and bias circuit which are always required for conventional impedance modulation circuit. And a theoretical analysis is carried out for comparison of the efficiencies of the base bias-controlled amplifiers with/without the load modulation. And the results have shown a far superior performance of the amplifier with the load modulation circuit. We have built a diode based load modulation circuit suitable for monolithic PA and demonstrated the performances. The PAE of the amplifier is remarkably improved over whole output power range while satisfying the stringent ACPR requirements of the CDMA handset systems. The improvement is especially significant at

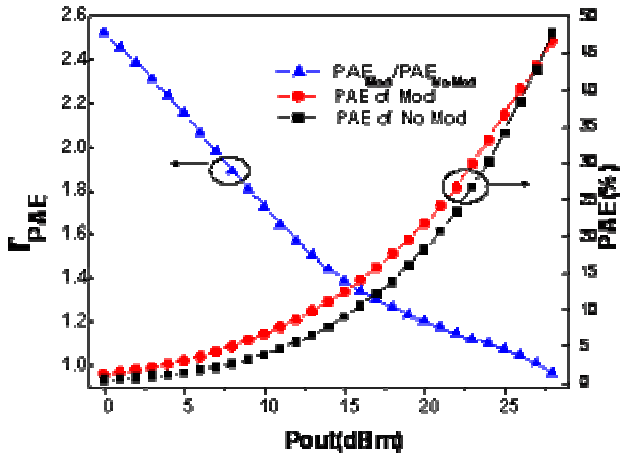

Fig. 6. Measured PAE and PAE ratio versus output power

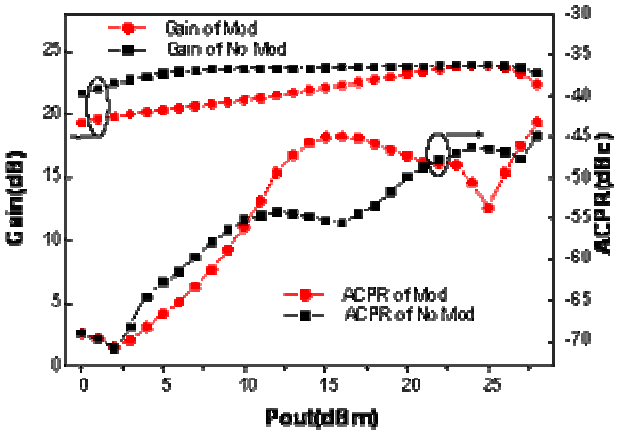

Fig. 7. Measured Gain and ACPR versus output power

a low power level. The PAE is increased more than 80% at the low output power range, less than 10 dBm where the most of handset operation arises.

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