Differential CMOS Linear Power Amplifier with 2nd Harmonic Termination at Common Source Node

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***Abstract*— In this paper, we present a 2.45 GHz fully-differential CMOS power amplifier (PA) with high efficiency and linearity. We have adopted a 0.18 μm standard CMOS process with Cu-metal and all components of the 2-stage circuit are integrated into one chip. To improve the linearity, we newly adopt the harmonic termination technique at the common source along with normal harmonic termination at the drain. The harmonic termination at the source suppresses the second harmonic generated at the input C_{gs} The amplifier shows 17.5 dB of power gain and 20.5 dBm of P_{1dB} with 37 % of PAE. Linearity measurements from 2-tone test show that the power amplifier with the second harmonic termination at the source improves maximum 6 dB of IMD3 and 7 dB of IMD5 over the amplifier with harmonic termination at the drain only. Furthermore, the linearity improvements appear over entire range of the power level and the linearity maintains low below -45 dBc of IMD3 and -57 dBc of IMD5 for an output power backed-off more than 5 dB from P_{1dB}.**

***Index Terms*— Differential power amplifier, even in-phase harmonics, odd anti-phase harmonics, harmonic termination.**

I. INTRODUCTION

As the proliferating wireless personal communication systems require the multi-function capability with miniaturization, CMOS process which has the merit of high level integration becomes a choice of technology for the solution. Due to the recent improvement on RF performances of the CMOS technology, multi-function RF transceivers, including base-band and IF blocks, could be integrated in a single-chip. Many efforts also have been made to implement RF CMOS PA [1]- [3] and integrate it with RF transceiver [4] [5]. But, it is still a big challenges for CMOS PA to be competitive with compound semiconductor based PA. The first problem is device reliability and ruggedness related to the low breakdown voltage characteristic of CMOS. Nowadays, many published papers show competitive power performances of switching type CMOS PA, but the operation at a large voltage swing ($\sim$3.6 V_{dd}) is still a burden. In this point of view, a linear CMOS PA with a relatively low voltage operation ($\sim$2 V_{dd}) is a more feasible solution than the switching type PA.

The second one is the substrate coupling which prohibits the integration of PA with other blocks. The coupled signal from PA is large enough to saturate LNA and disturb the oscillation frequency of VCO (load pulling effect). To reduce the coupling problem, a fully differential circuit topology must be adopted instead of single-ended type PA. In a fully differential condition, the current is dumped to the ground twice per a cycle and the substrate noise components at the signal frequency is suppressed while the second harmonic is remained, resulting in a reduced interference. The PA for wireless system based on a time division duplexing(TDD) mode can be easily integrated with transceiver because TDD based system does not concurrently operate between receiving part and transmitting part and the substrate coupling from PA is confined only to the transmitting part.

Considering the above two major problems and suitable applications, WLAN around 2.4 GHz is selected for the design target to adopt CMOS PA and realize the integrated RF-transceiver including PA. To transfer and receive high-speed data without corruption, WLAN adopts the TDD mode and requires very linear transceiver system, especially for OFDM based WLAN. Additionally, under severe interference restriction between side-bands, the maximum transmitting power is regulated to 20 dBm around 2.4 GHz. This medium power level of 20 dBm lowers the burden of PA reliability and ruggedness.

In this paper, we present a highly linear and efficient CMOS PA targeted for the 2.45 GHz WLAN. After we introduce the fully differential PA, the circuit design and harmonic termination methodology are presented at the third section. At the fourth section, the requirement of newly adopted harmonic termination at the common source is discussed. And then, RF measurements results and comparison of the linearity improvements are presented. Finally, summary of this work is followed.

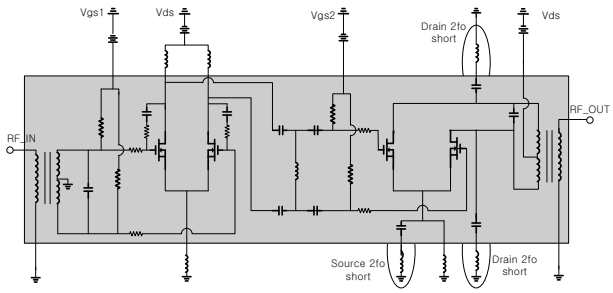

Fig. 1. Schematic of harmonic tuned fully-differential CMOS PA .

II. Implementation of differential CMOS PA

A simplified schematic of the designed PA is shown in Fig. 1. A 0.18-μm RF CMOS technology with Cu process is adopted. Comparing with Al process, the relatively higher quality factor of passive components with Cu-metal makes it possible to integrate the components without any severe power loss. Therefore, all components are integrated with the exception of the output transformer. In Fig. 1, the shaded region shows the integrated part and the components outside of the shaded region are bonding wire inductors and output matching part of the transformer. The bonding wire inductors are used as matching or harmonic control components. Active parts of the 2-stage circuit are 0.18-μm gate length NMOS. The cell sizes are determined through the iterations of simulation to get the best linearity and other RF performances. For the driver part, the gate width of 2 x 2.5 μm x 80 is selected and the width of 2 x 2.5 μm x 480 is chosen for the output cell. The simulation is done using ADS and the unit cell model of 200 μm gate width is expanded for the simulation of output cell. To minimize the thermal degradation and avoid the model deviation due to the expansion, each unit cell of 200 μm gate width is sufficiently separated. For an accurate simulation, the parasitic resistance, capacitance and inductance of the circuit are extracted through the EM-field simulation. This approach is also used for design of the input balun and inductors. The integrated input balun is a square symmetry type. This balun has two groups of inter-wound microstrip lines and the center tab can be placed precisely at the symmetric point between the terminals on each winding. By grounding the center tab, a precisely balanced signal can be obtained. Furthermore, the 2nd harmonic impedance of driver cell can be controlled at the center tab.

III. Circuit design methodology

In designing a linear PA, a class AB with well-controlled harmonics is the best choice to get high PAE and linearity under the trade-off relation between the two factors. In this work, the 2-stage PA adopts the class AB operation for both driver and output cells. To stabilize the PA, the driver cell is feed-backed and series resistor is applied for gain reduction at the driver and output cells. For the linear power operation, the power matching circuit includes the harmonic tunings. In case of differential topology, the characteristics of even in-phase harmonics and odd anti-phase harmonics make it more feasible to control the even harmonics than the single-ended topology. As shown in Fig. 1, the matching between the balun and input of driver cell is done with one MIM capacitor and the input balun is directly matched to 50 ohm input. To get a precisely balanced anti-phase signal after the balun, the center tab is connected to ground. Additionally, the grounded center tab provides nearly zero impedance at the second harmonic, improving the linearity of the driver cell. The inter-stage matching is a high pass filter circuit. This circuit can block the DC currents of each cell and deliver a conjugate matching between the output of the driver cell and input of the power cell. The load matching of the power cell is implemented with off-chip transformer and chip capacitor. To make an effective second harmonic short at the drain of the power cell, a resonance circuit is placed at the end of the drain. The integrated MIM capacitor with bonding wire provides a resonance at 2fo and the resonance frequency can be tuned by adjusting the length of the bonding wire. The bonding wire for the second harmonic short circuit can save the chip area and provides the adjustability. Additionally, by placing this resonance circuit at the very end of the drain and isolating from the drain matching circuit, the detuning effect of the matching is suppressed effectively. In this work, another harmonic termination circuit is implemented at the common source and the implementation method follows the drain harmonic termination case.

IV. Discussion on the effect of harmonic termination at the common source node

The standard CMOS process must use bonding wire for the grounding since via is not provided. In case of PA which has very low impedance, especially for the CMOS PA, a small inductance at the source can degrade power gain severely and the linearity is also very sensitive to the source inductance. A multiple down bonding at the source must be used to reduce the inductance as low as possible but there are limits. The virtual ground of the differential PA can solve the problem. But the linearity under class AB mode operation is another issue because even in-phase signal of differential PA sees the source inductance directly. In a normal class AB mode, it is well known fact that C_{gs}, g_m and R_{ds} are the major nonlinear sources [6] [7]. The nonlinear model of the differential PA with source inductance can be described by Fig. 2.

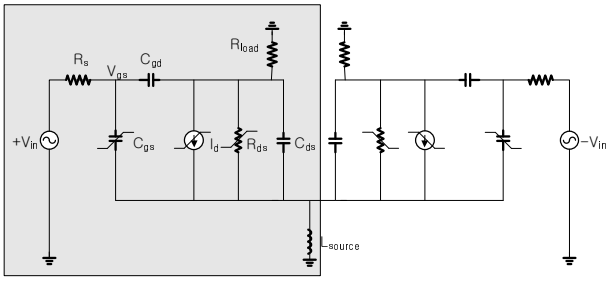

Fig. 2. Nonlinear model of differential CMOS PA.

From the shaded part of the figure, the nonlinear g_m and R_{ds} belong to the output part, while the nonlinear C_{gs} belongs to the input part. Accordingly, even though harmonic control circuit at the drain may terminate the second harmonic from the nonlinear g_m and R_{ds}, it can not basically terminate the second harmonic generated from the nonlinear C_{gs}. Additionally, a simulation result confirms that non-zero inductance at the source increases the harmonic distortion and makes the linearity very sensitive to the variation of it. Therefore, another harmonic control circuit is required to terminate the second harmonic at the input including C_{gs} nonlinearity. For this reason, this work places another second harmonic control circuit at the common source of the power cell as shown in the Fig. 1, whose implementation method follows that of drain harmonic termination. By placing it at the common source, the in-phase second harmonics at input of the power cell is reduced and the sensitivity of linearity on the source inductance is removed. Furthermore, because virtual ground of the fundamental frequency is made at the common source, the disturbance of power gain and PAE by the source harmonic termination circuit is almost negligible.

V. Experimental results

Fig. 3 shows a photograph of the fabricated CMOS PA whose chip area is 1.43 μm x 0.94 μm. Even though full integration of the circuit components increases the chip size, if necessary, it can be significantly reduced after layout optimization. So, we confirm that integration of fully differential CMOS PA is more cost effective than GaAs process, with reasonable chip size and low cost process. To verify the chip, an evaluation board is fabricated using FR-4 PCB and the chip is directly mounted on the ground plate of the evaluation board. Because the bonding wire inductance is dependent on the geometry and the mutual inductance of the multiple bonding makes it difficult to predict precise inductance, the inductances are estimated through EM-field simulation. On the basis of these data, the bonding wire is adjusted for the tuning of the delicate

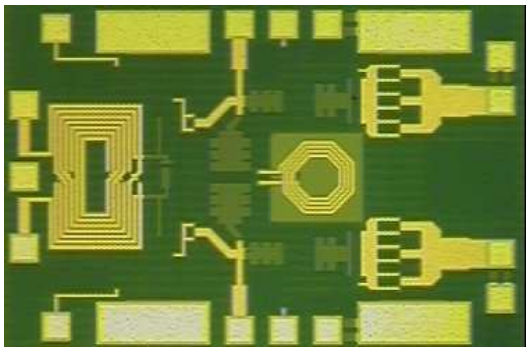

Fig. 3. Photograph of the fully-differential CMOS PA.

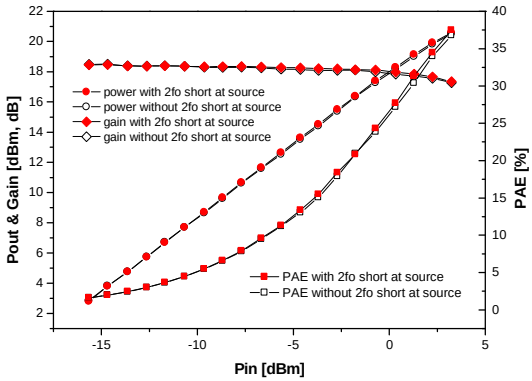

Fig. 4. Comparisons of the output power, gain and PAE between two types of PA with and without the second harmonic termination at the common source.

impedance matching and harmonic control. To measure the RF performances and harmonic termination effects at the common source node, two-tone test is performed at 2.45 GHz center frequency and 2 MHz tone-spacing. The comparison is made between the PA's with and without the second harmonic termination at common source. The both PA's terminate the second harmonic at the drain and 8-multiple bonding wires are provided at the source of the power cell to minimize the wire inductance.

Fig. 4 shows the power measurement results of the amplifier. From the graph, P_{1dB} and power gain of the PA with the second harmonic termination at the common source is 20.5 dBm and 17.5 dB respectively. The PAE at P_{1dB} is 37 %. Comparing the two PA's, the PA with second harmonic termination at the common source shows slightly higher power gain and PAE, but the differences are negligible. A big difference between the two PA's appears at IMD's as shown in Fig. 5. Despite of the high linearity of PA only with drain harmonic termination, both IMD3 and IMD5 of the PA with second harmonic termination are improved significantly. And, these improvements appear across the very broad power level. This result indicates that

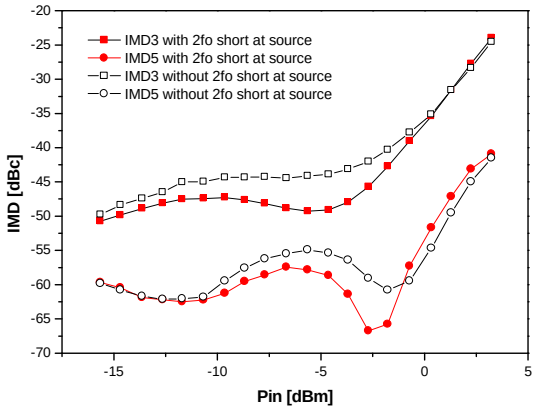

Fig. 5. Comparisons of the IMD between two types of PA with and without the second harmonic termination at the common source.

second harmonic at the input is effectively suppressed with second harmonic resonance circuit at the common source. Various simulation results show that the lower linearity PA operating on class AB has, the more improvement it experiences with the second harmonic termination at the common source. The improved linearity of this amplifier maintains low below -45 dBc of IMD3 and -57 dBc of IMD5 for an output power backed-off over 5 dB from P_{1dB}. We believe that the excellent linear behavior of this amplifier is fully compliant with EVM specification of high-speed data communication covering the 54 Mbps OFDM systems. The reduced linearity improvement at a high power level is due to the transfer of the source for non-linear harmonics generation from the non-linear components (C_{gs}, g_m, R_{ds}) to current saturation.

VI. Conclusions

A differential linear power amplifier at 2.45 GHz is implemented using a 0.18-μm CMOS process. This circuit integrates all components into one-chip and bonding wires are used for matching and harmonic controlling components. The simple and small sized second harmonic termination is realized with integrated MIM capacitor and bonding wire at the drain and source. The newly adopted second harmonic termination at the common source shows a large improvement on linearity without degrading output power and PAE and the excellent linearity is maintained across a broad power range. The RF performance of this amplifier shows the P_{1dB} of 20.5 dBm, 17.5 dB of power gain and 37 % of PAE at the point. The linearity of the amplifier is very good, below -45 dBc for IMD3 and -57 dBc for IMD5 across a broad power rage. These results clearly show that CMOS power amplifier is a fully compliant candidate with high speed data communication covering the OFDM systems.

Acknowledgements

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