An Improved Silicon RF LDMOSFET Model with a New Extraction Method for Nonlinear Drift Resistance

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***Abstract*— An improved large-signal model of RF LDMOS was developed to enhance the accuracy while maintain the physical meaning. Nonlinear drift resistance was carefully investigated and extracted directly from DC measurement data using the concept of the common intrinsic drain voltage in the two or more LDMOSs with different LDD lengths. The intrinsic part of LDMOS was constructed with the popular BSIM-based model. The model was validated in DC and RF results and had good agreements with measured data.**

***Index Terms*— LDMOSFET, lightly doped drain, LDD, large-signal model, RF device modeling.**

I. Introduction

The major difficulty for modeling silicon lateral-diffused metal oxide field effect transistors (LDMOSFET's) arises from the nonlinear drift resistance (R_{dn}), which can not be adequately characterized in popular MOSFET models [1]. Several papers for LDMOSFET model have been treated the resistance of n-LDD region, empirically [2] [3] or physically [4] [5]. The empirical approach means that the channel current model includes the LDD effect, regardless of its physical meaning. The physical method uses a JFET or a nonlinear resistor. Among the physical methods, the popular approach is to treat the LDD effect as a nonlinear drift resistance. The extraction method includes the resistance from the device simulation result [1] [4], the direct probing the intrinsic drain voltage with their special test structures [5], or the difference between the measured DC data and expanded version of low-biased commercial compact model [6]. However, the device simulation results and expansions of a low-biased MOSFET are somewhat unreliable and the direct probing method needs an additional test structure with significant restriction on LDD length.

In this paper, we have proposed a new extraction method of R_{dn}. We use two devices with the same intrinsic MOSFET but different LDD lengths. In this method, the channel output resistance (r_{ds}) and R_{dn} can be separated and extracted directly from DC measurement data. In order to keep physical meaning of the model and utilize the advantage of the mature industry standard, we adopt the physical-based BSIM3v3 for the intrinsic MOSFET model. The overall modeling procedure will be explained with several small unit devices. Finally, verification results with a large size device will be shown.

II. RF LDMOS Model Based on a New Nonlinear Drift Resistance

Fig. 1(a) shows the LDMOS structure with a long n-LDD, a tied source-body, a p+ sinker, and a p+ substrate. A sub-circuit model of an improved RF LDMOS model is shown in Fig. 1(b), which includes a BSIM3v3 intrinsic MOSFET with deactivation of capacitance parameters, a nonlinear drift resistance(R_{dn}), a substrate network(C_{dd} and R_{dd}) under LDD region, bias dependent capacitances(C_{gsx}, C_{gdx}, and C_{dsx}), an intrinsic gate resistance(R_i), and several linear parasitic elements. LDD region influences DC and RF characteristics of LDMOS. Due to the increase of potential drop across the LDD region with enhanced gate voltage, the intrinsic MOSFET of LDMOS is forced away from saturation into triode region of operation, causing a sharp transconductance fall-off. The proposed extraction algorithm is based on the above physical interpretation of R_{dn} behavior. As shown in Fig. 2(a), from the I_{DS}-V_{DS} measurements under the forced operation of V_{GS} for two devices(LDMOS$_A$ and LDMOS$_B$) with different LDD lengths, we can calculate the difference of the extrinsic drain voltages ($V_{DS,A1}$ and $V_{DS,B1}$) between two devices for the same gate bias (V_{GS1}) and intrinsic drain current (I_{DS1}). Then, we can easily calculate R_{dn} for the bias of $(V_{GS1}, V_{DS,B1})$ as shown in eqn. (1).

$$R_{dn}(V_{GS1}, V_{DS,B1}) = \frac{V_{DS,B1} - V_{DS,A1}}{I_{DS1}} \times K_{L_{ldd}} \quad (1)$$

where $K_{L_{ldd}}$ is the LDD size adjustment factor. Using this routine, we can easily extract R_{dn} data for a wide bias range. For accurate and reasonable results, bias range is carefully selected to avoid DIBL at a low V_{GS} and HCE at a high V_{DS}. In this work, two devices of W/L = 6 $\times$ $7.5\mu m/0.25\mu m$ with LDD lengths of 0.175 μm and 1.2

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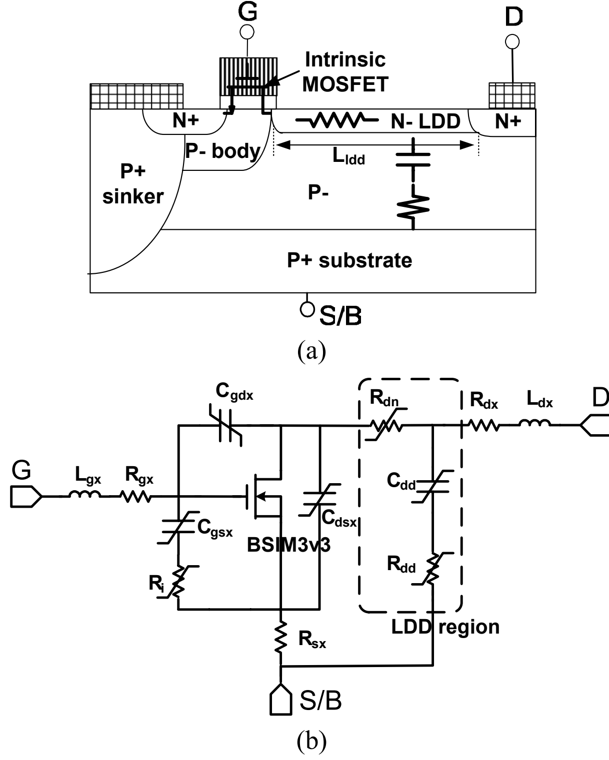

Fig. 1. (a) Cross section of LDMOSFET, (b) proposed sub-circuit model for the RF LDMOSFET.

μm are used. Its extraction and fitting results with the following empirical function are shown in Fig. 2(b).

$$R_{dn,fit} = \frac{45}{W_g(\mu m)} \cdot \frac{L_{ldd}(\mu m)}{1.2} \cdot [r_{d0} + r_{d1}\{r_{d2} tanh(r_{d3}V_{GS}+1)+1\} \cdot \{1 + r_{d4}V_{DS} + r_{d5} tanh(r_{d6}V_{DS}+1)\}] \quad (2)$$

Fig. 2(c) shows the scalability on LDD length (L_{ldd}) of R_{dn}. Two devices with LDD lengths of $1.0\mu m$ and $0.5\mu m$ have the same intrinsic I-V characteristics with each R_{dn} given by eqn. (3). Furthermore, from the intrinsic and extrinsic DC characteristics, we find that the intrinsic MOSFET of LDMOS operates mostly in the triode region with large nonlinearity.

III. Overall Modeling with BSIM-based Intrinsic Model

We have carried out the overall modeling for LDMOS with a total gate length of 45 μm and LDD length of 0.7 μm fabricated by 0.25 μm technology at Samsung Electronics Co., LTD. Fig. 3 shows the overall modeling procedure used in this work. At first, R_{dn} is carefully extracted using the proposed method mentioned in section II. S-parameters are measured at several bias conditions and de-embedded. The series parasitic elements are determined from "cold" S-parameters with V_{GS} = V_{DS} = 0 V. The substrate network is extracted and fitted under the bias condition with V_{DS} = 0 $\sim$ 9 V and V_{GS} = 0 V. These results are depicted in Fig. 4. Accompanied with R_{dn}, the substrate network models the effect of LDD region. The next step is to extract the intrinsic channel current model, which is performed after de-embedding the extrinsic series resistances including R_{dn}. BSIM3v3 compact model is used. As shown in Fig. 5, the intrinsic MOSFET has a moderate transconductance fall-off at a high current level

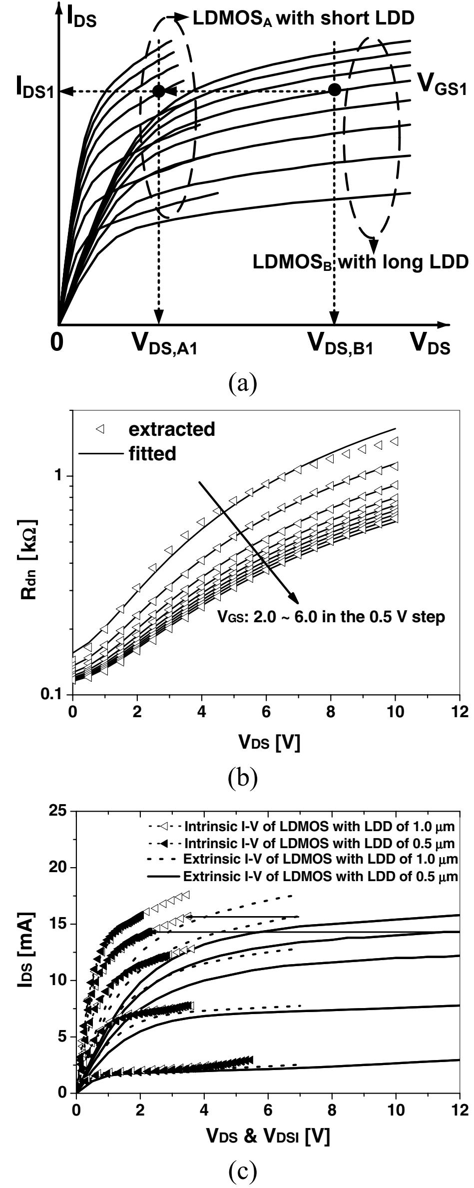

Fig. 2. Nonlinear drift resistance (R_{dn}): (a) the extraction algorithm, (b) extraction and fitting results, (c) the common intrinsic MOSFET model.

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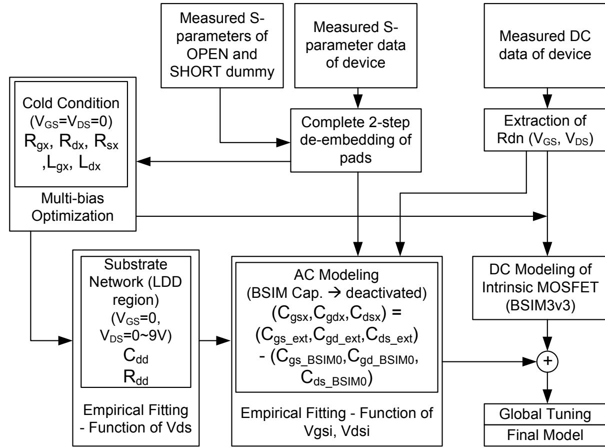


Fig. 3. Overall modeling procedure for RF LDMOSFET with nonlinear drift resistance.

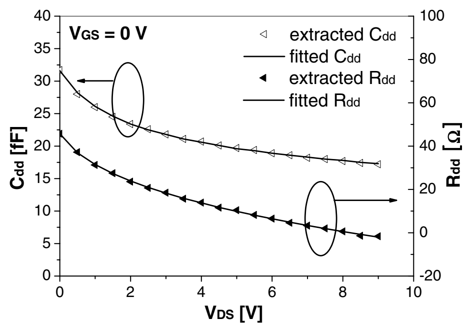


Fig. 4. Extraction and fitting results of substrate network elements: C_{dd} and R_{dd}.

due to mobility degradation by the high vertical electric field and degeneration by series resistances. However, R_{dn} creates a sharp fall-off, especially at a low drain bias, and generates strong nonlinearities. Nonlinear capacitances and intrinsic gate resistance of the intrinsic part of LDMOS are extracted following reference [7]. Since the capacitance and intrinsic gate resistance models of BSIM3v3 have some limits on accurate RF modeling, all of capacitance parameters are deactivated and NQS flag is set to zero. However, due to the incorporation of DC and AC behaviors of BSIM-model, the model still has capacitive components denoted C_{gs_BSIM0}, C_{gd_BSIM0}, and C_{ds_BSIM0}. Additional capacitances (C_{gsx}, C_{gdx}, and C_{dsx}) are added to get the extracted C_{gs}, C_{gd}, and C_{ds} as shown in Fig. 6. After the whole extraction and fitting steps, we have constructed the sub-circuit model in Agilent's ADS, using a BSIM3v3 and symbolically defined devices (SDD's).

IV. Model Verification and Discussion

For further verification of the usefulness, we have applied the proposed method to a large size device with

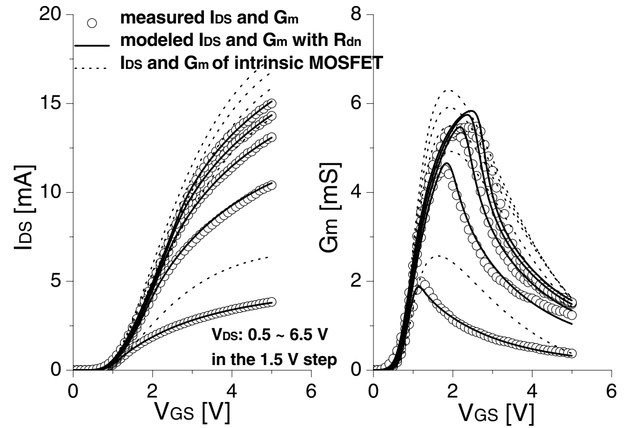
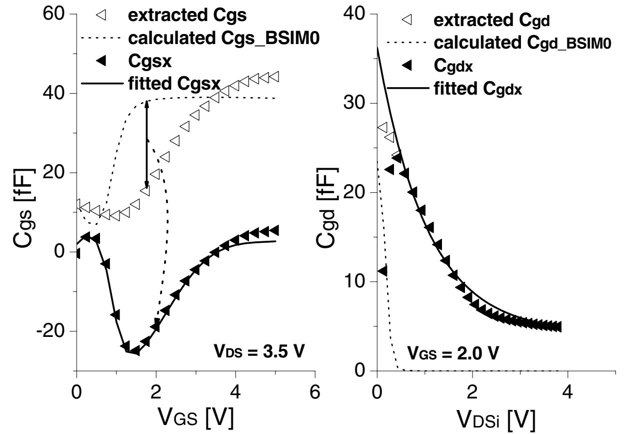
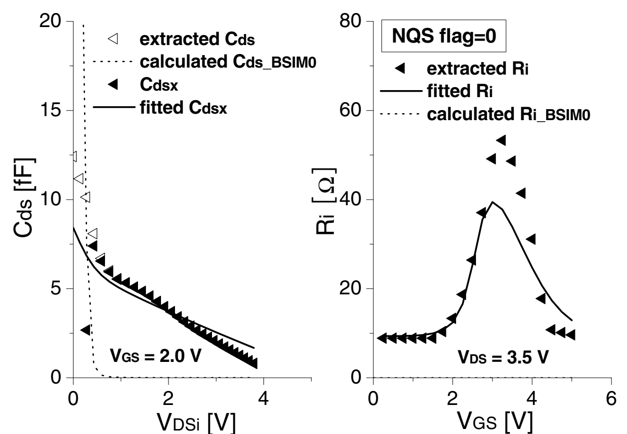


Fig. 5. Channel current modeling of the intrinsic MOSFET (BSIM3v3) with R_{dn}: I_{DS} and G_m.



(a)



(b)

Fig. 6. Nonlinear capacitances and gate resistance, extracted results, BSIM-elements incorporated DC model, additional nonlinear elements, and their fitted results, (a) C_{gs} and C_{gd}, (b) C_{ds} and R_i.

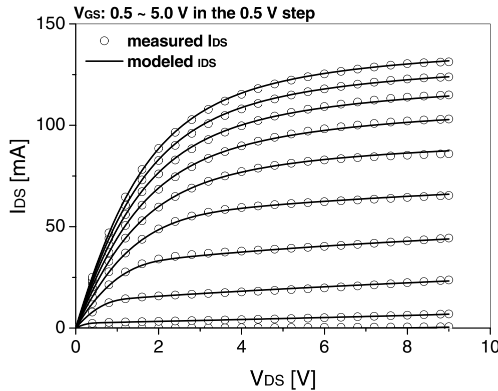
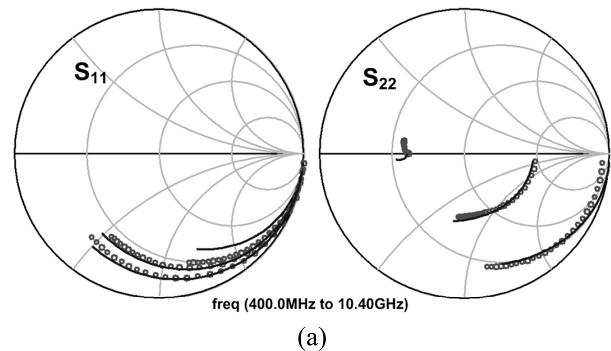
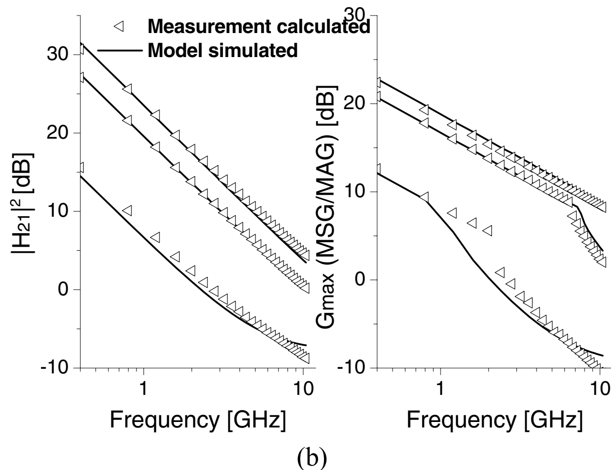


Fig. 7. Measured (symbol) and simulated (line) results of DC characteristics of the LDMOS with $W/L = 80 \times 5\mu m/0.25\mu m$.



(a)



(b)

Fig. 8. Measured (symbol) and simulated (line) RF characteristics of (a) S_{11} and S_{22}, (b) $|H_{21}|^2$ and G_{max}(MSG/MAG) of the LDMOS with $W/L = 80 \times 5\mu m/0.25\mu m$ in the frequency range of $0.4 - 10.4GHz$, at the (V_{DS}, V_{GS}) = (1.0V, 5.0V), (3.5V, 3.0V), and (6.0V, 1.0V).

total gate length of 400 μm and LDD length of 0.7 μm. Fig. 7 compares the measured and simulated results of the DC characteristics. As shown in the figure, the simulation result is in good agreement with measurement data. Fig. 8 shows S_{11}, S_{22}, and RF gain characteristics under various bias conditions from the measurement and the simulation of the developed model. Again, they fit moderately well in the wide bias range. In a deep triode bias region such as (V_{DS}, V_{GS})=(1.0V, 5.0V), slight discrepancies are found due to the fitting error of bias dependent intrinsic capacitances with strong nonlinearities. The results of the large size device modeling show that the developed extraction method of R_{dn} is scalable for the gate width and LDD length and it is a useful extraction method.

V. Conclusions

A simple and accurate extraction methodology of nonlinear drift resistance of LDMOS is proposed for modeling the LDD region. Based on the concept, a large-signal model that includes the resistance has been developed to predict the RF LDMOSFET characteristics accurately while keeping the physical meaningfulness. The simulated DC and RF characteristics using the model have good agreements with measured ones.

Acknowledgements

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