Phase Noise Optimization of CMOS VCO through Harmonic Tuning

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***Abstract* — An optimization technique for a low phase noise CMOS LC VCO is proposed. The combination of harmonic tuning and on-chip filtering improves both *1/f* ^{3} and *1/f* ^{2} phase noise more than 10 dB over a comparable reference VCO. A 2.7 V, 5.4 mA, 30 % tuning range, 1 GHz voltage controlled oscillator (VCO) is designed with the technique and implemented in a 0.35 μm CMOS process. The optimized 1 GHz CMOS differential VCO achieves -89 dBc/Hz, -116 dBc/Hz and -135 dBc/Hz at 10 KHz, 100 KHz, and 1 MHz offset frequencies from the carrier, respectively.**

***Index Terms* — CMOS VCO, harmonic tuning, low phase noise, nano CMOS, flicker noise.**

I. Introduction

A major challenge in the wireless industry these days is the high level integration of functional blocks using low-cost CMOS technology. Among the efforts for the single chip radio integration, the implementation of a low phase noise VCO gets a lot of attentions because the phase noise of the VCO is one of the most critical parameters for the establishment of the information transfer function. As the CMOS downscaling is in progress for high level integration at a low cost, the *1/f* corner frequency of the small size transistors in the newer process tends to increase and this is the crucial problem of the CMOS VCO. This paper presents an optimization technique for the phase noise performance of the CMOS LC VCO which reduces the up-converted flicker noise dominated *1/f* ^{3}-shaped part and thermal noise dominated *1/f* ^{2}-shaped part of the noise spectrum. The optimized 1GHz CMOS differential VCO delivers a measured phase noise which is 10dB lower than a conventional one for both close-in phase noise at 10KHz offset and a higher offset phase noise at 1MHz. Fig. 1 shows a simplified schematic diagrams of the proposed CMOS LC VCOs

II. Phase Noise Issues and VCO Design

Recently, the theory and analysis for the physical processes of the phase noise in differential oscillators [1] have been made significant progresses and the techniques to lower the phase noise have been advanced by understanding of these phase noise mechanism [2]. The phase noise is mainly induced from various mixing phenomena of negative gm switching differential pair such as downconversion from thermal noise component at harmonics of the oscillation frequency and upconversion from flicker noise in baseband to the phase noise in fundamental frequency.

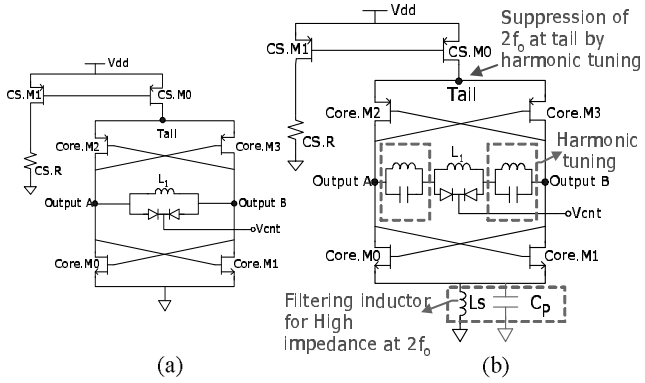

Fig. 1. A simplified schematic diagrams of (a) Standard VCO and (b) Harmonic tuned VCO.

The well-known phase noise model for an oscillator is Leeson's proportionality [3].

$$L\{\Delta\omega\} \propto \frac{1}{V_0^2} \cdot \frac{kT}{C} \cdot \left(\frac{\omega_o}{Q}\right)^2 \cdot \frac{1}{\omega_m^2} \tag{1}$$

Where the phase noise is given by *kT/C* noise that is shaped in frequency domain by LC tank and normalized to the power in the tank. The phase noise is scaled by a specific noise factor *F*, which has been extracted recently for an LC oscillator [1] from the noise model of mixer with a switching differential pair [4]. The noise factor is given by

$$F = 2 + \frac{8\gamma IR}{\pi V_o} + \gamma \frac{8}{9} \cdot g_{mbias} \cdot R \tag{2}$$

Where I is the bias current, γ is the channel noise coefficient of the FET, R is the load resistance and g_{mbias} is the transconductance of the current-source FET. The first and second terms in equation (2) describe the phase noise contributions from the resonator loss and differential-pair FETs, respectively. The second term can be reduced by increasing V_o, which is the voltage across the resonator and proportional to the slope at zero crossing voltage at the switching cell [4]. Thus, increasing V_o means a steep rising at the zero crossing point. To realize the concept, we have employed a harmonic tuned LC tank, which can deliver a square wave form voltage to the cell [5]. The proposed LC tank is open at the fundamental frequency and third harmonic and short at the second harmonic as shown in Fig. 2.

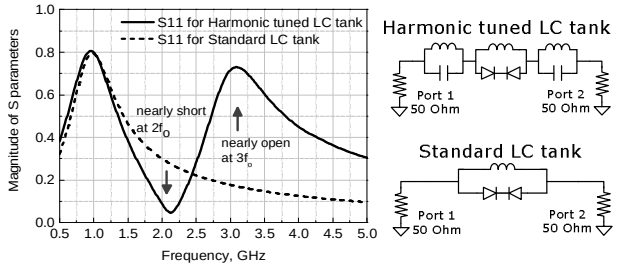

Fig. 2. Simulated S parameters of the two tanks for 50 Ohm terminations.

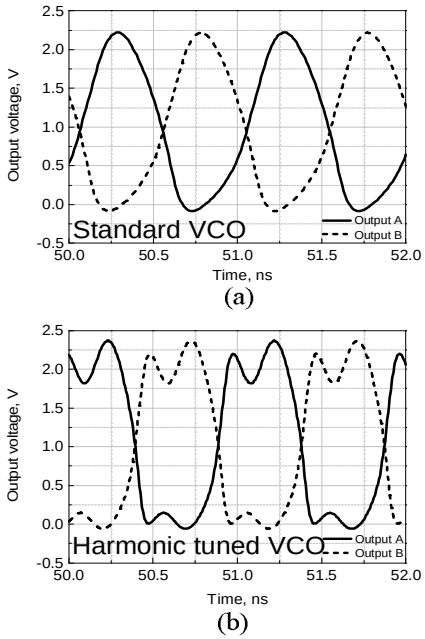

Fig. 3. Simulated time-domain voltage waveforms of (a) Standard VCO and (b) Harmonic tuned VCO.

With these LC tanks, the simulated output waveforms of oscillators at output node A and B of Fig. 1 are shown in Fig. 3.

Actually, because the phase noise from the resonator loss is also induced via modulation of zero crossing instants of the differential pair, the harmonic tuning can reduce the resonator noise portion also. The third term signifies the phase noise produced by down-conversion of the current source noise component at the 2nd harmonic of the oscillation frequency. The harmonic tuned LC tank presents shortness at the 2nd harmonic and this stabilizes the tail voltage fluctuation (see Fig. 4.). Thus, the current source induced phase noise is reduced through the harmonic tuning.

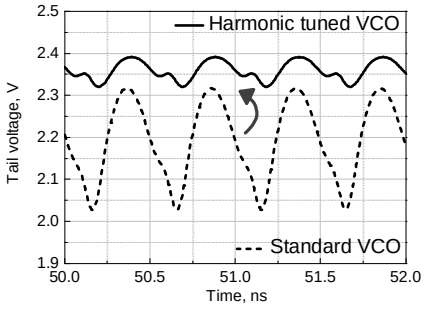

Fig. 4. Suppression of 2fo at tail node by harmonic tuning.

The phase noise close-in to the oscillation frequency is dominated by the flicker noise upconversion and has a slope of -30 dB/decade. The noise sources for the upconversion are the tail current source (CS) and negative gm switching differential pair.

The flicker noise from the tail current source is converted to f_o due to the mixing action of the VCO circuit [6] and the noise is delivered to the resonator as an AM noise and the tuning varactor converts the AM noise into an FM noise [1]. The FM sidebands appear as the close-in phase noise. The AM to PM conversion depends on the gain of the varactor and can be minimized by reducing the size of the CMOS varactor, while a wide tuning can be implemented via capacitor array which is switched on and off in parallel with the LC tank [2]. The switched tuning method is not adopted in this paper for a simple structure but PMOS CS with a large gate length of 3μm is used instead for less *1/f* noise generation.

Additionally, tail node(the common mode node of the CS) oscillates at twice of the oscillation frequency, $2f_o$ because the CS is pulled every time each NMOS (PMOS) transistor of the differential pair switches on. Thus, the flicker noise of the CS is upconverted to $2f_o$ through

channel length modulation [6] and it is mixed down again to the oscillation frequency and presents the close-in phase noise. The phase noise can be minimized by suppressing the 2nd harmonic at tail node(the common mode node of the CS). The suppression of $2f_o$ is made by the proposed harmonic tuning.

The flicker noise from the switching differential pair modulates the 2nd harmonic voltage waveform at the common source node every half period, which induces a noisy current in the parasitic capacitance at the source of each switching pair. This current is mixed down to the fundamental frequency by the switching pair, inducing the close-in phase noise. Actually this phase noise is a small portion due to the switching nature of the oscillator, but this portion can be increased with the downscaling of CMOS to nano-size. In nano-CMOS with tens of nm gate length, though the CS flicker noise can be minimized using MOS transistors with relatively large gate length, the nano-size transistors should be used for the switching pair for high frequency operation and generate much more flicker noise.

A process that plays an important role for generation of the *1/f* noise in MOSFET is carrier (de)trapping in localized oxide states. The switching interferes with the (de)trapping process and can be a means to reduce the *1/f* noise itself by forcing the trap to release its captured electron [7]. The proposed harmonic tuning makes the oscillating wave rectangular, much like an ideal switching with 50 % duty cycle. Ideally, it can remove all memory and consequently the flicker noise. The phase noise contributions of the various noise components of the test VCO at 100 KHz offset frequency show this anomalous 1/f noise reduction effect (see Table. 1).

TABLE I

PHASE NOISE CONTRIBUTION OF THE PROTOTYPE LC VCO

Standard LC VCO			Optimized LC VCO		
Noise sources	**Noise contribution (V^2/Hz)**	**% of Total**	**Noise sources**	**Noise contribution (V^2/Hz)**	**% of Total**
Core.M0, fl	4.53e-12	18.23	CS.M0, th	4.24e-13	11.03
Core.M1, fl	4.53e-12	18.23	CS.M1, th	4.24e-13	11.03
CS.M1, th	3.77e-12	15.16	Core.M3, th	4.00e-13	10.43
CS.M0, th	2.69e-12	10.81	Core.M2, th	4.00e-13	10.43
CS.M1, fl	2.39e-12	9.60	Core.M0, th	2.75e-13	7.16
Core.M1, th	1.50e-12	6.04	Core.M1, th	2.75e-13	7.16
Core.M0, th	1.50e-12	6.04	CS.M1, th	2.68e-13	6.97
CS.R, rn	1.17e-12	4.70	Reso.L1,rn	1.76e-13	4.58
CS.M0, fl	1.09e-12	4.38	Core.M0, fl	7.74e-14	2.1
Reso.L1,rn	3.61e-13	1.45	Core.M1, fl	7.74e-14	2.1

Core: switching differential pair, CS: current source, Reso: resonator
fl: flicker noise, th: thermal noise, rn: resistor

The noise filtering technique [2] prohibits the resonator being loaded by differential pair FETs in triode region, thus prevents degradation of the resonator Q. A 10 *nH* inductor is used to resonate at $2f_o$ in parallel with the parasitic capacitance C_P. This technique has an independent phase noise reduction effect and the combination of both harmonic tuning and filtering technique can reduce the phase noise significantly for both $1/f^3$ and $1/f^2$ regions. Using these techniques, a complementary VCO is adopted for the phase noise optimized test structure. The phase noise simulation results in Fig. 5 shows the phase noise reduction effect of each technique and also of the combined case.

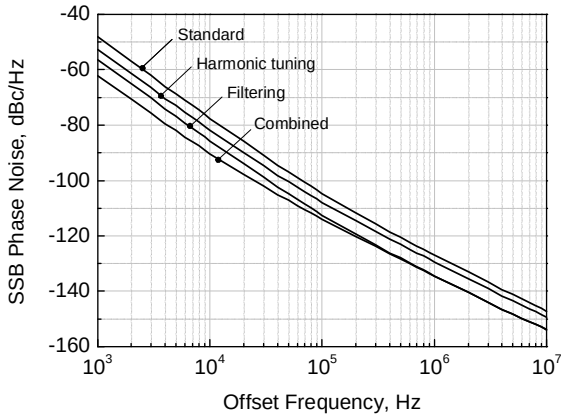

Fig. 5. The simulated phase noises for 1GHz VCO, showing the phase noise reduction effects for each technique and for combined case.

For the design parameters, a symmetric inductor of 9 *nH* with patterned ground shield and two diode varactors of 4.5 *pF* in series connection are used for the resonator at f_o and estimated Q of the inductor is about 9. The additional resonator at $3f_o$ is included using 1.2 *nH* inductor and 1.15 *pF* capacitor. Fig. 2 shows the simulated S parameters of the two tanks for 50 Ω terminations. The combined circuit of the two resonators provides nearly perfect short at $2f_o$, creating the rectangular wave at OSC output node as shown in Fig. 3(b).

III. MEASUREMENT RESULTS

A test VCO circuit is designed using the proposed phase noise optimization technique in the 0.35μm CMOS process of STMicroelectronics. The microphotograph of the fabricated chip with 1.2 mm x 0.43 mm area is shown in Fig. 6. The VCO is tunable between 800 MHz and 1.1 GHz. The VCO operates from 2.7 V supply and biases at 5.4 mA. The packaged chips are measured on a HP4352S

VCO/PLL signal test system. Fig. 7 plots the measured phase noise for the test VCO at the oscillation frequency of 1 GHz. It is compared with the measured phase noise of the standard VCO. Both OSCs are biased at the same current. The fully integrated VCO with the phase noise optimization technique shows a phase noise reduction of about 10 dB in both $1/f^3$ and $1/f^2$ regions. The VCO achieves -89 dBc/Hz, -116 dBc/Hz and -135 dBc/Hz at 10 KHz, 100 KHz, and 1 MHz offset frequencies from the carrier, respectively. The proposed phase noise suppression technique arises from understanding of both thermal and flicker noise induced phase noise mechanism and enables the reduction of differential switching pair flicker noise itself and its translation into phase noise. This is represented by the reduction of $1/f^3$ corner frequency from 110 to 35 KHz (Fig. 7).

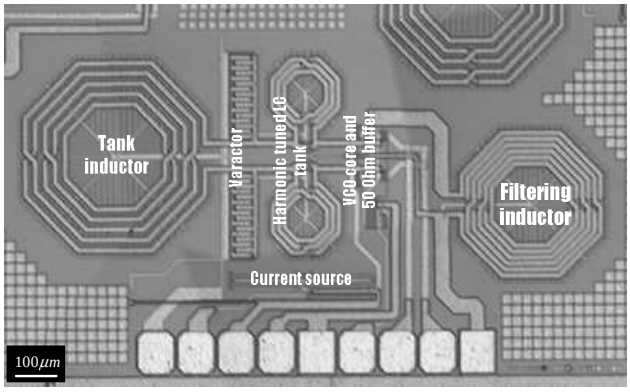

Fig. 6. Microphotograph of the VCO with 1.2mm X 0.43mm chip area.

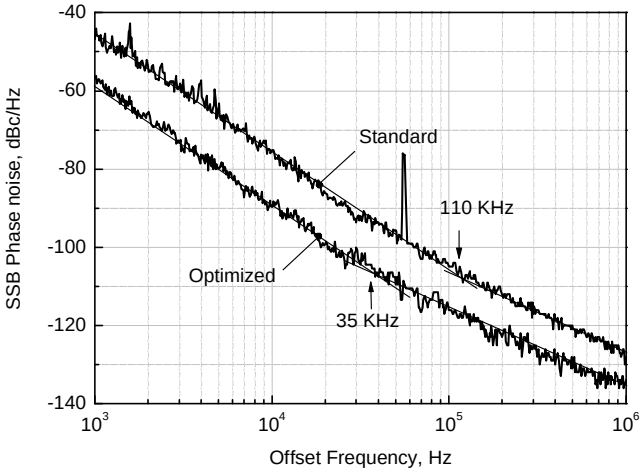

Fig. 7. Measured phase noises at 1GHz of the proposed VCO and comparable standard VCO.

TABLE 2
DIMENSIONS OF THE VCO TRANSISTORS

Transistors	Size (W X L in μm)
CS,M1	300 X 3
CS, M0	320 X 3 (4)
Core, M2, M3	160 X 0.35
Core, M0, M1	100 X 0.35

IV. CONCLUSIONS

A 2.7 V, 5.4 mA, 1 GHz CMOS LC tank VCO with 30 % tuning range has been presented. The proposed phase noise optimization technique achieves a phase noise reduction of about 10 dB in both $1/f^3$ and $1/f^2$ regions, which is from maximizing the slope of the output voltage wave at zero crossing point, presenting very low resonator impedance at $2f_o$ and providing high impedance at common source node of NMOS switching pair at $2f_o$. The proposed technique also reduces the differential pair flicker noise itself and is expected to extend the applicability of CMOS LC VCO to nano CMOS with progressed downscaling.

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