11.9 A Single-Chip Linear CMOS Power Amplifier for 2.4 GHz WLAN

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A number of different CMOS implementations of power amplifiers (PAs) have performed well [1-4], but most of them are switching-type PAs. In this paper, we report the first demonstration of a single-chip linear CMOS PA for OFDM WLAN applications. This PA adopts a fully differential topology with a transformer-type output matching and operates at V_{DD} = 3.3V. All of the components are integrated on a single 0.18μm CMOS die, including input balun and output transformer, and no off-chip components are required.

A simplified schematic of the 2-stage CMOS PA that we have developed is shown in Fig. 11.9.1. For 3.3V operation, the power stages consist of 0.35μm NMOS transistors with high breakdown voltage and a feedback stabilization circuit. To compensate for the low RF power gain of the 0.35μm NMOS power cells, the driver cells consist of 0.18μm NMOS transistors and adopt a new self-biased cascode configuration for 3.3V operation. Compared to a conventional cascode structure, this configuration lowers the burden for gate-oxide breakdown and reduces the chronic generation of harmonics. The input balun uses a structure with square symmetry and the center tap of the secondary winding is connected to ground to achieve a precisely balanced signal and the 2nd-harmonic termination of the driver cell.

Integrating the output network using a low-loss transformer is very important for realizing a high PAE in a CMOS PA [2,5] and cannot be achieved using a conventional spiral transformer. For this reason, we have developed a new type of transformer on a Silicon substrate; the basic structure is shown in Fig. 11.9.2. This transformer consists of two half-turned slab inductors and the balanced signal is transformed into an unbalanced signal by purely magnetic coupling. In this transformer, the coupling coefficient k is high in the GHz band even though the half-turned two slab inductors and magnetic flux cancellation from the oppositional line doesn't exist, enhancing the passive efficiency (P_{out}/P_{in}). Therefore, the loss is mainly determined by metal conductivity. For the output impedance matching, MIM tuning capacitors are connected to the inner and outer slab inductors as shown in Fig. 11.9.2. Since the transformer should be resonant at the operating frequency for minimum loss and the impedance should be matched at the same time, the values of the slab inductors and tuning capacitors should be carefully determined. In this CMOS technology, 2μm thick Al is used for the circuit and the integrated transformer is about 83% efficient (i.e., it has about 0.8dB of loss) at 2.4GHz when operated without bias. We have also confirmed that the passive efficiency can be further improved to over 90 % with Cu metalization. Since the center of the first slab inductor forms a virtual ground, the DC bias can be connected at this point, simplifying the bias circuit. The 2nd-harmonic termination for the linearization can be done with only one MIM-capacitor as shown in Fig. 11.9.2. Along with the inductance of the first slab inductor, the MIM capacitor causes the circuit to be resonant at $2f_o$ and linearizes each cell of the power stage simultaneously.

In a class-AB CMOS PA, the transconductance and gate-source capacitance are the major sources of nonlinearity. Even though the 2nd harmonics generated by the transconductance are terminated at the transformer, significant residual 2nd harmonics still exist at the output because of the source inductance of bond wires. Therefore, to further reduce the 2nd harmonics at the output, another MIM-capacitor is added at the common source of power stage which forms a $2f_o$ resonance circuit along with the seriese inductance of bond wire, which is shown in Fig 11.9.1. For the self-cancellation of the 3rd harmonics caused by g_{m3}, the gate bias point is set to the g_{m3} zero-crossing point and the output impedance is adjusted for harmonic cancellation from the large signal. To reduce the harmonic generation from the gate-source capacitance, a deep N-well (DNW) is employed for the unit power cells. DNW under the active region of an NMOS transistor effectively reduces the gate-source capacitance nonlinearity without disturbing the DC characteristics. Besides, DNW can suppress the noise coupling through the highly conductive Silicon substrate, which is an important concern for SOC implementations.

This CMOS PA is designed for 2.4GHz WLAN with an OFDM signal, which is a follow-up IEEE 802.11g standard. The measured RF performance is shown in Fig. 11.9.3. At $P_{1dB,}$ the PA delivers 24.5dBm with 19.8dB power gain and 31% PAE. To test EVM, a 54Mbps/64 QAM OFDM signal is applied; the measured result is also shown in Fig. 11.9.3, where the EVM of the signal source itself is 1%. From the figure, we see that the PA delivers 18.8dBm average power with 15.8% PAE and 4.6% EVM, and 17.9dBm with 14% PAE and 3% EVM. Figure 11.9.4 shows the output spectrum and signal constellation at 17.9dBm average output power with 3% EVM.

The CMOS PA is fabricated in a standard 0.18μm CMOS process and the performance is summarized in Fig. 11.9.5. Figure 11.9.6 shows a micrograph of the single-chip linear CMOS PA. The total chip area is 1×1.7mm².

Acknowledgements:
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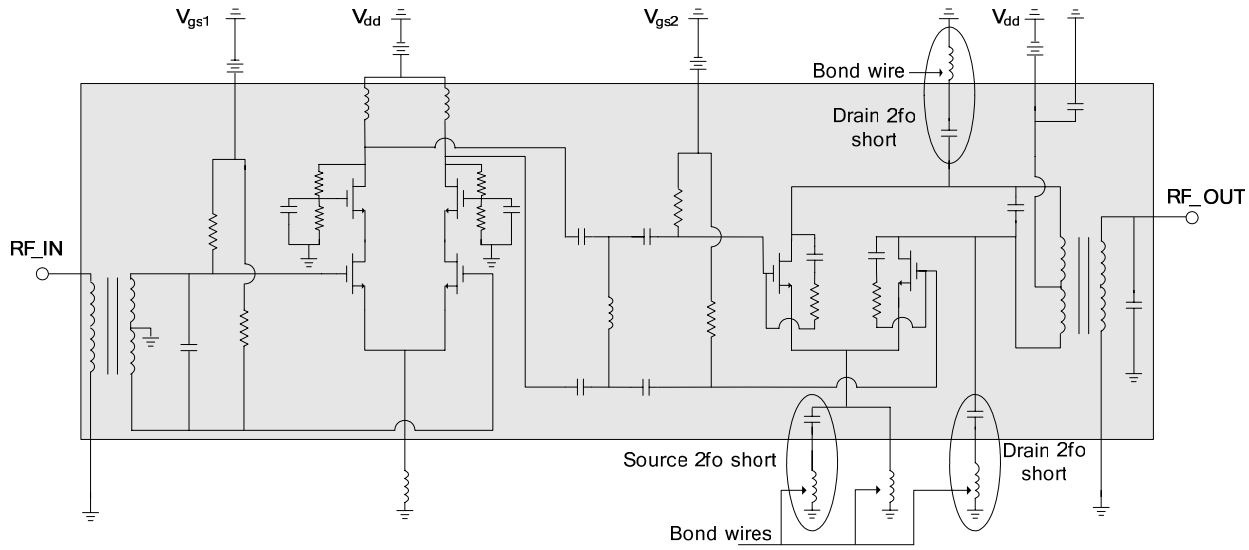

Figure 11.9.1: Simplified schematic of single-chip linear CMOS PA.

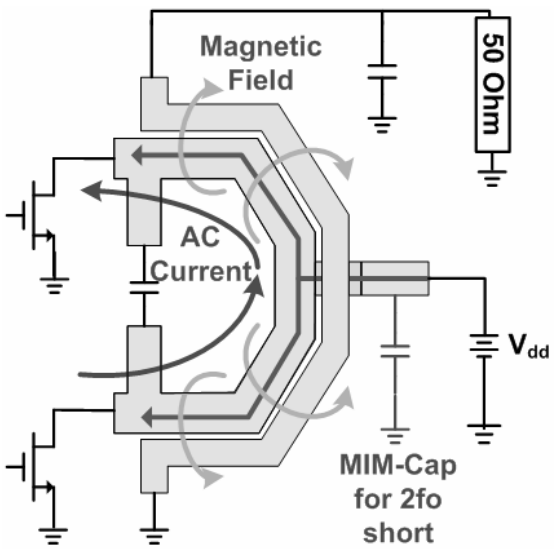

Figure 11.9.2: Basic structure of integrated transformer.

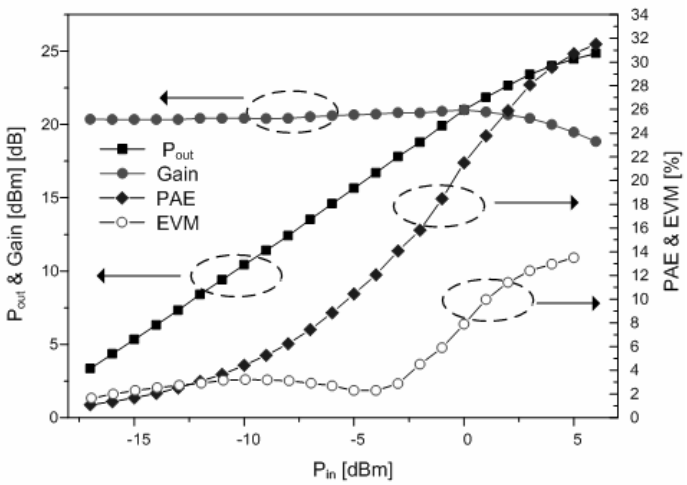

Figure 11.9.3: Measured RF performance (P_{out}, Gain, PAE) and EVM.

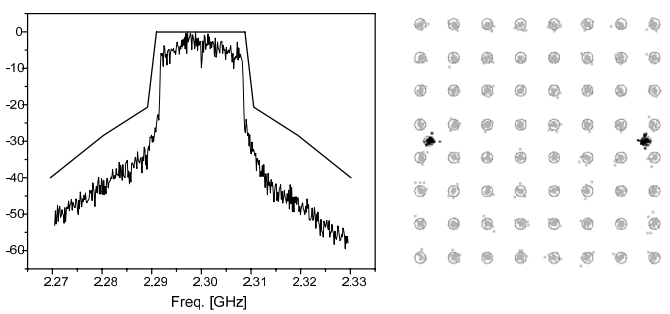

Figure 11.9.4: Output spectrum and signal constellation (P_{out}=17.9dBm, EVM=3%).

Technology	0.18 µm CMOS	
Power Supply	3.3 V	
Frequency	2.4 GHz	
Area	1 x 1.7 mm^2	
RF performance at P_{1dB}	**measured**	
P_{out}	24.5 dBm	
Power gain	19.8 dB	
PAE	31 %	
OFDM signal Test	**54 Mbps/64 QAM**	
EVM	4.5 %	3 %
Average power	18.8 dBm	17.9 dBm
PAE	15.8 %	14 %

Figure 11.9.5: Performance summary.

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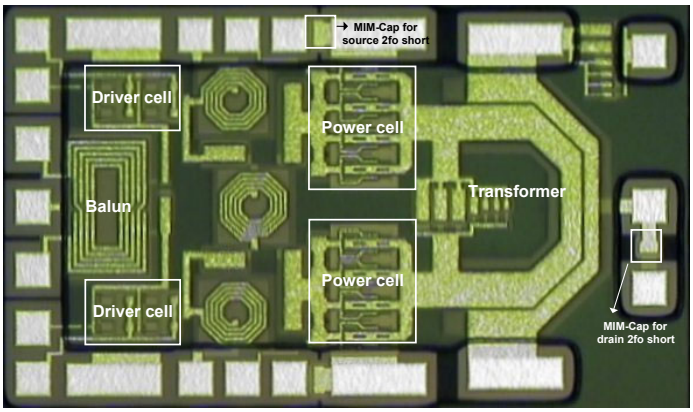

Figure 11.9.6: Chip micrograph (1x1.7 mm^2).

