# Fully Integrated Doherty Power Amplifiers for 5 GHz Wireless-LANs

Daekyu Yu[1], Young-woong Kim[2], Kichon Han[3], Jin-ho Shin[2], and Bumman Kim[1]

[1] Department of Electrical Engineering, Pohang University of Science and Technology, Gyeongbuk, 790-784, Republic of Korea
[2] XRONet Corporation, Bundang, Gyeonggi, 463-020, Republic of Korea
[3] Future Communication Integrated Circuit Inc., Bundang, Gyeonggi, 463-020, Republic of Korea

***Abstract* — Fully integrated Doherty amplifiers have been developed for 5 GHz wireless-LAN (WLAN) applications. Through a new Doherty power amplifier circuit topology, the bulky Doherty in/output matching block including quarter-wave (λ/4) impedance transformer can be fully integrated using capacitors, short micro-strip lines and bonding wires. To improve efficiency at a full power, without using the bulky input power splitter, a new input power driving concept is implemented by inserting λ/4 impedance transformers at the inputs of the carrier and peaking amplifiers using the lumped elements. The amplifier based on InGaP HBT technology, shows an output power of 22.5 dBm and a power-added efficiency (PAE) of 21.3 % at an error vector magnitude (EVM) of 5 %, measured with 54 Mbps 64-QAM-OFDM signals at 5.2 GHz. The proposed in/output matching topology allows the fully integrated Doherty amplifiers with a small size.**

## I. INTRODUCTION

Linearity is one of the most important figures of merit for power amplifiers of wireless communication system. To meet the stringent requirements for the linearity, the power amplifiers are usually biased at the class A or AB mode. However, these modes cause a low efficiency. In addition, 802.11a and 802.11g WLAN systems adopt orthogonal frequency division multiplexing (OFDM) modulation providing high-speed data rate and robustness to narrow band fading and interference. However, the OFDM signal, which is a multi-carrier modulation, has a large peak-to-average-power-ratio (PAPR). Due to the high PAPR of OFDM signal, the power amplifiers have to operate at a large amount (usually about 6 dB) of back-off out power from 1 dB gain compression point ($P_{1dB}$) to achieve the linear operation, which further degrades the overall efficiency. Therefore the efficiency of the power amplifier has become an important issue for mobile communication terminals because it determines the battery lifetime.

There are many efficiency enhancement techniques at the low/average power region such as power amplifier employing DC-DC converters [1] and switched gain stage power amplifiers with bypass power stage [2]. However, these techniques need additional components such as DC-DC converters or switches, which result in a significant increase of the module size/cost and power loss that make the power amplifiers not suitable for fully integrated power amplifiers. The gain fluctuation of the switched amplifier may not be suitable for the OFDM signal.

The load modulation scheme, which is described by Doherty, is a simpler circuit than the others, and the most promising solution for the handset applications [3]-[5]. Unlike the base station application, it is still big challenges to be integrated in a small size. The first problem is λ/4 impedance transformer for load modulation. Nowadays, many published papers show the transformer can be replaced by π-type L-C lumped components [6]. But size and loss problems especially due to large inductor, are still burdens. The second one is the bulky 3 dB hybrid coupler generally needed for power dividing in the input circuit [7].

In this paper, we present a fully integrated Doherty power amplifier for the 5 GHz (IEEE 802.11a) band WLANs. We introduce a new amplifier circuit topology with fully integrated in/output matching components including the λ/4 impedance transformer at the second section. At the next section, a new input power dividing concept in Doherty power amplifiers to obtain a high efficiency at a full power region, is discussed. And then, RF measurement results by using 54 Mbps 64-QAM-OFDM signals at 5.2 GHz are presented. Finally, summary of this work is followed.

## II. DESIGN DESCRIPTION FOR A FULLY INTEGRATED-DOHERTY PA

### *A. Doherty Circuit Topology Description for Miniaturization*

Many published papers show that the λ/4 impedance transformer for load modulation can be replaced π-type L-C lumped components. But for full integration on MMIC chip, the size and loss problems especially due to large

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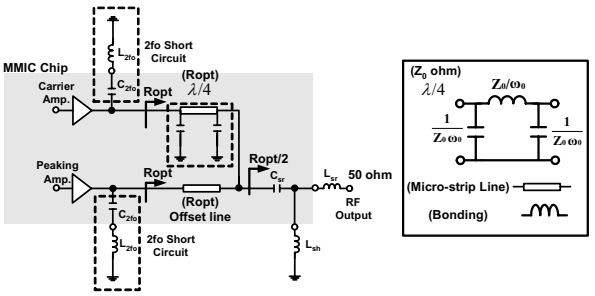


Fig. 1. Schematic diagram of the new Doherty output matching circuit for miniaturization

inductor are still burdens. Therefore, we need a new circuit topology for implementation of fully integrated Doherty power amplifiers.

In a π-type equivalent lumped circuit of the transformer, the inductance is in proportion to characteristic impedance ($Z_o$). Therefore, it is preferred to match the output load impedance from 50 Ω to a suitably low value $R_{opt}/2$ for a low $Z_o$. In case of the $R_{opt}$ of 5.8 Ω and center-frequency ($f_o$) of 5.2 GHz, the inductance in π-type equivalent lumped circuit is reduced to 0.17 nH and can be replaced by a micro-strip line with 200~300 μm length on MMIC chip. To prevent the power leakage into off-state peaking amplifier in low power ranges, the output impedance of the peaking amplifier should be transformed to nearly open using another offset line [9], [10]. Because the characteristic impedance of offset line is the optimum load impedance ($R_{opt}$), the offset line can be easily integrated on MMIC chip, too.

Additionally, a simple and small sized second harmonic termination circuit is realized with integrated MIM capacitors and bonding wires at the end of the carrier and peaking amplifier collectors. The bonding wires for the resonance at $2f_o$ can be tuned by adjusting the length of the wires.

A schematic diagram of the new Doherty output matching circuit with miniaturization of the transformer is shown in Fig. 1. The output matching circuit consists of MIM capacitors ($C_{sr}$ and $C_{2fo}$) on the MMIC chip and bonding wires ($L_{sh}$, $L_{sr}$, and $L_{2fo}$) connecting MMIC chip with a PCB module substrate [8]. The bonding wires are used as inductors, whose size, cost and loss are far better than those of on-chip spiral inductors and micro-strip transmission lines on PCB substrates. Thus, the chip size can be small and efficiency is high.

*B. New Uneven Power Drive in Doherty PA*

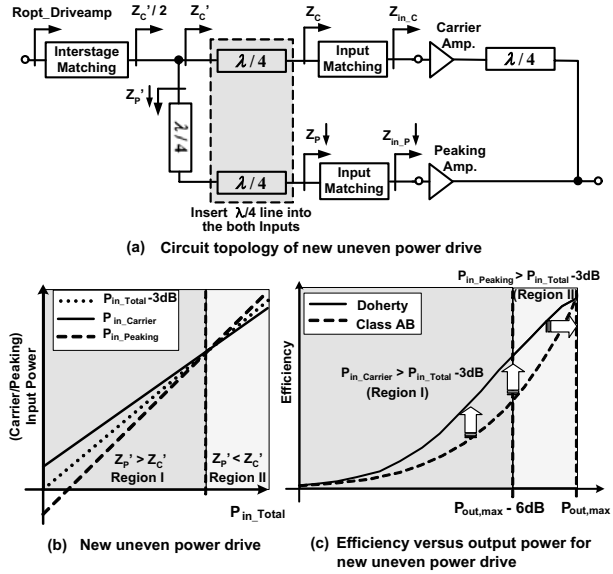


Fig. 2. New uneven power drive concept in the handset Doherty power amplifiers.

In this section, we discuss how to divide input power for the carrier and peaking amplifiers effectively without using a bulky 3 dB hybrid coupler or power divider. Similarly to the output matching topology, the optimum load impedance of the drive amplifier ($R_{opt\_Driveamp}$) is transformed to a low impedance of $Z_C'/2$ at the carrier and peaking amplifier split point through the interstage matching circuit. Because $Z_C'$ is pretty low value, we can implement the λ/4 delay line of peaking amplifier on MMIC chip. Also this input matching topology reduces the match circuit loss. In conventional interstage matching circuit of Doherty power amplifier using a λ/4 delay line with $Z_o$=50 Ω, $R_{opt\_Driveamp}$ is matched to 25 Ω and the input impedance of power cell ($Z_{in\_C}$ or $Z_{in\_P}$) to 50 Ω through the interstage matching and input matching circuits, respectively. Matching circuit loss is burden because the impedance transform range is wide. On the other hand, the proposed input matching topology reduces power loss, especially inductor loss owing to replacement of spiral inductors by micro-strip lines at the interstage matching and input matching circuits of the power stage.

Because the peaking power cell has been biased lower than the carrier one, the current level of the peaking cell at the maximum input drive can not reach the maximum allowable current level. Thus, the load impedances of both cells can not be fully modulated to the optimized impedances. As a result, the conventional Doherty power amplifier has been heavily saturated, and it degrades linearity and produces far less power. In our earlier work,

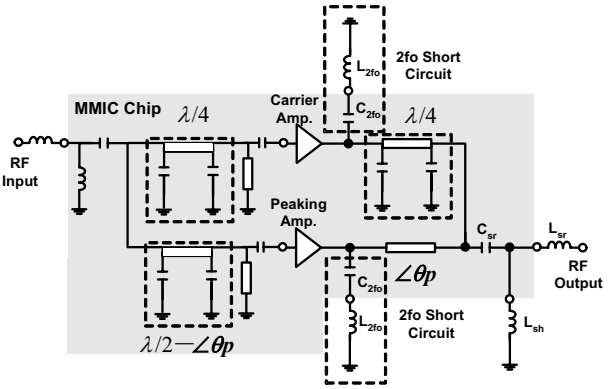


Fig. 3. Simplified schematic circuit diagram of Doherty power amplifiers for the 5 GHz WLANs.

we propose the *uneven power driving* for base station power amplifiers application [11], applying more power to the peaking power cell. In the drive, the peaking cell is opened fully and the load impedances are modulated completely. The concept can be applied for Doherty amplifier for the mobile application with suitable modification for the small chip design. Because of applying less power to carrier power cell, it leads to not only power gain loss but also reduce efficiency at low and medium power levels. So we propose a *new uneven power driving* concept in Fig. 2 (b). At a low or medium power level, the more power is applied to the carrier power cell for the increase a power gain and efficiency. On the other hand, the more power is applied to the peaking power cell at a high power to reach the maximum allowable current level of the cell.

The *new uneven power drive* can be achieved without using bulky 3 dB hybrid coupler or power divider. The input impedance of the carrier power cell ($Z_{in\_C}$) does not change considerably according to the input power level. On the other hand, the input impedance of the peaking power cell ($Z_{in\_P}$) decreases considerably as the input power increases due to the self biasing effect. We can utilize the effect. In conventional Doherty topology, due to the λ/4 delay line in front of the peaking amplifier, the impedance of the peaking amplifier increases as the power level increases. Therefore, a less power is delivered to the peaking amplifier. To solve the problem, we insert λ/4 impedance transformers at the in ports of the carrier and peaking amplifiers as shown in Fig. 2 (a). As the input power level becomes higher, more input power is applied to the peaking power cell and less to the carrier.

A simplified schematic circuit diagram of the Doherty power amplifier with *new uneven power driving* is shown in Fig. 3.

## III. FABRICATION AND EXPERIMENTAL RESULTS

The commercial 2μm InGaP/GaAs HBT foundry is employed to fabricate the MMIC chip. The emitter size of each InGaP/GaAs HBT is 2 μm x 20 μm x 2 fingers (unit cell). To obtain an output power of more than 28 dBm, 32 unit cells are employed for the output stages of carrier and peaking power amplifiers, respectively.

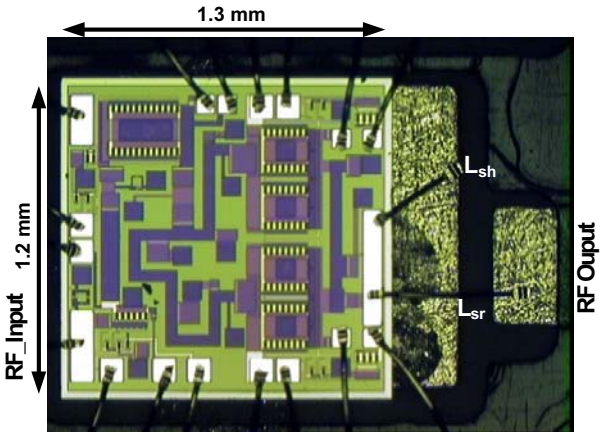


Fig. 4. Photograph of fully integrated Doherty power amplifiers with bonding wires.

Fig. 4 shows a photograph of the fully integrated Doherty power amplifier module consisting of an HBT MMIC with 3-stage HBT power amplifier and bonding wires. The MMIC chip area is 1.2 mm x 1.3 mm. To verify the chip, an evaluation board is fabricated using TMM6 PCB with relative permittivity ($\varepsilon_r$) of 6 and the MMIC chip is directly mounted on the ground plate of the evaluation board. The output matching circuit consisting of capacitors and micro-strip lines and bonding wires enables the miniaturization of the power amplifier module size as small as 3 mm x 3 mm.

Fig. 5 shows the power measurement results of the fabricated amplifier with 54 Mbps 64-QAM-OFDM signal at 5.2 GHz and supply voltage $V_{CC}$ of 3.3 V. The quiescent currents of the 1st, 2nd derive amplifiers, and carrier amplifier are 10, 36, and 50 mA, respectively. From the figure, $P_{1dB}$ and power gain of the fabricated power amplifier is 28.4 dBm and 21.5 dB, respectively. The PAE at $P_{1dB}$ is 29.5 %. At an EVM of 5 %, PAE of 21.3 % and an output power $P_{out}$ of 22.5 dBm are achieved. We estimate the performance at Class AB operation by adjusting the peaking amplifier bias equal to

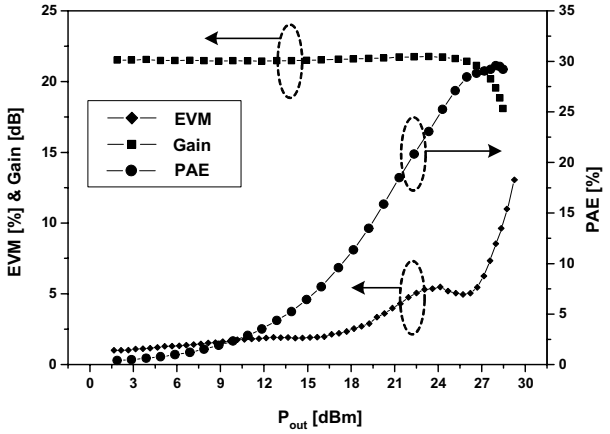


Fig. 5. Measured power characteristics of the fabricated Doherty power amplifiers with 54 Mbps 64-QAM-OFDM signals at 5.2 GHz.

the carrier amplifier one. The PAE at an output power $P_{out}$ of 22.5 dBm is 16.6 %, which is an 4.7 % improvement. In the amplifier, RF power gain of the power stage in Doherty action, is very low, about 6 dB. As the RF power gain of power stage is increased, the PAE of Doherty power amplifier can be improved further.

## IV. CONCLUSIONS

A fully integrated Doherty power amplifier for the 5 GHz (IEEE 802.11a) band WLANs is developed using a InGaP/GaAs HBT process. This circuit integrates all components including λ/4 impedance transformer into MMIC chip and bonding wires are used for output matching components and harmonic controlling components. The simple and small sized second harmonic termination is realized with integrated MIM capacitor and bonding wire at the collector. The new input power driving concept in Doherty power amplifiers is adopted to obtain enhanced efficiency at a full power region. The proposed topology allows fully integrated Doherty power amplifiers. The measured data show that Doherty power amplifier is a fully compliant candidate with high speed data communication systems covering the OFDM systems.

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## REFERENCES

[1] P. M. Asbeck, L. E. Larson, and I. G. Galton, "Synergistic Design of DSP and Power Amplifier for Wireless Communications," *IEEE Trans. Microwave Theory and Tech.*, vol. 49, no. 11, pp. 2163-2169, November 2001.

[2] J. Staudinger, "Applying Switched Gain Stage Concepts to Improve Efficiency and Linearity for Mobile CDMA Power Amplification," *Microwave Journal*, vol. 43, no. 9, pp.152-162, September 2000.

[3] W.H. Doherty, "A New High Efficiency Power Amplifier for Modulated Waves," *Proc. IRE*, vol. 24, no. 9, pp. 1163-1182, September 1936.

[4] J. Jung, U. Kim, J. Jeon, J. Kim, K. Kang, and Y. Kwon, "A New "Series-Type" Doherty Amplifier for Miniaturization," *2005 IEEE RFIC Symp., Dig.*, pp. 259-262, June 2005.

[5] J. Nam, J. Shin, and B. Kim, "A Handset Power Amplifier With High Efficiency at Low Level Using Load-Modulation Technique," *IEEE Trans. Microwave Theory and Tech.*, vol. 53, no. 8, pp. 2639-2644, August 2005.

[6] C. Tongchoi, M. Chongcheawchamnan, and A. Worapishet, "LUMPED ELEMENT BASED DOHERTY POWER AMPLIFIER TOPOLOGY IN CMOS PROCESS," *Int. Symp. Circuit and Systems '03, Proc.,* vol. 1, pp. I-445 – I-448, May 2003.

[7] M. Iwamoto, A. Williams. P. F Chen, A. G. Metzger, L. E. Larson, and P. M. Asbeck, "An Extended Doherty Amplifier With High Efficiency Over a Wide Powe Range," *IEEE Trans. Microwave Theory and Tech.*, vol. 49, no. 12, pp. 2472-2479, December 2001.

[8] T. Oka, M. Hasegawa, K. Fujita, M. Yamashita, M. Hirata, H. Kawamura, and K. Sakuno, "Enhanced Linearity and Efficiency of HBT Power Amplifiers for 5-GHz Wireless-LANs," *2005 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 649-652, June 2005.

[9] Y. Yang, J. Yi, Y.Y. Woo, and B. Kim, "Optimum Design for Linearity and Efficiency of Microwave Doherty Amplifier Using a New Load Matching Technique," *Microwave Journal,* vol. 44, no. 12, pp. 20-36, December 2001.

[10] Y. Yang, J. Cha, B. Shin, and B. Kim, "A Fully Matched N-way Doherty Amplifier with Optimized Linearity," *IEEE Trans. Microwave Theory and Tech.*, vol. 51, no. 3, pp. 986-993, March 2003.

[11] J. Kim, J. Cha, I. Kim, and B. Kim, "Optimum Operation of Asymmetrical-Cells-Based Linear Doherty Power Amplifiers Uneven Power Drive and Power Matching," *IEEE Trans. Microwave Theory and Tech.*, vol. 53, no. 5, pp. 1802-1809, May 2005.