

# Postech activities on CMOS based Linear Power Amplifiers

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## Abstract

As the proliferating wireless personal communication systems require multi-function capability with miniaturization, the CMOS process, which has the merit of high level integration, becomes the technology of choice for the solution. Due to the recent improvement of CMOS technology, the multi-function RF transceivers, including the base-band and IF blocks, could be integrated in a single chip. There's no exception at the territory of GaAs based PA. Over recent several years, the switching-type PA has been evolved into the form of single-chip around GSM/GPRS communication systems, and by releasing the data about overcoming ruggedness and reliability problem under extreme condition, it is expected to rise a storm up to the PA market. In this talk, we present the contents from the basic designing methods of linear CMOS PA, to the first demonstration of single-chip CMOS PA and advanced Doherty CMOS PA with ultra high PAE. Unlikely to the switching-type CMOS PA, there's not much of knowledge or optimization method for the linear CMOS PA design and such a poor environment makes the designing of linear CMOS PA thought to be a difficult field.

In the first part, the CMOS linearity is analyzed with Volterra analysis and essential linearization techniques for the CMOS PA are presented. Especially, deteriorate effects of bond wire inductance is newly expounded and effective method to eliminate the effect is suggested under fully differential circuit condition. For the verification of the linearity improvement, a fabricated fully differential 0.18  $\mu\text{m}$  CMOS PAs are presented and linearization effects are explained by comparing the IMDs and EVM of IEEE 802.11g signal.

The second part introduces the linearity improvement technique by adopting a DNW (Deep N-well) structure on a NMOS and its reasons are expounded. Since the DNW is known to improve the device isolation and RF performances, most of the recent sub-micron CMOS foundries provide the process. For the verification of the linearity improvements by the DNW, the fabricated 0.18  $\mu\text{m}$  CMOS PAs of single-ended and fully-differential types are presented and their linearity improvements are compared.

In the third part, the first demonstration of 3.3 V operating single-chip CMOS PA is introduced. For a high voltage operation with sub- $\mu\text{m}$  NMOS, the new self-biased cascode configuration is adopted. To obtain a high PAE of differential PA, the integration of the output transformer with low loss has been a main issue. In this part, our integrated transformer is introduced with explanation of operating principle. To show the performance of this PA, the measured results with 54 Mbps OFDM signal are shown.

The fourth part introduces the highly efficient Doherty CMOS PA for 2.4 GHz WLAN. Since the Doherty PA can improve the PAE at the medium power level, such technique is very useful for the CDMA or WCDMA systems which require the high PAE at the medium power level. Further more, this technique can provide the high PAE and good EVM simultaneously for a PA amplifying OFDM signal. This work suggests the lumped component conversions with transmission lines such as quarter-wave transformer and input offset line, whose method can be adopted for the full-integration of the CMOS Doherty PA and save the fabrication cost.

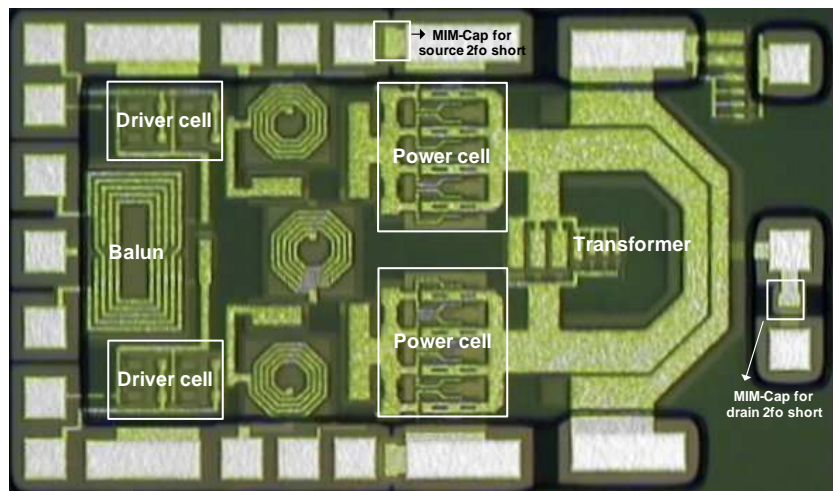


Fig. 1. Chip photo.

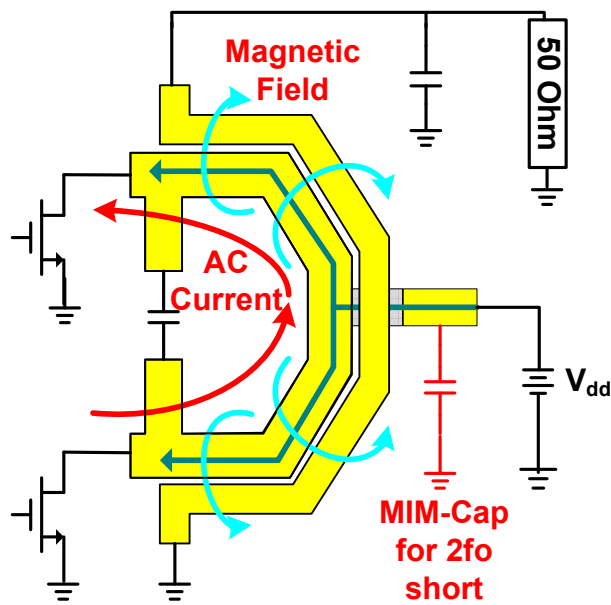


Fig. 2. Chip photo.