

# Microwave Doherty Power Amplifier for High Efficiency and Linearity

(Invited Paper)

Bumman Kim, Jangheon Kim, Ildu Kim, Jeonghyeon Cha, and Sungchul Hong

Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH),  
Pohang, Gyeongbuk, 790-784, Republic of Korea  
E-mail : bmkim@postech.ac.kr

**Abstract**— This paper explains the basic circuit configuration of microwave Doherty amplifier and additional design methods for wide bandwidth and high power applications. This paper also presents the recent experimental results of our group using the uneven power drive. Most of the previous works about microwave Doherty amplifier have employed identical input drives. In this works, two 1:1(2-way) and a 1:2(3-way) Doherty amplifiers are implemented at 2.14GHz center frequency using LDMOS with a peak envelope power of 180 watt and 285 watt, respectively. The 2-way Doherty amplifiers are optimized at 25 watt average output power for high efficiency and linearity and the 3-way Doherty amplifier at 16 watt average output power for high linearity. The amplifiers are tested using WCDMA 4FA signal. The performances of the 2-way Doherty amplifier are compared with that of the comparable class AB amplifier and the Doherty amplifier with even power drive. The performances of the 3-way Doherty amplifier are compared with that of the comparable class AB amplifier. The experimental results show the superior performances of our Doherty amplifiers.

## I. INTRODUCTION

As the current wireless communication systems such as CDMA-2000, WCDMA, OFDM and so on, are progressed to increase a bandwidth, minimize the size, and save the cost, the thermal problem of the system and the linearity problem for wideband applications become important. The design technique of the power amplifiers with the high efficiency and linearity across the wide bandwidth has become a hot issue.

In this paper, we explain the basic circuit configuration of microwave Doherty amplifier and additional design methods for wide bandwidth and high power applications. We have summarized our recent works based on high power devices with uneven power drive for the 1:1(2-way) and 1:2(3-way) Doherty amplifiers tested using WCDMA 4FA signal. The implemented Doherty amplifiers show very good performance, demonstrating that Doherty amplifier is a promising candidate for power amplifiers with wide bandwidth, high efficiency and linearity.

## II. MICROWAVE DOHERTY AMPLIFIER

The basic operation principles of the Doherty amplifier are well described in many articles [4]- [6]. From the paper, we have seen that the advantages of the Doherty amplifier are

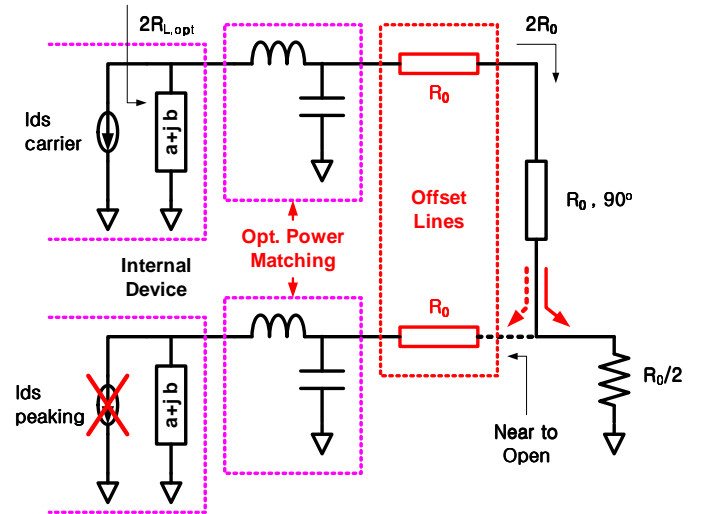


Fig. 1. Equivalent load networks at a low-power operation for the 1:1(2-way) Doherty amplifier with optimum power-matching circuits and offset lines.

the simple circuit configuration and improved efficiency. In this section, we have explained some problems to apply the Doherty technique at the microwave frequency and proposed methods to solve them.

General microwave devices suited for power amplifiers have reactive parasitic components. Due to the components, the Doherty amplifier is faced with some serious problems when the conventional load network is used. First, the output power from the carrier amplifier can leak into the peaking amplifier port at a low power level. Second, the optimum power matching impedance becomes complex and the pure resistive load modulation cannot deliver the maximum power. Finally, the ideal load modulation of  $2Z_{opt}$  to  $Z_{opt}$  cannot be achieved.

To solve the problems, we have introduced an offset line concept in our earlier works [1]- [3], [7]- [11]. Figure 1 shows the microwave version of the 1:1 Doherty amplifier. The amplifier can deliver a maximum power due to the power matching circuits. For the peaking amplifier, the output impedance seen at the output junction can be transformed

close to open by the proper length of offset line. Since the output impedance of the active device is very low resistive and strongly capacitive one, it can be rotated to a high resistive value by the offset line. Thus, the leakage power to the peaking amplifier at a low-power operation can be substantially reduced and the proper load modulation can be guaranteed.

The N-way Doherty amplifier is basically paralleling the one carrier amplifier and (N-1) peaking amplifiers, which is a simple approach to acquire an (N-1) time larger sized peaking amplifier with compared to the carrier amplifier. A schematic diagram of the N-way Doherty amplifier is shown in Fig. 3 and its basic concept is very similar to that of 1:1 microwave Doherty amplifier explained in the previous paragraph. In the ideal cases, the peak efficiency points occur at 9.5 and 12dB power back-off points for the 3- and 4-way, respectively. However, the ideal efficiency can not be achieved due to the linearity consideration [7].

The carrier and peaking amplifiers have different operating classes. The peaking amplifier is normally biased at deep class AB, B or C mode, while the bias of the carrier amplifier is set to normal class AB mode. The Doherty amplifier with this biasing strategy can deliver a high efficiency due to the low average bias current and efficient asymmetric power combination using the load modulation scheme. Additionally, the late gain expansion of the class B or C peaking amplifier can compensate for the gain compression of the class AB carrier amplifier. Due to the gain expansion and compression characteristics, the linear operation of the Doherty amplifier can be achieved [2], [3], [7].

### III. ADVANCED DESIGN METHODS OF DOHERTY AMPLIFIER

The Doherty amplifier usually has two amplifiers with identical size devices, matching circuits, and input drives. Because the peaking amplifier has been biased lower than the carrier amplifier, the current level of the peaking amplifier at the maximum input drive can not reach to the maximum allowable current level. Thus, the load impedances of both amplifiers can not be fully modulated to the optimized impedance,  $Z_{opt}$ , and they are larger than the optimum values. As a result, the conventional Doherty amplifier is heavily saturated, and it degrades linearity and produces far less power. It is also difficult to improve the linearity of Doherty amplifier across a wide bandwidth due to the memory effect. Therefore, we propose the following three design methods for wide bandwidth, high linearity, and high power applications; First, the uneven power drive, applying more power to the peaking amplifier, can open the peaking amplifier fully and modulate properly the load impedances to the optimum values. Therefore, the amplifiers with uneven power drive operate more linearly and produce more power than that with an identical input power drive, so called the even drive. Figs. 2 and 3 show schematic diagrams of the 1:1(2-way) microwave Doherty amplifier with the uneven power drive and the N-way Doherty amplifier with the uneven power drive. Second, due to the improper load modulation, the power matching circuits of both amplifiers

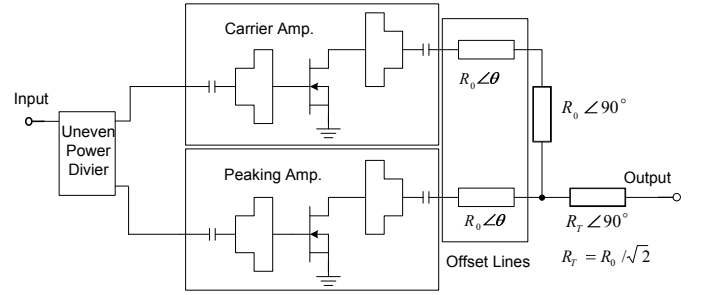


Fig. 2. Schematic diagram of the 2-way Doherty amplifier with uneven power drive.

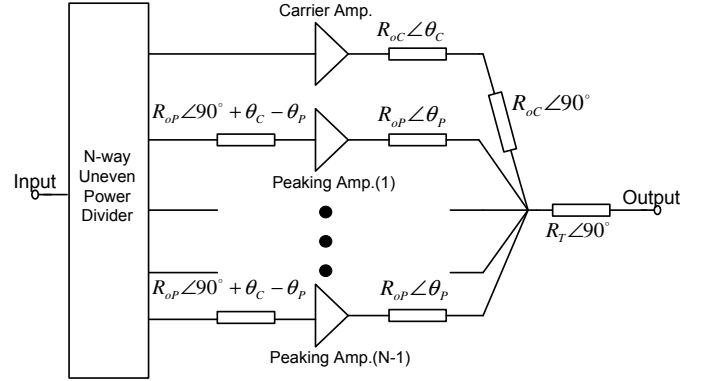


Fig. 3. Schematic diagram of the N-way Doherty amplifier with uneven power drive.

should be appropriately designed to have low load impedances for better linearity. Because of the low bias point of the peaking amplifier, the power matching circuit of the peaking amplifier should be designed to have lower load impedance than that of the carrier amplifier. Moreover, the matching circuits of both amplifiers should be individually optimized to enhance the IM cancellation over whole power ranges across the wideband signals [3].

Third, the bias circuit should be designed to minimize the memory effect [13] - [15]. The linearizing techniques focused on the harmonic cancellation such as Doherty amplifier and PD are restricted to a low cancellation limit because the memory effect brings about the different lower and upper spurious emissions. The bias circuit should be prevented the frequency dispersion of envelope impedance to minimize the memory effect. To reduce the memory effect, the bias circuit is optimized using a quarter-wave bias line and decoupling capacitors for each frequency. The tantalum capacitors are inserted within a quarter-wave bias line for the short at the envelope frequencies. Additionally, the biases of both amplifiers are properly adjusted to maintain the optimized linearity and efficiency.

### IV. IMPLEMENTATION AND EXPERIMENTAL RESULTS

Fig. 4 shows a schematic diagram of the implemented 2-way Doherty amplifier with uneven power drive. The 2.14 GHz Doherty amplifier is implemented using Freescale's MRF5P21180 LDMOSFET. The uneven power drive is implemented using an Anaren's 1A1305-5(5 dB directional coupler)

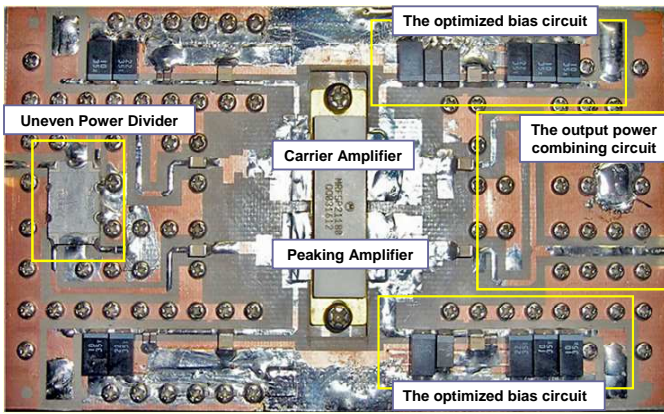


Fig. 4. A photograph of the 2-way Doherty amplifier with uneven power drive.

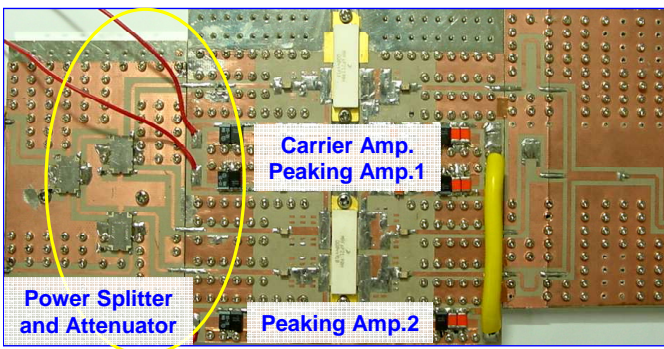


Fig. 5. A photograph of the 3-way Doherty amplifier with uneven power drive.

which delivers 4 dB more input power to the peaking amplifier than the carrier amplifier. The individual matching of the Doherty amplifier is further optimized to achieve high efficiency and linearity at 25 W(44 dBm) average output power. In the experiments, the suitable offset line is  $80.4^\circ$ , and the transformed output impedance is  $502 \Omega$ . Quiescent biases for the carrier amplifier and peaking amplifier are set to  $V_C = 3.938 \text{ V}$  (1.1 A) and  $V_P = 1.713 \text{ V}$  at  $V_{DD} = 27 \text{ V}$ , respectively.

We optimize the bias circuit to minimize the memory effect and improve the linearity and efficiency. The drain bias circuit is incorporated by a quarter-wave line and several decoupling capacitors with 10 pF for the RF and 22 uF, 10 uF, 1 uF, 1 nF, 150 nF for the envelope frequency. The tantalum capacitors(22 uF, 1 uF) located within a quarter-wave bias line are especially important to minimize the memory effect, while the impedance at the RF is reduced by these capacitors. Thus, we have optimized the bias circuit along with the matching circuit considering these effects. As a result, the bias circuit becomes an active matching circuit. For the performance comparison in terms of power drive, we also fabricate Doherty amplifier with even power drive, and the amplifier is optimized using the individual matching and bias circuit to get the linearity and efficiency as high as possible.

Fig. 5 shows a schematic diagram of the implemented 3-way Doherty amplifier with uneven power drive. The 2.14 GHz Doherty amplifier is implemented using Freescale's

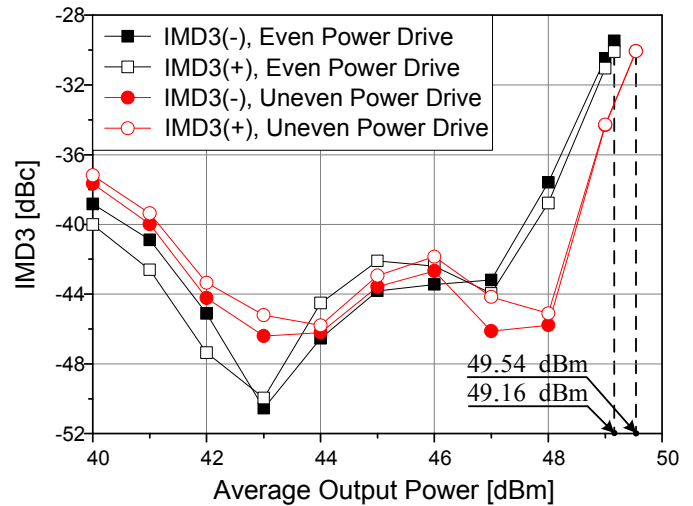


Fig. 6. Two-tone measurement results of the 2-way Doherty amplifier with even and uneven power drives.

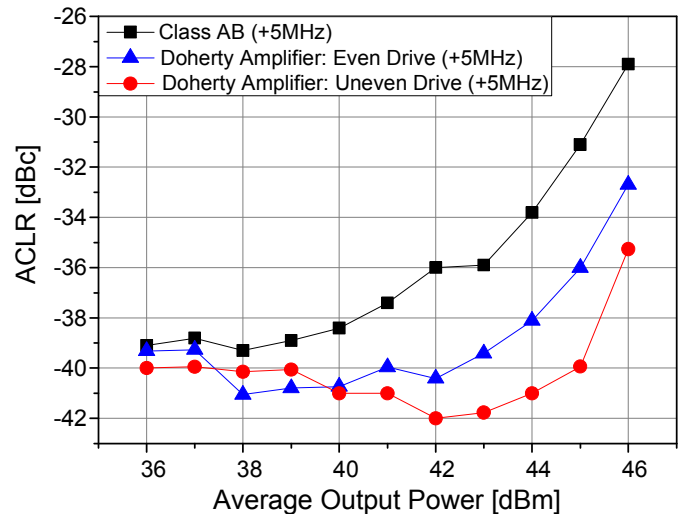


Fig. 7. Measured ACLR performance of the 2-way Doherty amplifier with even and uneven power drives and class AB push-pull amplifier for WCDMA 4FA signal.

MRF6P21190 LDMOSFETs. The 95W power cell of the push-pull configuration has been used as a carrier amplifier, and the other device's two 95W power cells have been used as peaking amplifiers in sequence. Hybrid couplers and  $\pi$ -attenuator at the input of the carrier amplifier are employed to create the uneven power drive, and the suitable offset line is  $83.5^\circ$ . The optimized quiescent bias points of the amplifier are 2.1A, 0.29A, and 0.12A, respectively. We also optimize the bias circuit to minimize the memory effect and improve the linearity. The 3-way Doherty amplifier is optimized to satisfy the high linearity characteristic without extra linearization circuits while maintaining the drain efficiency.

Fig. 6 shows the measured IMD3 of the 2-way Doherty amplifier with even and uneven power drives for a two-tone signal. We measure a peak envelope power(PEP) using two-tone signal with 1 MHz tone spacing. The PEP of the amplifier with uneven drive is improved by 15 W, from 165 W to 180 W,

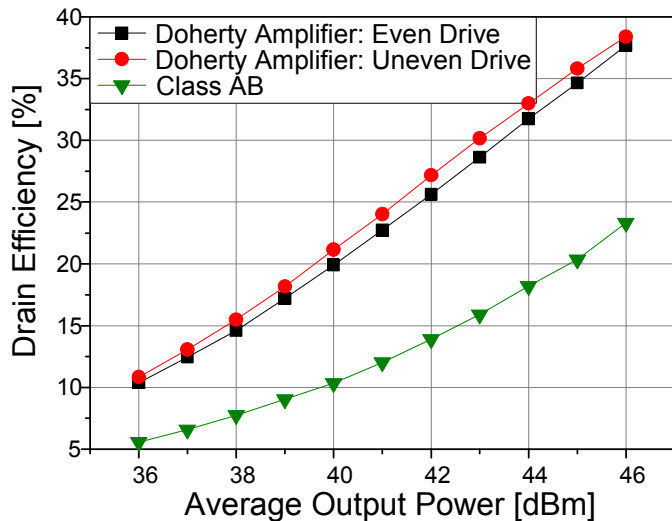


Fig. 8. Measured drain efficiency of the 2-way Doherty amplifier with even and uneven power drives and class AB push-pull amplifier for WCDMA 4FA signal.

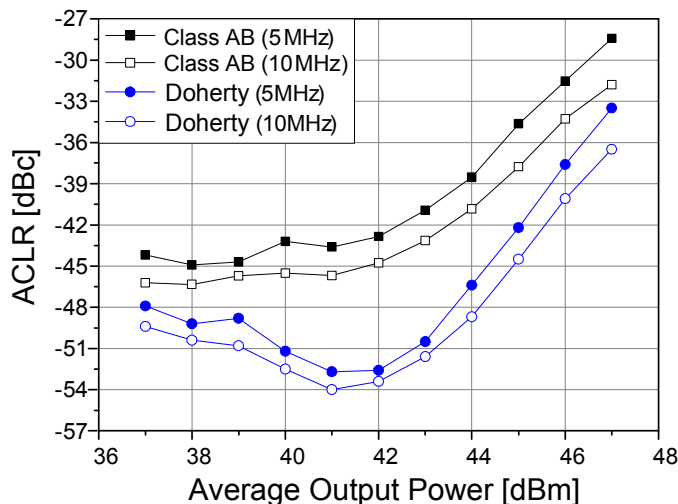


Fig. 9. Measured ACLR performance of the 3-way Doherty amplifier and class AB amplifier for WCDMA 4FA signal.

compared to the even case. This result implies that the Doherty amplifier with uneven power drive generates full power from both amplifiers.

Fig. 7 shows the measured ACLR's of the 2-way Doherty amplifier for the even and uneven cases, and class AB push-pull amplifier. the ACLR of the Doherty amplifier with uneven drive is improved by 3 dB compared to the Doherty amplifier with even drive at the average output power of 44 dBm. Fig. 8 shows the drain efficiencies of the 2-way Doherty amplifier with even and uneven power drive, and class AB push-pull amplifier for WCDMA 4FA signal. The drain efficiency of uneven case is slightly improved over the even case.

Fig. 9 shows the measured ACLR's of the 3-way Doherty amplifier with uneven drive and class AB amplifier. In comparison with the class AB amplifier, the Doherty amplifier delivers significantly improved ACLR performance, by 9.5 dB at the average output power of 42 dBm.

## V. CONCLUSIONS

In this paper, we explain the basic circuit configuration of microwave Doherty amplifier and additional design methods for wide bandwidth and high power applications. We have implemented two 1:1(2-way) and a 1:2(3-way) high power Doherty amplifiers with uneven power drive at 2.14GHz using Freescale's MRF5P21180 and MRF5P21190 LDMOSFETs, respectively. The 2-way Doherty amplifier has ACLR of -41 dBc and the drain efficiency of 33 % at average output power of 44 dBm, and the 3-way Doherty has ACLR of -52.5 dBc and fair efficiency at average output power of 42 dBm.

These experimental results clearly demonstrate the superior performance of the microwave Doherty amplifier. It is clearly show that the microwave Doherty amplifier technique is a promising candidate for power amplifiers of base station or repeater systems.

## ACKNOWLEDGEMENT

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