A Fully Matched N-Way Doherty Amplifier With Optimized Linearity

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***Abstract*—This paper presents a new fully matched N-way Doherty amplifier. The basic principles of operation and important features are described. For the experimental verification, 2.14-GHz Doherty amplifiers having two-, three-, and four-way structures are implemented using silicon LDMOSFETs and tested using down-link WCDMA signal. The linearity performances of the two-, three-, and four-way Doherty amplifiers are optimized for better *efficiency versus linearity* by a bias adjustment of the peaking amplifiers. For simultaneously improving the efficiency and linearity to achieve maximum *efficiency versus linearity*, the gate biases of the peaking amplifiers for the N-way Doherty amplifier are optimized. As a result, the *efficiency versus linearity* characteristics are drastically improved by N-way extension of the Doherty amplifier.**

***Index Terms*—Adjacent channel leakage ratio (ACLR), efficiency, linearity, microwave Doherty amplifier, power amplifiers, WCDMA.**

I. Introduction

THE base-station power amplifiers for CDMA applications, such as IS-95 series, CDMA-2000, WCDMA, and so on, generally have a critical system requirement for high linearity, but the efficiency is not specified. General power amplifiers for base stations have a very low efficiency because they must achieve the required high linearity by operating with over 10 dB backed off due to a high peak-to-average ratio (around 10 dB), additional linearization circuits, and complex control circuits. Therefore, overheating becomes an important consideration regarding reliability and cost. Conventional efficiency-boosting techniques, such as the Kahn technique, dynamic envelope tracking, or the linear amplification using nonlinear components (LINC) technique, may not be easily implemented to CDMA base stations since they can degrade the linearity, raise the cost, or provide only a very narrow bandwidth. However, the Doherty amplifiers have a definite capability to improve the efficiency and potential capability to improve linearity using very simple and low-cost RF circuits [1].

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Many previous works have analyzed or practically realized the microwave Doherty amplifier [2]–[11]. However, there are some problems that limit the microwave Doherty amplifier for use as power amplifiers of commercial wireless communication systems. The only resistive matching method using bulky two-sections of quarter-wave transformers has been implemented for the output of the Doherty amplifier [2] and is not the optimum power matching for a complex device impedance. Against general expectations, linearity is degraded instead of enhanced [3]. Though there are a few linearization results using the Doherty amplifier [2], [4]–[6], the mechanism of linearization and how to optimize linearity have not been fully described as of yet. For CDMA base-station power amplifiers, linearity is the most critical specification. Therefore, efficiency enhancement using the Doherty technique should be performed without degrading the linearity characteristics. To improve the *efficiency versus linearity* characteristics, a new load modulation topology to enhance efficiency has been implemented, using optimum output power matching circuits assisted by offset lines [7], and a linearity enhancement technique has been incorporated by cancelling the intermodulations from the carrier and peaking amplifiers [8].

In this paper, we propose a new N-way generalization method of the microwave Doherty amplifier to further enhance output performances. The N-way Doherty amplifier is basically paralleling one carrier amplifier and $N-1$ numbers of the peaking amplifiers, which is the simple approach to acquire an $N-1$ times larger-sized peaking amplifier compared with the carrier amplifier. We will present the basic circuit configuration and operation principle including efficiency and linearity improvement mechanism using the N-way Doherty technique. Using the load network with optimum output power-matching circuits, offset lines, and bias optimization, the amplifiers can deliver their maximum output power with improved efficiency and linearity. For verification and comparison, the two-, three-, and four-way Doherty amplifiers have been implemented at 2.14-GHz band and tested using a down-link WCDMA signal. To maximally achieve the *efficiency versus linearity* measure, linearity has been extensively optimized and compared for each way of the Doherty amplifiers. The measured results have also been compared with class-AB biased amplifiers as their counterparts.

II. Operation Principles of N-Way Doherty Amplifier

A. Load Modulation

Load modulation can be analyzed using ideal current sources. Fig. 1 shows an operational diagram to analyze the load mod-

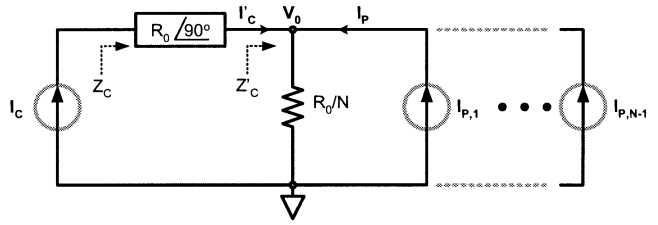


Fig. 1. Operational diagram of the N-way Doherty amplifier.

ulation characteristics for the N-way Doherty amplifier. Ideal ac current sources of $\mathbf{I_C}$ and $\mathbf{I_{P,1}}, \ldots, \mathbf{I_{P,N-1}}$ are deployed to express one carrier amplifier and $N-1$ numbers of the peaking amplifiers, respectively. The current sources in phasor form are resolved into

$$\mathbf{I_C} = I_C \cdot \cos(\omega_0 t) = I_C \angle 0^\circ \tag{1}$$

$$\mathbf{I_{P,n}} = I_{P,n} \cdot \cos(\omega_0 t - 90^\circ) = I_{P,n} \angle -90^\circ \tag{2}$$

where n is an integer from 1 to $N-1$ for the N-way case. The phase difference of -90° between the carrier source ($\mathbf{I_C}$) and the peaking sources ($\mathbf{I_{P,n}}$) is adopted in order to compensate for the phase shift caused by the quarter-wave transformer.

Next, the node voltage $\mathbf{V_0}$ as a phasor notation across the load resistor R_0/N can be easily calculated as

$$\begin{aligned}\mathbf{V_0} &= \frac{R_0}{N}\left(\mathbf{I}'_C + \sum_{n=1}^{N} \mathbf{I}_{P,n}\right) \\ &= \frac{R_0}{N}\left(I_C \angle -90^\circ + \sum_{n=1}^{N} I_{P,n} \angle -90^\circ\right).\end{aligned} \tag{3}$$

The load impedance viewed from the quarter-wave transformer and its transformed impedance viewed from the carrier current source are consequently derived as follows:

$$Z'_C = \frac{\mathbf{V_0}}{\mathbf{I'_C}} = \frac{R_0\left(I_C + \sum_{n=1}^{N} I_{P,n}\right)}{N \cdot I_C} \tag{4}$$

$$Z_C = \frac{R_0^2}{Z'_C} = \frac{N \cdot R_0 \cdot I_C}{I_C + \sum_{n=1}^{N} I_{P,n}}. \tag{5}$$

If we use the same sized and simultaneously controlled peaking current sources, (5) can be further simplified as

$$Z_C = \frac{N \cdot R_0 \cdot I_C}{I_C + (N-1) \cdot I_P}, \qquad 0 \le I_P \le I_C \tag{6}$$

where I_P is the current amplitude of the peaking current sources.

From (6), the load impedance of the N-way Doherty amplifier can be modulated as a function of the number of ways and the current supply of the peaking amplifiers. For low-power operations ($I_P = 0$), the load impedance becomes $N \cdot R_0$. For high-power operations ($I_P = I_C$), the load impedance becomes R_0. For medium-power operations ($0 < I_P < I_C$), the load impedance transits from $N \cdot R_0$ to R_0.

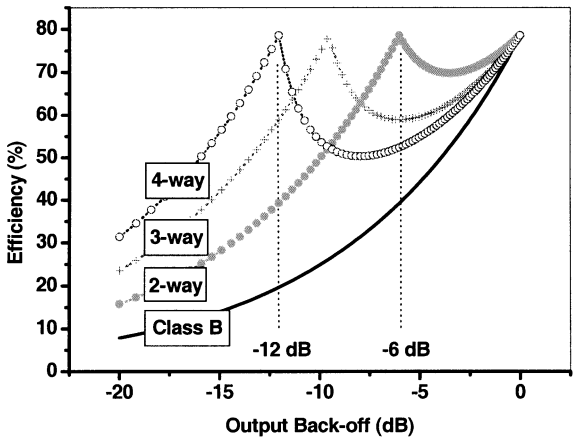


Fig. 2. Ideal efficiencies of the N-way Doherty amplifiers.

B. Efficiency

The ideal efficiency of the Doherty amplifier for the class-B carrier and peaking amplifiers was already derived by Raab [9]. The ideal efficiency of the N-way Doherty amplifier for the class-B carrier and peaking amplifiers can be easily formulated by modifying Raab's as

$$\eta = \begin{cases} \dfrac{\pi}{4} \cdot \dfrac{N \cdot v_0}{v_{\max}}, & 0 \le v_0 < \dfrac{v_{\max}}{N} \\ \dfrac{\pi}{4} \cdot \dfrac{N \cdot \left(\dfrac{v_0}{v_{\max}}\right)^2}{(N+1) \cdot \left(\dfrac{v_0}{v_{\max}}\right) - 1}, & \dfrac{v_{\max}}{N} \le v_0 < v_{\max} \\ \dfrac{\pi}{4}, & v_0 = v_{\max} \end{cases} \tag{7}$$

where $v_{\max}$ and v_0 are the maximum output voltage and an output voltage for a given power level, respectively.

Fig. 2 shows the calculated efficiencies of the two-, three-, and four-way Doherty amplifiers and the normal class-B amplifier. Another peak efficiency point occurs at 6- and 12-dB output backoff points for the two- and four-way cases, respectively. In spite of the well-shaped efficiency curves of the N-way Doherty amplifiers, it is very difficult to achieve ideal efficiency due to the previously mentioned linearity consideration.

C. Linearity

To realize the ideal Doherty amplifier system, a very complex control system may be required to obtain proper gm profiles for the carrier and peaking amplifiers [9], [11]. However, much research has tried to realize the Doherty amplifier using a simple bias arrangement for the carrier and peaking amplifiers. The on/off transient of the peaking amplifier for different modes of operation can be continuously self-adjusted by the large gain expansion characteristics of the general class-B or class-C amplifiers through output power levels, while the carrier amplifier is biased at class-A or class-AB operation [2]–[8]. In this case, the nonlinear output current of the active devices can be approximately expressed using Taylor series expansion by

$$I_{\text{out}} = gm_1 \cdot v_i + gm_2 \cdot v_i^2 + gm_3 \cdot v_i^3 + \cdots \tag{8}$$

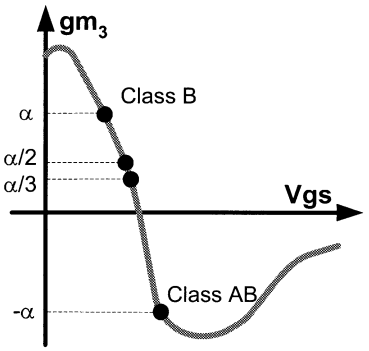


Fig. 3. Large-signal gm_3 curve versus gate biases for general FETs.

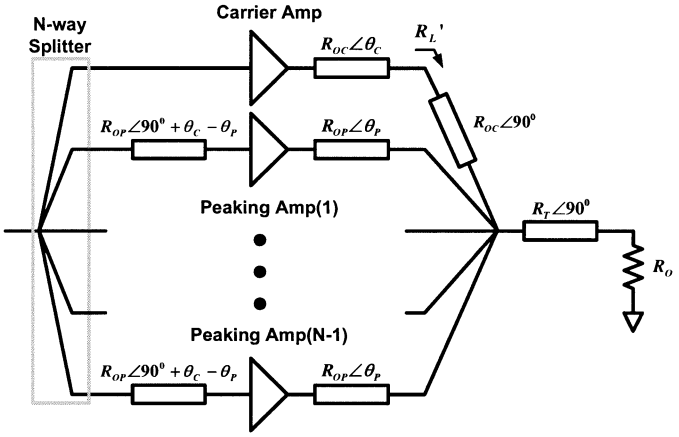


Fig. 4. Schematic diagram of the N-way Doherty amplifier.

where v_i is an input voltage and gm_X's are the Xth-order expansion coefficients of the nonlinear transconductance. The third-order intermodulation distortion (IMD3) current is mainly generated by the $gm_3 \cdot v_i^3$ term of (8).

The IMD3 generated by the carrier and peaking amplifiers can be cancelled by selecting proper gate biases for the two amplifiers. Fig. 3 presents the large-signal third-order transconductance coefficient (gm_3) curve through the gate bias level for general FETs [12]. If we assume that the load modulation does not seriously affect linearity, and that the carrier amplifier is biased as class AB to have gm_3 of $-\alpha$, as shown in Fig. 3, the bias of the peaking amplifier for the two-way Doherty amplifier should be adjusted to have gm_3 of α to perfectly cancel the IMD3 current generated by the carrier amplifier. However, the bias point of the peaking amplifier for a perfect IMD3 cancellation may approach closely to class-B bias, and the peaking amplifier may generate a considerable amount of higher order intermodulation terms, such as fifth, seventh, ninth, and so on.

For the three- or four-way cases, which have two or three peaking amplifiers, the biases of the peaking amplifiers to have perfect IMD3 cancellation should be adjusted near to the points having gm_3 of $\alpha/2$ or $\alpha/3$, respectively. Therefore, the expected optimum bias levels of the peaking amplifiers for the multiway cases become higher than that of the two-way case, and the peaking amplifiers operate more linearly without excessively generating higher order distortion terms. By contrast, the higher biases for more than three-way Doherty amplifiers to optimize linearity reduce the load modulation range and resultant efficiency improvement of the Doherty amplifier. Consequently, for the design of CDMA base-station power amplifiers, the best *efficiency versus linearity* characteristics should be considered.

III. Realization of Linear Amplifier Based on Doherty Concept

A. N-Way Realization

The realization of the N-way Doherty amplifier is another important issue. A schematic diagram of the N-way Doherty amplifier is shown in Fig. 4. The N-way Doherty amplifier is composed of an N-way power splitter/combiner, fully power matched amplifiers for the carrier and peaking amplifiers, offset lines, and quarter-wave transformers. In our earlier paper s[7], [8], we used identical amplifiers with full output power matching circuits and their respective offset lines for the carrier and peaking amplifiers.

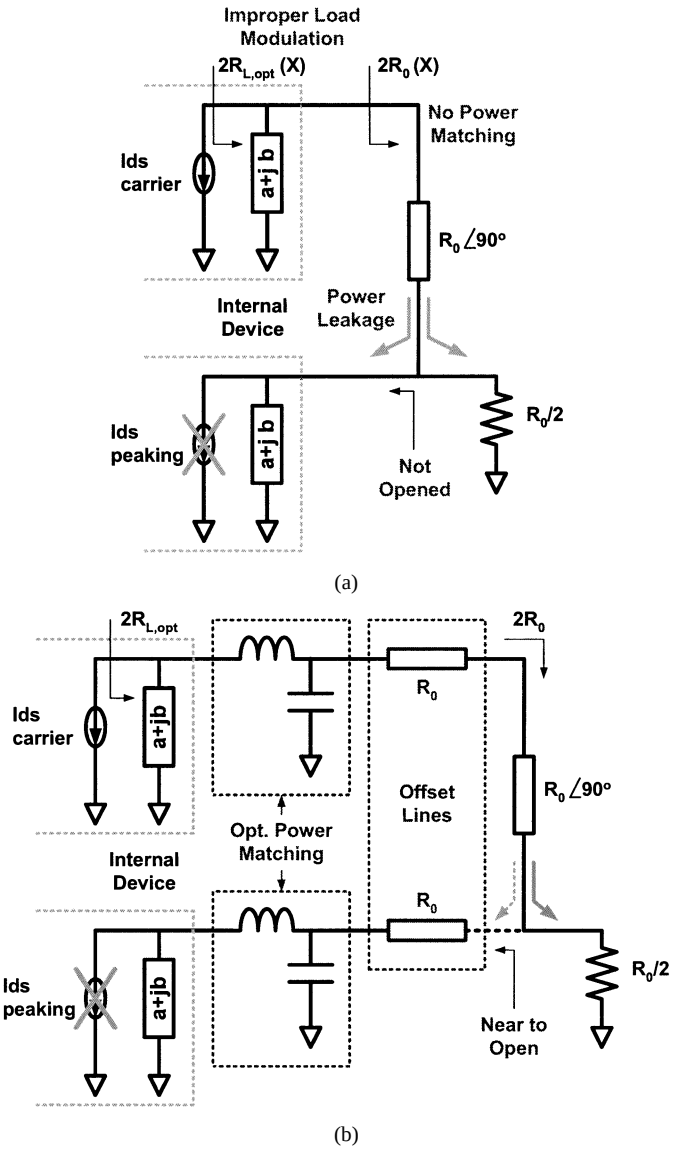


Fig. 5. Equivalent-load networks at a low-power operation for: (a) the conventional Doherty amplifier and (b) the two-way Doherty amplifier with optimum power-matching circuits and offset lines.

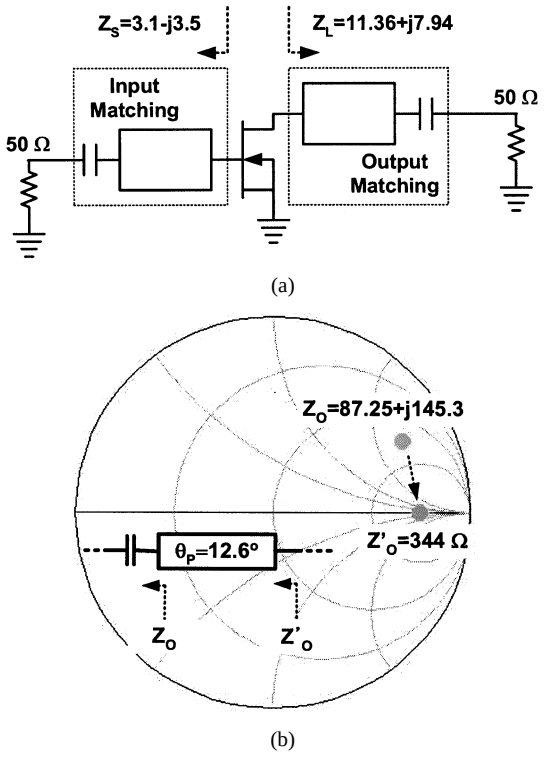


Fig. 6. (a) Schematic diagram for the designed amplifier cell. (b) Output impedance transformation with an offset line for the peaking amplifier.

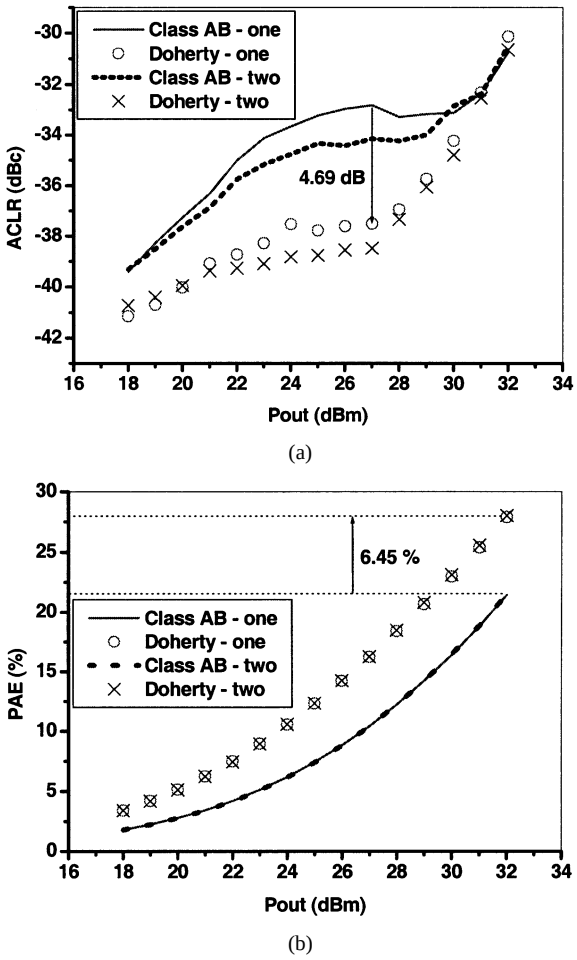


Fig. 7. Measured performances of the two-way Doherty and class-AB amplifiers with one- and two-carrier down-link WCDMA signals. (a) ACLRs. (b) PAEs.

In Fig. 4, the carrier and peaking amplifiers are matched at full power levels to the characteristic impedances R_{0C} and R_{0P}, respectively. The lowered impedance due to N-way combining is transformed to $R_0\ \Omega$ load impedance using an output quarter-wave transformer. The characteristic impedance of the output impedance transformer should be

$$R_T = \sqrt{\frac{R_{0P} \cdot R_{0C}}{R_{0P} + (N-1) \cdot R_{0C}} \cdot R_0}. \tag{9}$$

For $R_0 = R_{0C} = R_{0P} = 50\ \Omega$, the impedance R_T is further simplified to be $50/\sqrt{N}$.

The load impedance seen at the offset line of the carrier amplifier is modulated by the current supply of peaking amplifiers. At a low-power mode, where the peaking amplifier is completely turned off, the load impedance becomes

$$R'_{L,\text{low}} = \frac{R_{0P} \cdot R_{0C} + (N-1) \cdot R_{0C}^2}{R_{0P}}. \tag{10}$$

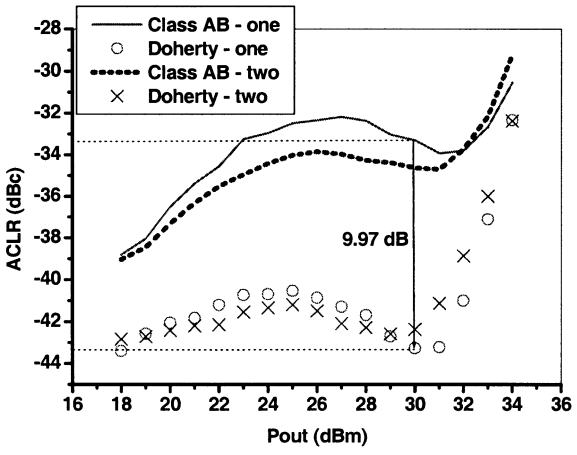
If we let $R_0 = R_{0C} = R_{0P} = 50\ \Omega$ again, the load impedance seen at the offset line is further simplified to $N \cdot 50$ at a low-power mode, while the load impedance at a high-power mode is still $50\ \Omega$.

B. Power-Matched Load-Modulation Circuit Design

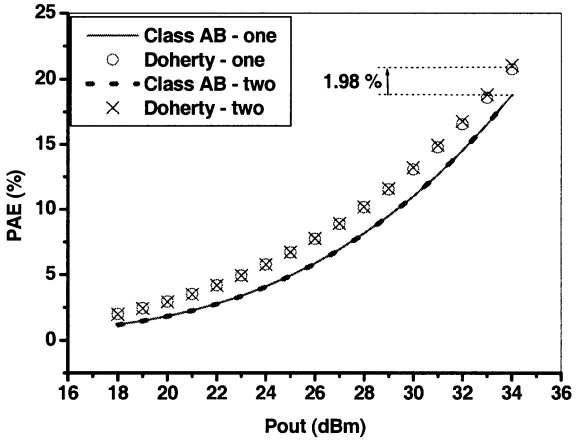
To achieve the load modulation described using (10), the peaking amplifiers at a low-power mode should be turned off and open circuited at the output junction. General microwave devices suited for the power amplifiers have large shunt capacitances, feedback capacitances, and pad or package parasitics. These reactive components render the output impedance of the device strongly reactive with low resistance. Due to the low and complex output impedance of the peaking amplifier, a considerable power leaks from the carrier amplifier to the peaking amplifier, causing improper load modulation.

Fig. 5 illustrates equivalent-load networks including a simplified equivalent circuit of active devices at a low-power operation for the conventional Doherty amplifier [see Fig. 5(a)] and the two-way case among the proposed N-way Doherty amplifiers [see Fig. 5(b)]. As shown, the equivalent-output circuit of the active device can be expressed as an ideal current source whose shunt termination has an impedance of $a + jb$.

The internal shunt circuit creates serious problems with the operation of the Doherty amplifier with a conventional load network, as shown in Fig. 5(a). First, the output power from the carrier amplifier can leak into the peaking amplifier port at a low-power level, which leads to efficiency degradation. Second, the optimum power matching impedance becomes complex and the pure resistive load modulation cannot deliver a proper power match. Finally, an ideal load modulation cannot be achieved. If the peaking amplifier is not opened due to the internal component of $a + jb$ at a low power level, the load impedance seen at the output of the carrier amplifier is not $2R_0$. The actual load impedance seen at the current source of the amplifier is deviated by the shunt component of $a + jb$.

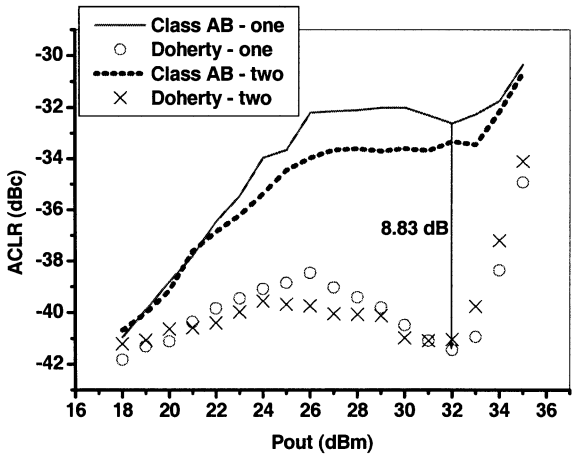


(a)

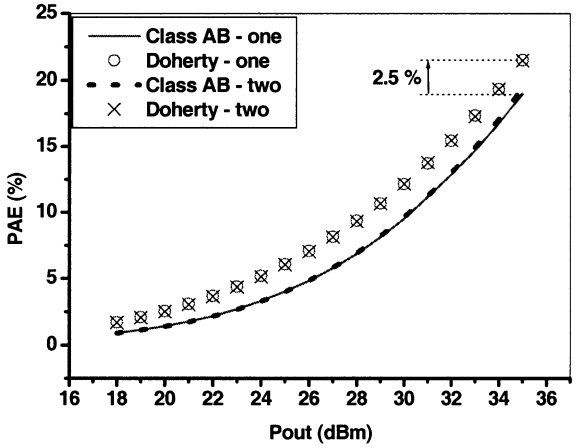


(b)

Fig. 8. Measured performances of the three-way Doherty and class-AB amplifiers with one- and two-carrier down-link WCDMA signals. (a) ACLRs. (b) PAEs.



(a)



(b)

Fig. 9. Measured performances of the four-way Doherty and class-AB amplifiers with one- and two-carrier down-link WCDMA signals. (a) ACLRs. (b) PAEs.

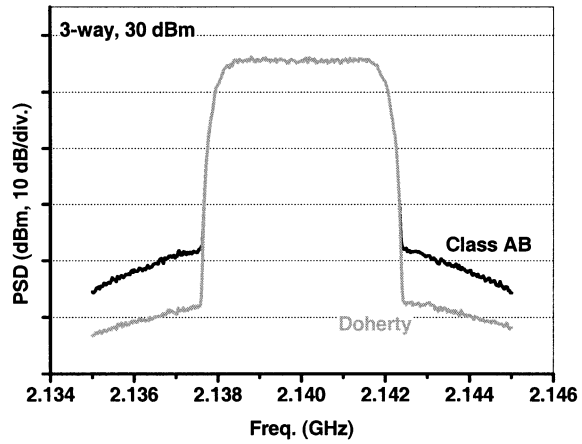
Those problems can be totally eliminated by the load network shown in Fig. 5(b). For the peaking amplifier, the output impedance seen at the output junction can be transformed close to open by using power matching circuits at a high power level and the proper length of offset line. Since the output impedance of the active device is very low resistive and strongly capacitive, it is rotated to a high-resistive value by the offset line. Hence, the power leakage to the peaking amplifier at a low-power mode can be substantially blocked, which guarantees a proper load modulation with the load impedance of $2R_0$ seen at an offset line of the carrier amplifier. The impedance $2R_0$ seen at an offset line can be transformed to be $2R_{\mathrm{L,opt}}$ at the current source of the carrier amplifier inside of the power matching circuit by a proper length of offset line. Note $2R_{\mathrm{L,opt}}$ is twice that of the optimum load impedance ($R_{\mathrm{L,opt}}$) seen at the internal current source at a high-power level. Consequently, proper load modulation can be achieved.

IV. Design and Experiments

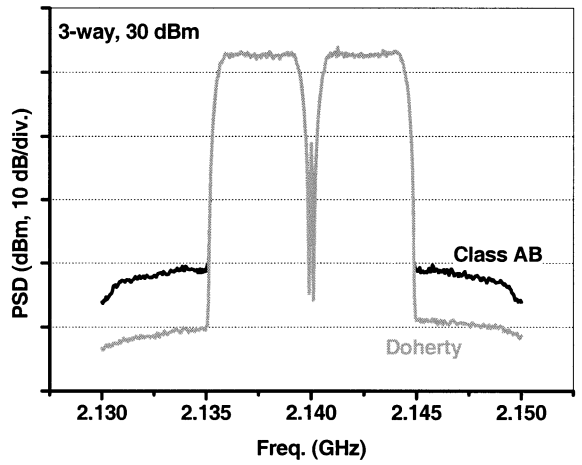
To investigate the linearity and efficiency of the N-way Doherty amplifier, the two-, three-, and four-way Doherty amplifiers were implemented and compared for their performances. The basic amplifier cell has been designed using Motorola's 4 W-PEP silicon LDMOSFET for the carrier and peaking amplifiers. Fig. 6(a) shows a schematic diagram of the class-AB amplifier with optimized input and output matching circuits to have a maximum output power at a certain linearity (-30 dBc of adjacent channel leakage ratio (ACLR) in this experiment). The amplifier was tuned to have the best performance with deep class-AB operation for better efficiency.

A proper length of offset line for the peaking amplifier can be easily determined using the measured output impedance. Fig. 6(b) shows the process to determine the proper offset line of the peaking amplifier. The measured output impedance (denoted by Z_O) of the peaking amplifier with class-B bias can be transformed to be highly resistive value with an appropriate offset line (12.6° in this experiment). The transformed output impedance of Z_O' becomes 344 Ω, which is high enough to block the output power leakage to the peaking amplifier at a low-power operation. Similarly, given the impedance transformation operation explained in the final paragraph of Section III, the length of the offset line for the carrier amplifier is determined to be the same as that for the peaking amplifier.

The linearity was optimized using bias adjustment of the peaking amplifier for the implemented two-, three-, and



(a)



(b)

Fig. 10. Measured power spectral densities of the three-way Doherty and class-AB amplifiers with: (a) one- and (b) two-carrier down-link WCDMA signals.

four-way Doherty amplifiers. The efficiency can be automatically improved due to the load modulation principle. The class-AB amplifiers can be achieved with just AB biasing the all-unit cells of the Doherty amplifiers. Fig. 7(a) shows the measured ACLRs of the two-way Doherty and class-AB amplifiers at offset 2.5 and 5 MHz for one- and two-carrier down-link WCDMA signals, respectively. For the one-carrier WCDMA signal, ACLR is improved by 4.69 dB at output power of 27 dBm. Fig. 7(b) shows the measured power-added efficiencies (PAEs) of the two-way Doherty and class-AB amplifiers for one- and two-carrier down-link WCDMA signals. The PAE is improved by 6.45%, from 21.45% to 27.9% at an output power of 32 dBm. The optimized quiescent current of the peaking amplifier becomes 0.1 mA, while those of the carrier amplifier and the class-AB amplifiers are set to 60 mA.

Fig. 8(a) shows the measured ACLRs of the three-way Doherty and class-AB amplifiers. For the one-carrier WCDMA signal, ACLR is improved by 9.97 dB at output power of 30 dBm. Fig. 8(b) shows the measured PAEs of the three-way Doherty and class-AB amplifiers. The PAE improved slightly by 1.98% at output power of 34 dBm. Fig. 9(a) shows the measured ACLRs of the four-way Doherty and class-AB amplifiers. For the one-carrier WCDMA signal, ACLR is improved by 8.83 dB at output power of 32 dBm. Fig. 9(b) shows the measured PAEs of the four-way Doherty and class-AB amplifiers. The PAE is improved by 2.5% at output power of 35 dBm. The optimized quiescent currents of the peaking amplifiers are 12.8 and 15.73 mA for the three- and four-way cases, respectively. Fig. 10 shows the measured power spectral densities of the three-way Doherty and class-AB amplifiers at output power of 30 dBm for one- and two-carrier WCDMA signals, which show the best linearity improvement. As shown in Fig. 10, the out-of-band spectrum emission levels were drastically reduced by the Doherty combining technique, in addition to efficiency enhancement.

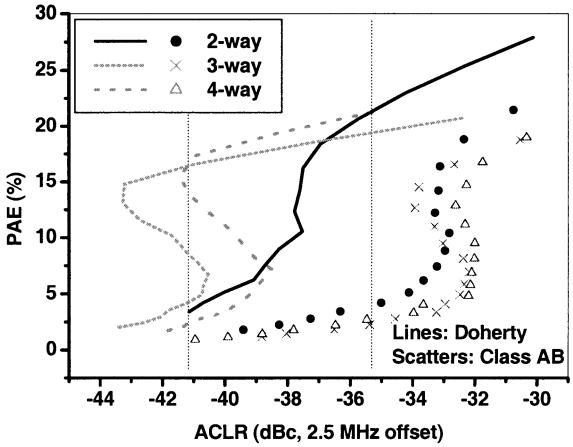


Fig. 11. *Efficiency versus linearity* characteristics for the N-way Doherty and N-way class-AB amplifiers.

TABLE I
REPRESENTATIVE EXPERIMENTAL RESULTS FOR THE OPTIMIZED TWO-, THREE-, AND FOUR-WAY DOHERTY AMPLIFIERS

case	PAE(%) / ACLR(dBc)	Pout(dBm)
2-way	27.90 / -30.13	32
3-way	14.77 / -43.22	31
4-way	19.34 / -38.36	34

As predicted in Section II-C, the three- or four-way Doherty amplifiers showed a greater linearity improvement than the two-way Doherty amplifier. However, for the four-way case, linearity improvement was observed through a relatively narrow output power range compared with the three-way case, which means that the excessive numbers of the peaking amplifiers make IMD3 cancellation more sensitive. Also, as the number of peaking amplifier is increased, the bias currents of the peaking amplifiers should be raised for the intermodulation cancellation. Therefore, the efficiency improvement does not reach to the level expected in Section III-B due to a reduced load modulation.

Fig. 11 shows comparative data for *efficiency versus linearity* characteristics of the amplifiers. Compared with the normal class-AB operated amplifiers, the N-way Doherty amplifiers deliver much more improved *efficiency versus linearity*. The two-way shows best efficiency above -35 dBc of ACLR, while the three-way shows best efficiency below -41 dBc. For the intermediate region, the four-way shows slightly better efficiency than that of the three-way. Table I presents the

representative experimental results for the two-, three-, and four-way Doherty amplifiers.

V. Conclusions

For the CDMA base-station power amplifiers, an N-way extending technique of the Doherty amplifier has been proposed. The N-way technique has the capability to discretely increase the number of peaking amplifiers. The most important advantage of the N-way technique is the use of the same size devices as the carrier and peaking amplifiers, which makes the overall implementation easy and insensitive. The efficiency of the N-way Doherty amplifier has been theoretically calculated. Further, we described the linearity improvement mechanism of the Doherty amplifier using the general FETs. For practical implementation, we have employed full output power matching circuits and offset lines for the carrier and peaking amplifiers. This circuit approach solves the problem of the conventional Doherty amplifiers, such as nonoptimum power matching and possible output power leakage to the peaking amplifier at a low-power mode, and improper load modulation caused by the nonideal output impedance of the microwave devices.

For the experimental verification of the N-way Doherty amplifier and comparative investigation on linearity and efficiency improvements, the two-, three-, and four-way Doherty amplifiers have been implemented at the 2.14-GHz band. Their optimized linearity characteristics and resulting efficiencies are compared and also compared with the two-, three-, and four-way class-AB amplifiers as their respective counterparts.

The three-way shows best ACLR improvement (9.97 dB at 30 dBm) and the two-way shows best PAE improvement (6.47% at 32 dBm) at the same output power, when they have been optimized to have the best *efficiency versus linearity* measure. The optimized two- and three-way Doherty amplifiers show 27.9% of PAE at -30.13 dBc of ACLR and 14.77% of PAE at -43.22 dBc of ACLR at 2.5-MHz offset, respectively, which are state-of-the-art *efficiency versus linearity* performances for any amplifiers for the down-link WCDMA signal.

From the experimental results, the optimum topology (i.e., number of ways) can be selected according to the various purposes. Consequently, this paper has presented the N-way approach to realize the Doherty amplifier, in addition to output power matching and offset line techniques, which will provide highly cost effective and producible linearization, as well as efficiency-boosting techniques of the base-station power amplifiers for various CDMA applications.

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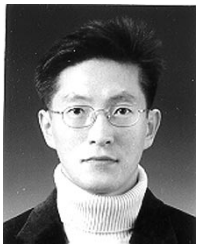

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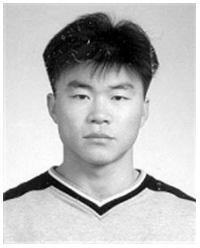

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