A Handset Power Amplifier With High Efficiency at a Low Level Using Load-Modulation Technique

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***Abstract*—A new monolithic-microwave integrated-circuit power amplifier for cellular handsets has been implemented using the load-modulation concept of the Doherty amplifier, which has a high efficiency at a low power level. In order to get a compact module, the $\lambda/4$ transmission line for the load modulation is replaced by a passive high-pass π-network, and the load-modulation circuit is also modified to function as a power-matching circuit of the main amplifier. The amplifier has two modes of operation, low- and high-power modes, controlled by a control voltage. At the high power mode, both the main and auxiliary amplifiers are operational and, at the low power mode, only the main amplifier generates output power enhancing the efficiency. For the code-division multiple-access environment, the amplifier at the low-power mode provides power-added efficiency (PAE) of 39.8% and an adjacent channel power ratio (ACPR) less than 49.8 dBc at 23.1 dBm, and the high-power mode PAE of 37.9% and ACPR of 46.4 dBc at 28 dBm. The efficiency is improved by approximately 18.8% at $P_{\rm out} = 23$ dBm by the load-modulation technique. For the advanced mobile phone system-mode operation, the amplifier delivers 26.1 dBm with PAE of 53% and 30.8 dBm with 48.7% at the low and high modes, respectively.**

***Index Terms*—Advanced mobile phone system (AMPS), cellular, code division multiple access (CDMA), Doherty amplifiers, handset, InGaP/GaAs HBT, load modulation, $\lambda/4$ transmission line, power amplifiers (PAs).**

I. Introduction

THERE ARE increasing demands on highly efficient linear amplifiers for mobile handsets. The power amplifiers (PAs) usually deliver a high efficiency only near the maximum rated power level (~28 dBm), and the efficiency drops drastically as the output power level is reduced. For the code-division multiple-access (CDMA) system, the power level for usual operation is less than 20 dBm and the PAs operate mostly at the low-efficiency region. Since the PAs in a mobile handset consume a large portion of battery power, it is desirable to have a high efficiency at the backed-off power region to extend battery lifetime [1], [9], [11].

There are many efficiency enhancement techniques at the low-power region such as Khan, envelope tracking, linear amplification using nonlinear components (LINC), and load modulation [1], [7], [10]. The load-modulation scheme, which is described by Doherty, is a simpler circuit than the others, and the most promising solution for the handset applications [1], [2], [9].

Manuscript received November 15, 2004; revised February 6, 2005. This work was supported by the Ministry of Education, Korea, under Brain Korea 21 projects.

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Digital Object Identifier 10.1109/TMTT.2005.852745

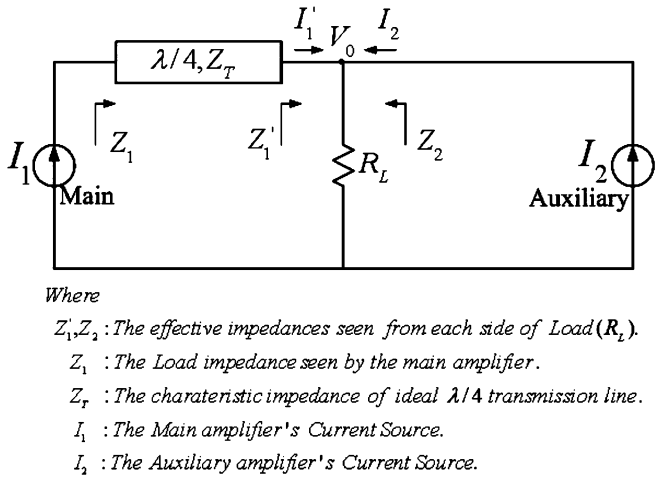


Fig. 1. Operational diagram of the load-modulation circuit.

In the load-modulation amplifier, only the main amplifier generates output at a low-power level. At a high-power level, the main and auxiliary amplifiers generate output together. Therefore, the PA delivers a high efficiency at a low-power level while maintaining a comparable efficiency at a high-power level.

The classical Doherty amplifier uses a $\lambda/4$ transmission line for the load modulation, but it is not suitable for handset amplifier application due to the large size [1], [4], [6], [8]. To apply the load-modulation technique to a handset PA, the $\lambda/4$ transmission line is replaced by a lumped *LC* π-network [4]. Based on the circuit, we have demonstrated a linear PA with a high efficiency at the back-off region using GaAs HBT technology.

II. Operation of PA Based on the Doherty Concept

Fig. 1 shows an operational diagram of the load-modulation technique suggested by Doherty. Let I_1 be the main amplifier's current source, I_2 is the auxiliary amplifier's current source, and the $\lambda/4$ transformer is an ideal $\lambda/4$ transmission line with characteristic impedance of Z_T. When both currents flow into load R_L, the effective impedances seen from each side of the load (Z_1', Z_2) and the load impedance seen by the main amplifier (Z_1) are given by

$$Z_1 = \frac{V_0}{I_1'} = R_L\left(\frac{I_1' + I_2}{I_1'}\right) = R_L(1+\alpha) \tag{1}$$

$$Z_2 = \frac{V_0}{I_2} = R_L\left(\frac{I_2 + I_1'}{I_2}\right) = R_L\left(1+\frac{1}{\alpha}\right) \tag{2}$$

$$Z_1 = \frac{Z_T^2}{Z_1'} = \frac{Z_T^2}{R_L\left(1+\dfrac{I_2}{I_1'}\right)} = \frac{Z_T^2}{R_L(1+\alpha)} \tag{3}$$

$$\alpha = \frac{I_2}{I_1'} = \frac{Z_1'}{Z_2}, \qquad \text{where } 0 \le \alpha \le 1 \tag{4}$$

When the auxiliary amplifier is turned off, i.e., $\alpha = 0$, the impedances of Z_1', Z_2, and Z_1 are given by

$$Z_{1,\alpha=0}' = R_L \quad Z_{2,\alpha=0} = \infty \quad Z_{1,\alpha=0} = \frac{Z_T^2}{R_L} \tag{5}$$

and when the auxiliary amplifier is fully turned on, i.e., $\alpha = 1$, generating a current comparable to that of the main amplifier, the impedances of Z_1', Z_2, and Z_1 are given by

$$Z_{1,\alpha=1}' = 2R_L \quad Z_{2,\alpha=1} = 2R_L \quad Z_{1,\alpha=1} = \frac{Z_T^2}{2R_L}. \tag{6}$$

From (5) and (6), we can see that the load impedance seen by the main amplifier (Z_1) and the auxiliary amplifier (Z_2) are modulated. If $Z_T = 2R_L$, the load impedance of the main amplifier is $4R_L$ when $\alpha = 0$ and the load impedances of both amplifiers are equal to $2R_L$ when $\alpha = 1$.

The power (P_0) at the load R_L is a sum of the powers from the main amplifier (P_1) and auxiliary amplifier (P_2). P_0 at $I_2 = \alpha I_1'$ is described by

$$P_0 = P_1' + P_2 = (1+\alpha)P_1, \qquad \text{where } 0 \le \alpha \le 1. \tag{7}$$

Here, we have assumed that the two current sources deliver the same maximum power.

When the auxiliary amplifier is turned off, i.e., $\alpha = 0$, the output power (P_0) is obtained from (5) and (7) as follows:

$$P_{0,\alpha=0} = P_{1,\alpha=0} = V_0^2/Z_{1,\alpha=0}. \tag{8}$$

When the auxiliary amplifier is fully tuned on and two amplifiers generate the same power, i.e., $\alpha = 1$, P_0 is given by

$$P_{0,\alpha=1} = 2P_{1,\alpha=1} = 2V_0^2/Z_{1,\alpha=1}. \tag{9}$$

From (5), (6), (8), and (9), we can describe the relationship between the output power at $\alpha = 0$ and $\alpha = 1$ as follows:

$$P_{0,\alpha=1} = 2^2 P_{1,\alpha=0}(W) \tag{10}$$

$$P_{0,\alpha=1}(\text{dBm}) = 6\text{ dB} + P_{1,\alpha=0}\,(\text{dBm}). \tag{11}$$

Equation (11) indicates that the maximum power with the auxiliary amplifier turned off is 6 dB lower than that when both the amplifiers are fully turned on. Therefore, a high efficiency at the lower power operation can be achieved by generating power from the main amplifier only with lower bias. For the high-power operation, the main and auxiliary amplifiers are higher biased, and both amplifiers generate full power. The load lines and biases of the two amplifiers are depicted in Fig. 2. For a linear operation with good efficiency, the amplifiers are biased at class AB.

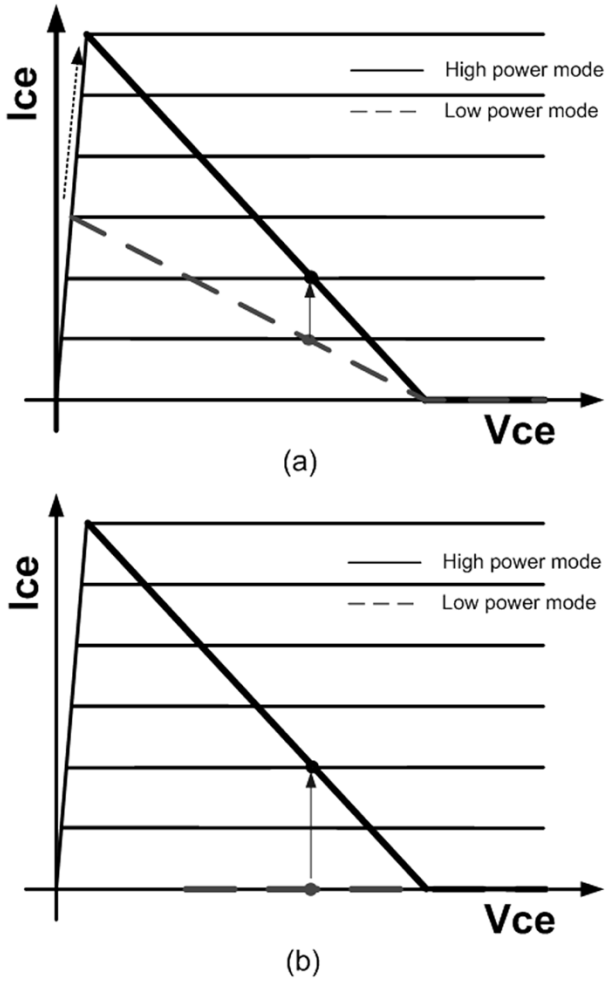


Fig. 2. Load line variations for the main and auxiliary amplifiers. (a) Main amplifier. (b) Auxiliary amplifier.

III. Implementation of the Load-Modulation PA in MMIC Form

For the conventional Doherty amplifier [4], the main amplifier needs a $\lambda/4$ line for the load modulation. The output matching network and load-modulation network are separated, and the additional matching network is needed for matching to the system impedance. However, the line is too big to be employed in a miniaturized amplifier module for a mobile handset. The line can be approximated by one of the four lumped component equivalents shown in Fig. 3 [5]. The lumped component values in this figure are given by

$$C = 1/2\pi f Z_T \text{ [F]} \tag{12a}$$

$$L = Z_T/2\pi f \text{ [H]} \tag{12b}$$

where f is frequency at which the line is $\lambda/4$ length [Hz]

$$Z_T = \sqrt{Z_L Z_S}\ [\Omega]. \tag{13}$$

In this study, the high-pass π-network is employed because the capacitor can function as a dc block and the inductor can be used for a dc bias. Due to the multiple functions of the elements, we can reduce the number of matching elements and save cost and total module size.

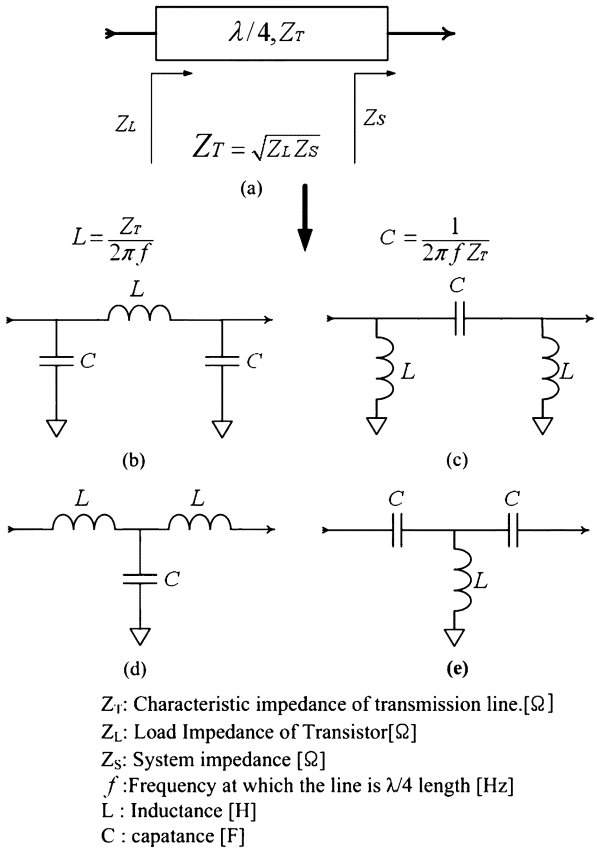


Fig. 3. Equivalent-circuit topology of $\pi/4$ transmission line using lumped elements. (a) $\pi/4$ transmission line. (b) Low-pass π-network. (c) High-pass π-network. (d) Low-pass T-network. (e) High-pass T-network.

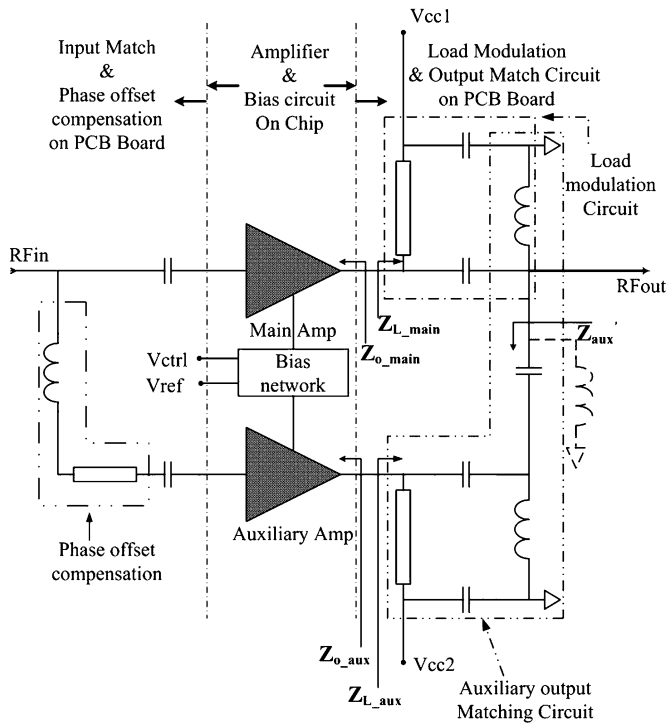


Fig. 4. Matching schematic of the load-modulation amplifier.

Fig. 4 is the matching circuit schematic of the load-modulation amplifier. The $\lambda/4$ transmission line is replaced by the high-pass π-network, but the inductor used for dc bias is replaced by a transmission line because the inductor cannot support high dc current at a high-power region. To simplify the circuit topology and miniaturize the module, the impedance levels of the main amplifier and auxiliary amplifier (Z_1', Z_2) are designed to be $2R_L = 100\ \Omega$ for $R_L = 50\ \Omega$ output load matching. One side of the high-pass π-network is designed to have $2R_L =$

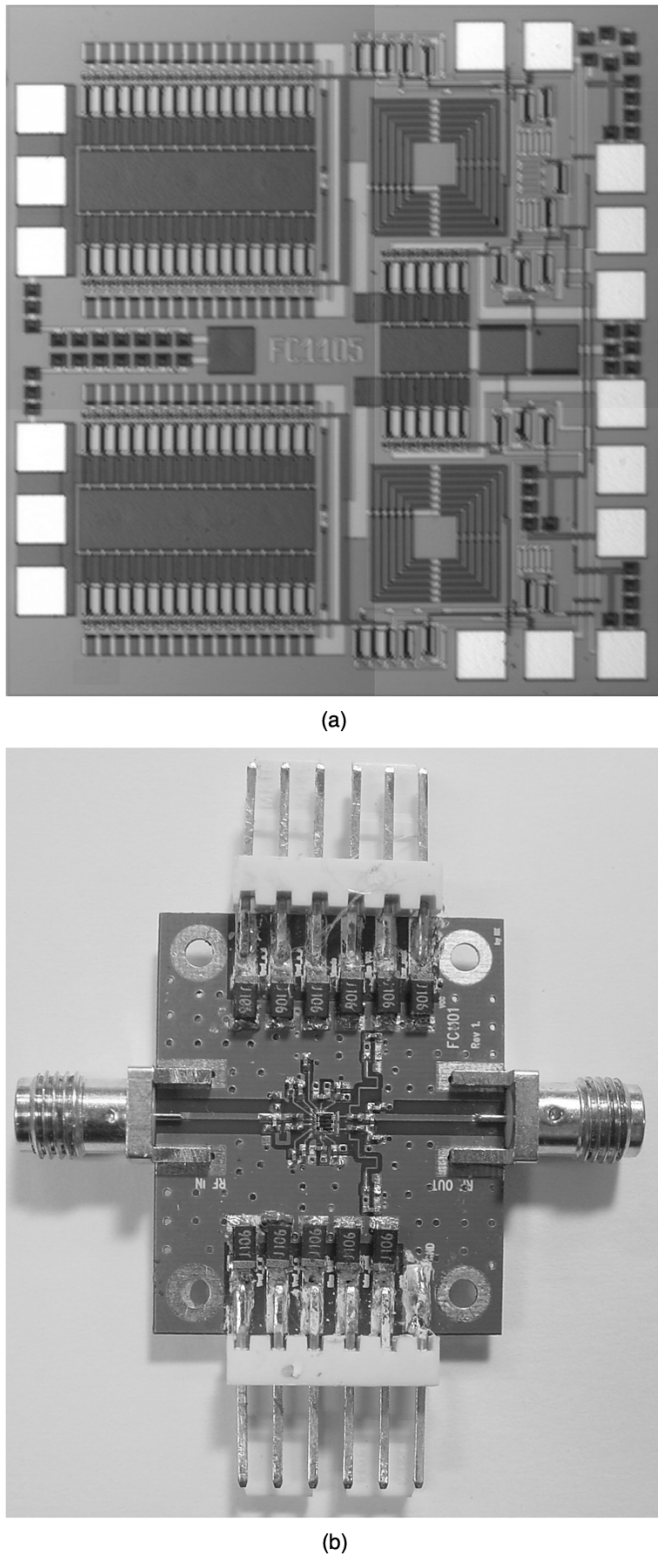


Fig. 5. MMIC chip and PCB board. (a) MMIC chip. (b) Test board module.

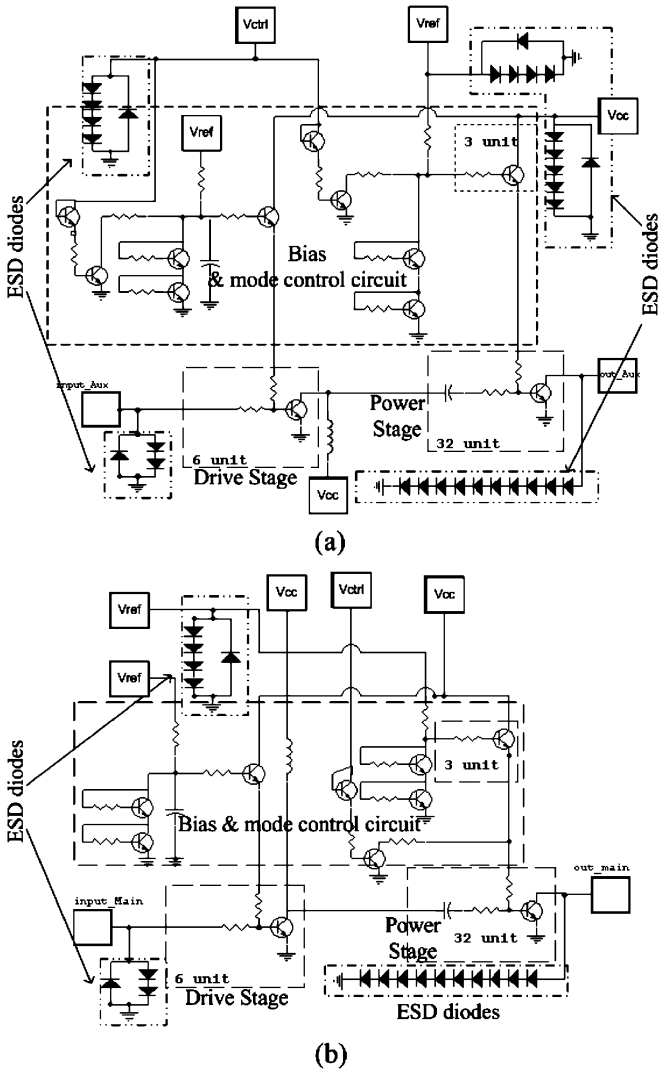


Fig. 6. Schematic for the MMIC chip of the PA. (a) Auxiliary amplifier block. (b) Main amplifier block.

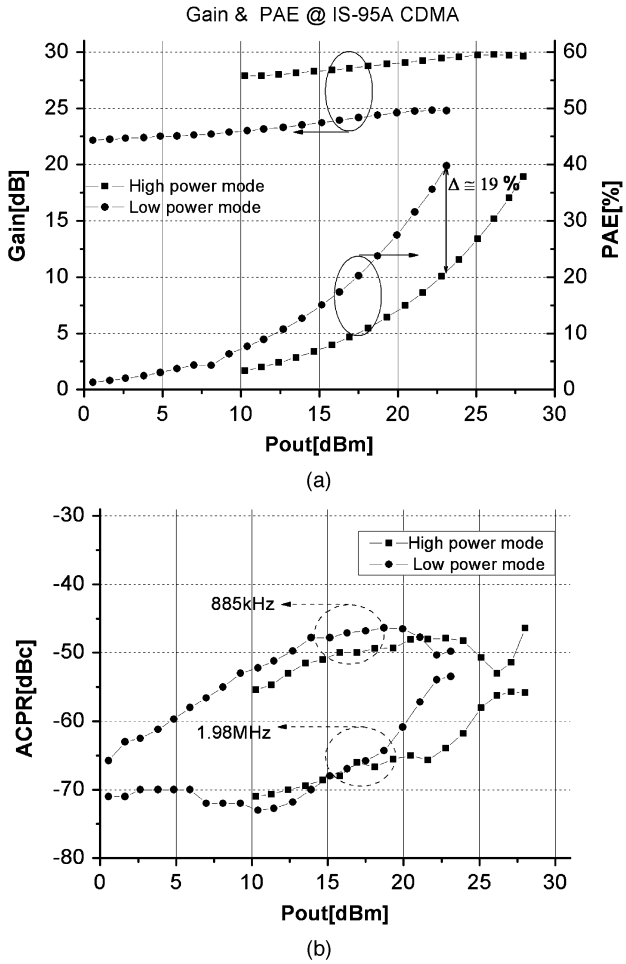
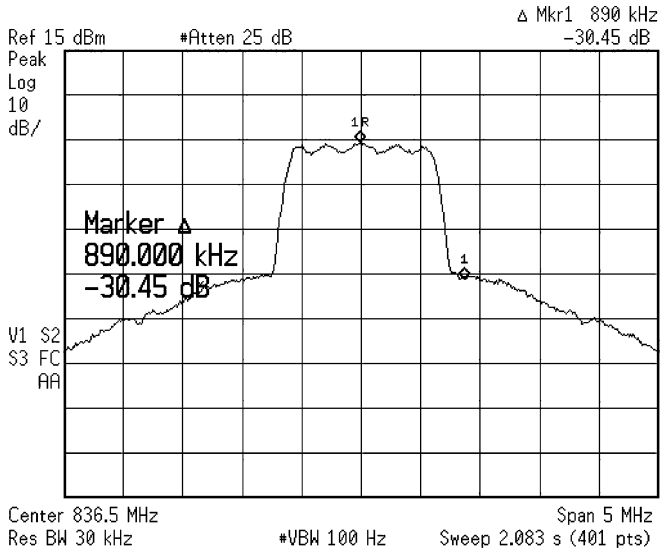


Fig. 7. RF power and linearity performances of the PA. (a) Gain and PAE for the two modes of operations. (b) ACPR at offsets of 885 kHz and 1.98 MHz.

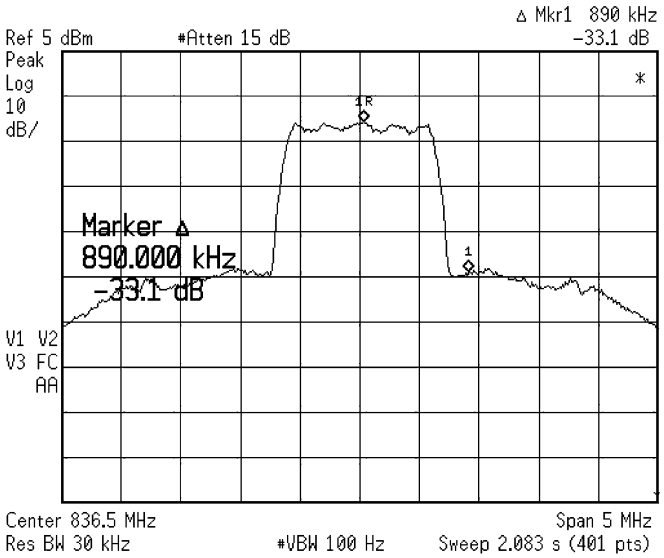
100 Ω and the other side (Z_1) is designed to have Z_{L_main} (main amp's optimum load impedance) by adjusting Z_T suitably from (13), which is unequal to $2R_L$ (system impedance). Therefore, the modulation circuit functions as a dual-purpose circuit for load modulation and power matching, miniaturizing the module. There are other important design issues for the amplifier. When the auxiliary amplifier is turned off, the output impedance (Z'_{aux}) of the auxiliary amplifier circuit should be high, close to an open circuit to prevent any power loss through the amplifier path. When the auxiliary amplifier is turned on, Z_{L_aux} should be power matched to the auxiliary amplifier and $(Z'_{\mathrm{aux}})^*$ is matched to $2R_L = 100\ \Omega$. The matching circuit of the auxiliary amplifier may need a multisection topology to satisfy the above two conditions. We have designed the off-state impedance more than 600 Ω, which is near open [3], [4]. The amplification chain paths for the main and auxiliary amplifiers have different phase delays, and the input matching networks of the two amplifiers have to compensate the phase difference. The inductor in the input network is used for the phase compensation, and the capacitor and base ballasting resistor, which are not shown in Fig. 4, are used for input matching. Since the input networks of the main and auxiliary amplifiers are parallel combined, they matched to 100 Ω, respectively, for 50-Ω input matching.

Fig. 5 shows a photograph of the monolithic-microwave integrated-circuit (MMIC) chip and module on a printed circuit board (PCB) for test. The chip is fabricated using a commercial InGaP/GaAs HBT foundry process and the chip size is as small as 1 mm × 1 mm. Fig. 6 shows the schematic of the MMIC chip, and the PA is designed for cellular and advanced mobile phone system (AMPS) band operations at 824 to 849 MHz. The amplifier has two modes of operation controlled by the bias: high-power and low-power modes. The main and auxiliary amplifiers are two stage, and the driver amplifiers of both paths consisted of 2 μm × 40 μm × 6 cells. As discussed in (11), the sizes of the power stages are equal with 2 μm × 40 μm × 32 cells to get the maximum rated powers of 22 and 28 dBm at the low- and high-power modes. Inter-stage consisted of a series capacitor and shunt inductor, which also work for dc blocking and dc biasing, respectively. The ballasting resistor and capacitor are used at each unit cell in order to improve the amplifier stability, to prevent the thermal runaway, and to match the network.

Mode control switches are also integrated in the MMIC chip and controlled by a mode control voltage source ($V\mathrm{ctrl}$). $V\mathrm{ctrl}$ is available from the baseband controller of a handset. In the



(a)



(b)

Fig. 8. Measured spectra at the peak powers of the high and low modes. (a) High-power mode @ $P_{\rm out} = 28$ dBm. (b) Low-power mode @ $P_{\rm out} = 23.1$ dBm.

low-power mode operation, the auxiliary path's drive and power stages are turned off by the mode control switch. At the same time, the quiescent bias of the power stage of the main amplifier is reduced, but the drive amplifier's quiescent bias point is not changed. At the high-power mode, all the transistors in the amplifiers are fully turned on and operated in class AB. This operation is similar to a conventional PA. The input matching circuits, load-modulation circuit, and output matching circuit are realized on a PCB to tune the phase delay and reduce RF output loss. Stack diodes are attached to prevent electrostatic discharge (ESD) at the input and output of each path and voltage source terminals.

IV. Measurement Results

Fig. 7 shows the gain, PAE, and adjacent channel power ratio (ACPR) for two modes of operation of the amplifier using a

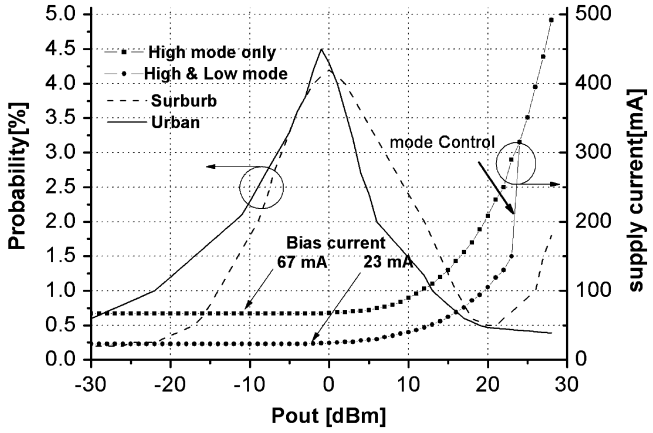


Fig. 9. Measured dc current versus $P_{\rm out}$ for the load-modulation PA by mode control.

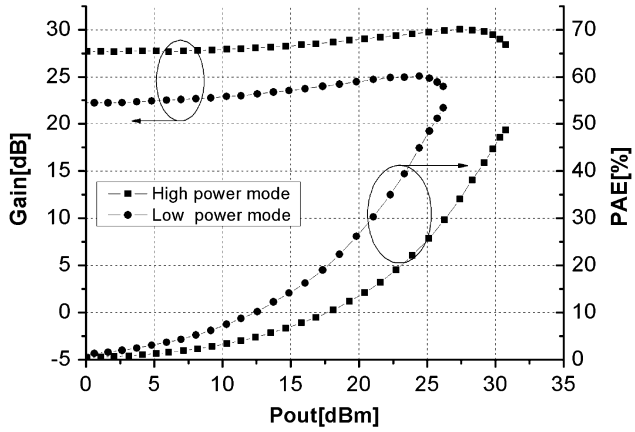


Fig. 10. Gain and efficiency versus $P_{\rm out}$ for AMPS mode operation.

reverse-link IS-95A signal with a chip rate of 1.2288 Mc/s at 836.5 MHz. When Vctrl is 2.85 V, which is the low-power mode, the auxiliary amplifier is turned off, and only the main amplifier contributes to the output power. The total quiescent bias current is 23 mA with $Vcc = 3.4$ V. The PAE of the amplifier is 39.8% at $P_{\rm out}$ of 23 dBm, and ACPR is below 50 dBc and 53.5 dBc at 885 kHz and 1.98-MHz offsets, respectively. When Vctrl is 0 V, which is the high-power mode, the auxiliary amplifier is turned on and both the main and auxiliary amplifiers contribute to the output power. The total quiescent bias current is 67 mA with $Vcc = 3.4$ V. The amplifier has efficiencies of approximately 21%, 37.8% at $P_{\rm out} = 23$ and 28 dBm, respectively, with ACPRs of below 46.5 and 56 dBc at 885 kHz and 1.98-MHz offsets, respectively. The data shows that the efficiency is improved approximately 18.8% at $P_{\rm out} = 23$ dBm by the load-modulation technique. The gain of the PA is 24.8 dB at 23 dBm in the low-power mode, and 29.8 dB at 28 dBm in the high-power mode. The control currents for the high- and low-power modes are 0 mA and less than 0.5 mA, respectively. Fig. 8 shows the CDMA spectra at the peak powers of the high and low modes, respectively, which indicate proper operations.

Fig. 9 shows the measured dc currents and the probability distribution function (PDF) versus output power ($P_{\rm out}$) of the PA. There is a significant reduction in current consumption at a

lower power with comparable consumption at a high power operation. The average current is calculated by the equation in [9]. The average current of this PA is 42 mA in urban and 58.6 mA in suburban CDMA environments, which is reduced by 58%–64% compared to the standard PA in [9].

Fig. 10 shows one-tone continuous signal measurements of the amplifier for AMPS mode operation. The amplifier delivers 26.2 dBm with PAE of 53.4%, 30.8 dBm with 48.7% in the low- and high-power modes, respectively.

V. Conclusion

It has been shown that a handset PA based on the load-modulation technique can deliver highly efficient operation at low output power levels, backed off from the maximum output power, while maintaining high-power RF performances. In order to get a compact module, a $\lambda/4$ transmission line for the load-modulation circuit is replaced by a passive high-pass π-network. Each amplifier is designed for matching at 100 Ω for the combined 50-Ω impedance, and the load-modulation circuit is modifies to function as a matching circuit of the main amplifier, reducing the matching components. For the CDMA environment, the amplifier at the low-power mode exhibits PAE of 39.8% and ACPR less than 50 dBc at 23 dBm and the high-power mode PAE of 37.8% and ACPR of 46.5 dBc at 28.0 dBm. The efficiency is improved by approximately 18.8% at $P_{\text{out}} = 23$ dBm by the load-modulation technique. For the AMPS mode operation, the amplifier delivers 26.2 dBm with a PAE of 53.4% and 30.8 dBm with 48.7% in the low and high modes, respectively. These data clearly show that the new amplifier based on the load modulation to boost efficiency at the low-power level can be a viable circuit approach for handset application.

Acknowledgment

The authors thank FCI Inc., Bundang, Gyeonggi-do, Korea, for fabrication of the PA and technical assistance.

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