A Highly Linear and Efficient Differential CMOS Power Amplifier With Harmonic Control

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***Abstract*—A 2.45 GHz fully differential CMOS power amplifier (PA) with high efficiency and linearity is presented. For this work, a 0.18-μm standard CMOS process with Cu-metal is employed and all components of the two-stage circuit except an output transformer and a few bond wires are integrated into one chip. To improve the linearity, an optimum gate bias is applied for the cancellation of the nonlinear harmonic generated by g_{m3} and a new harmonic termination technique at the common source node is adopted along with normal harmonic termination at the drain. The harmonic termination at the source effectively suppresses the second harmonic generated from the input and output. The amplifier delivers a 20.5 dBm of $P_{1\mathrm{dB}}$ with 17.5 dB of power gain and 37% of power-added efficiency (PAE). Linearity measurements from a two-tone test show that the power amplifier with the second harmonic termination improves the IMD3 and IMD5 over the amplifier without the harmonic termination by maximally 6 dB and 7 dB, respectively. Furthermore, the linearity improvements appear over a wide range of the power levels and the linearity is maintained under −45 dBc of IMD3 and −57 dBc of IMD5 when the output power is backed off by more than 5 dB from $P_{1\mathrm{dB}}$. From the OFDM signal test, the second harmonic termination improves the error vector magnitude (EVM) by over 40% for an output power level satisfying the 4.6% EVM specification.**

***Index Terms*—Differential power amplifier, error vector magnitude (EVM), even in-phase harmonics, harmonic termination, odd anti-phase harmonics, Volterra series.**

I. Introduction

As THE PROLIFERATING wireless personal communication systems require multi-function capability with miniaturization, the CMOS process, which has the merit of high-level integration, becomes the technology of choice for the solution. With the continued scaling of CMOS technology, the multi-function RF transceivers including the baseband and IF blocks, could be integrated in a single chip. Many efforts have also been made to implement RF CMOS power amplifier (PA) [1]–[3] and integrate it with RF transceivers [4]–[6]. However, it is still a challenge for CMOS PA to be competitive with compound semiconductors-based PA. For competitiveness, the CMOS PA needs to overcome poor device reliability and ruggedness problems due to its low breakdown voltage. Many published papers show reasonable power performances with switching CMOS PA, but the operation with large voltage swings ($\sim 3.6\ \mathrm{V_{dd}}$) are still a reliability concern. The full integration of CMOS PA has progressed steadily [7], [8] but signal coupling due to the highly conductive substrate may prohibit the integration of PA with other blocks. The coupled signal from the PA can be large enough to saturate the low-noise amplifier (LNA) and disturb the oscillation frequency of the voltage-controlled amplifier (VCO) (load pulling effect). To reduce the coupling problem, a fully differential circuit topology should be adopted instead of the single-ended PA. In a fully differential topology, the current is dumped to the ground twice per a cycle and the substrate noise components at the signal frequency are suppressed while the second harmonic remains, resulting in a reduced interference.

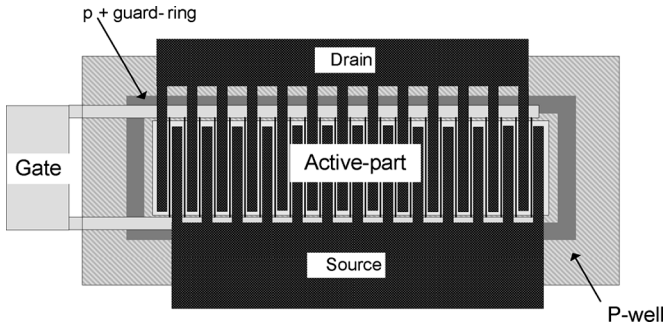

Fig. 1. Simplified structure of unit cell.

Considering the points mentioned above, an IEEE 802.11 WLAN may be the most suitable application for the CMOS PA. Since they operate at a comparably low power level with a low voltage swing ($\sim 2\ \mathrm{V_{dd}}$), the burden of the reliability and ruggedness is significantly reduced. Additionally, the time division duplexing (TDD) mode of the 802.11 WLAN helps the integration with the transceiver since a TDD-based system does not concurrently operate both the receiver and transmitter parts. This confines the substrate coupling problem to the transmitter. A tight error vector magnitude (EVM) specification for the high speed data communication and the over-10-dB peak-to-average-power ratio (PAR) of the OFDM signal require extremely high linearity over a broad power range below $P_{1\mathrm{dB}}$. Furthermore, these requirements impede obtaining high power-added efficiency (PAE) and lower the battery life.

In this paper, we present a highly linear and efficient CMOS PA operating at 2.45 GHz. To secure the high linearity, the gate

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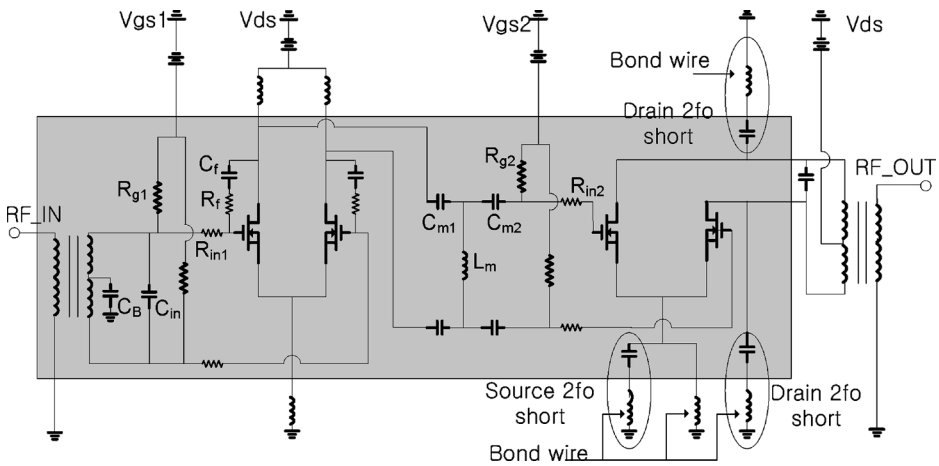

Fig. 2. Schematic of harmonic tuned fully differential CMOS PA.

bias of the PA is applied close to the g_{m3} zero-crossing point and the transistor device size and load line are adjusted for the third-order inter-modulation distortion ratio (IMD3) cancellation not only for a small signal but also for a large signal. Furthermore, this work adopts a new second harmonic termination at the common source node in addition to the typical harmonic termination at the drain. Although the basic idea has been discussed in [9], this work presents a more detailed analysis and impact of linearity improvements on EVM.

After we introduce the implementation of a fully differential CMOS PA in Section II, Section III shows the device characteristics with extracted nonlinear parameters and analysis of the linearity with Volterra series. Based on this information, the circuit design methodology for the optimized linear PA is explained. In Section IV, the RF measurement results and EVM improvements for OFDM signal are presented. Finally, Section V summarizes this work.

II. Implementation of a Differential CMOS PA

A 0.18-μm RF CMOS technology with Cu process is adopted for this work. Compared with the Al process, the relatively higher quality factor of passive components with Cu-metal makes it possible to integrate the components without any severe power loss. Fig. 1 shows the simplified cross section of the unit cell. Since the unit cell of the linear CMOS PA uses nMOS with a very large gate width, it consists of sufficiently spaced multiple unit cells to prevent thermal problem. The gate width and unit finger size of the unit cell should be carefully determined considering the thermal generation and nonuniform current distribution by the gate resistance. The 0.18-μm nMOS with $2.5\ \mu\text{m} \times 80$ gate width is selected for the cell. As shown in Fig. 1, p+ guard-ring surrounds the active part for the substrate contact and device isolation. The substrate contact is connected to the source right inside of the unit cell to minimize the potential difference between the source and substrate. The cell sizes of the two-stage circuit are determined through the iterations of simulation to get the best linearity and other RF performances. The driver consists of 2×1 unit cells and the output consists of 2×6 unit cells. A simplified schematic of the designed PA is shown in Fig. 2. From the figure, the shaded region shows the integrated circuitry and the components outside of the shaded region are bond wire inductors and output matching network of the transformer. R_{g1} and R_{g2} are poly-resistors for blocking RF signal. C_f and R_f form the RC feedback circuit. Capacitor C_{in} consists of the input matching circuit with balun inductance. For the inter-stage matching, C_{m1}, C_{m2}, L_m form the high-pass filter circuit. For the stabilization of the PA, series resistors of R_{in1} and R_{in2} are used. The bond wire inductors are used as matching and harmonic control components. All other inductors are integrated with the low-loss Cu process. For an accurate simulation, the parasitic resistance, capacitance and inductance of the circuit are extracted through electromagnetic (EM)-field simulation. This approach is also used for the design of input balun and inductors. The integrated input balun uses square symmetry [10]. This type of balun has two groups of inter-wound micro-strip lines and the center tab can be placed precisely at the symmetric point between the terminals on each winding. By grounding the center tab, a precisely balanced signal can be obtained.

III. Circuit Design Methodology

In designing a linear PA with high linearity and PAE, a class AB with well-controlled harmonics is a good choice. To find the optimum design condition, this work analyzes the device characteristics and linearity of the unit cell (test device) using a small-signal model and Volterra series. For a simulation, we use the large signal model and S-parameters obtained from on-wafer measurement of test devices at various bias points. The probe-pads effects are eliminated using a two-step de-embedding procedure [11], [12]. Based on the small-signal equivalent circuit of Fig. 3 [13], the parameters are extracted from the de-embedded S-parameters. The Volterra series is a Taylor series equivalent for a memory system and can be used to accurately model any nonlinear systems [14]. The analysis has the ability to individually describe all orders of distortion and to compare the contributions from different nonlinear components. The expansion coefficients of the series are calculated from the extracted nonlinear parameters of the small-signal model. Based on the linearity analysis, the circuit configuration for the optimized linear CMOS PA are determined.

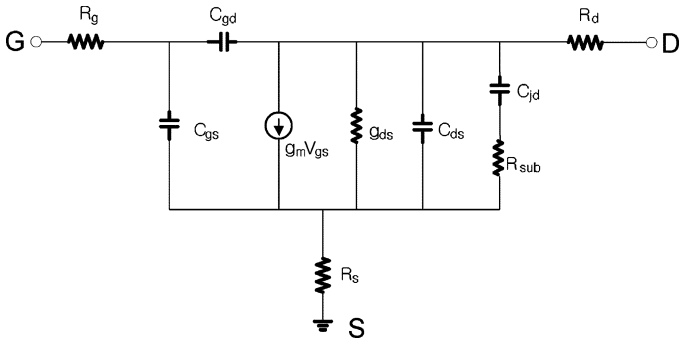

Fig. 3. Small-signal equivalent circuit of the test device.

A. Analysis of Device Linearity Characteristics

In Fig. 3, the transconductance g_m, output conductance g_{ds}, gate-source capacitance C_{gs}, and drain junction capacitance C_{jd} are bias-dependent nonlinear parameters and generate nonlinear harmonics. In the saturation region, the gate-drain capacitance C_{gd} is mainly extrinsic capacitance and drain-source C_{ds} capacitance is nearly zero [15], so the parameters are approximated as bias independent parameters.

Fig. 4 shows the bias dependent transconductance g_m and output conductance g_{ds}. In normal CMOS operation, the nonlinear harmonic comes mainly from these two parameters, more from g_m nonlinearity [16]. Since the high-order coefficients and cross modulations of g_m and g_{ds} are negligible, the nonlinear g_m and g_{ds} can be expressed by the third-order Taylor expansion as follows:

$$g_m = g_{m1} + g_{m2}v_{gs} + g_{m3}v_{gs}^2 \tag{1}$$
$$g_{ds} = g_{ds1} + g_{ds2}v_{ds} + g_{ds3}v_{ds}^2. \tag{2}$$

The corresponding nonlinear currents from the g_m and g_{ds} are given by

$$i_{\text{trans}} = g_{m1}v_{gs} + g_{m2}v_{gs}^2 + g_{m3}v_{gs}^3 \tag{3}$$
$$i_{\text{cond}} = g_{ds1}v_{ds} + g_{ds2}v_{ds}^2 + g_{ds3}v_{ds}^3. \tag{4}$$

The second- and third-order inter-modulation currents generated from the g_m and g_{ds} are as follows:

$$i_{\text{trans},2\omega_2} = \frac{1}{2}g_{m2}v_{gs,\omega_2}^2 \tag{5}$$
$$i_{\text{trans},2\omega_2-\omega_1} = \frac{3}{4}g_{m3}v_{gs,\omega_2}^2 v_{gs,\omega_1}^* \tag{6}$$
$$i_{\text{cond},2\omega_2} = \frac{1}{2}g_{ds2}v_{ds,\omega_2}^2 \tag{7}$$
$$i_{\text{cond},2\omega_2-\omega_1} = \frac{3}{4}g_{ds3}v_{ds,\omega_2}^2 v_{ds,\omega_1}^*. \tag{8}$$

where the asterisk implies the complex conjugate. Fig. 5 shows the expansion coefficients of g_m and g_{ds} which are calculated around the actual bias point of our class-AB PA described in Section IV. In the figures, the second-order expansion coefficients of g_{m2} and g_{ds2} generate the second harmonics and they couple backed to the input through gate-drain capacitance. The feedbacked second harmonics and fundamental signal generate the third harmonics by g_{m2} and g_{ds2} related with second-order term of (3) and (4). For an optimized linear PA, the nonlinear second harmonic generated from the output should be terminated, thereby suppressing the third harmonic regeneration. A strong nonlinear behavior of g_{m3} (6) can be avoided by setting the bias point close to g_{m3} zero-crossing point as indicated in Fig. 5(a). Because g_{m3} has symmetrical magnitude with anti-phase around the point, the harmonic distortion generated from it can be canceled for a small signal [17]. Furthermore, the harmonic distortion for a large signal can also be canceled by the proper v_{gs} sweeping with the optimized cell size and load line, which will be shown in Section IV. It is worthwhile to notice that g_{m2} is the largest at the bias point, increasing the importance of the second harmonic termination. The third harmonic generated from g_{ds3} (8) is negligible and it is confirmed by the almost zero of g_{ds3} in Fig. 5(b).

For the optimized linear PA with the linearized g_m and g_{ds}, the nonlinear harmonic distortion generated from the gate-source capacitance C_{gs} determines the overall linearity of the PA [18]. In the substrate network, the drain junction diode is always reverse biased, working as a nonlinear capacitance C_{jd}, and is not negligible [16]. Fig. 6 shows the extracted C_{gs} and C_{jd}. The C_{gs} shows a rapid variation around threshold voltage ($\sim V_{gs} = 0.5$ V) and the class AB PA is biased around the point. The extracted C_{jd} shows a typical decreasing curve according to V_{ds} [19], [20]. The nonlinear behaviors of C_{gs} and C_{jd} can be expressed by the third-order Taylor expansion as follows:

$$C_{gs} = C_{gs1} + C_{gs2}v_{gs} + C_{gs3}v_{gs}^2 \tag{9}$$
$$C_{jd} = C_{jd1} + C_{jd2}v_{ds} + C_{jd3}v_{ds}^2. \tag{10}$$

The second- and third-order intermodulation currents generated from the C_{gs} are as follows:

$$i_{C_{gs},\omega_2-\omega_1} = j(\omega_2-\omega_1)C_{gs2}v_{gs,\omega_2}v_{gs,\omega_1}^* \tag{11}$$
$$i_{C_{gs},2\omega_2} = j\omega_2 C_{gs2}v_{gs,\omega_2}^2 \tag{12}$$
$$i_{C_{gs},3\omega_2} = \frac{3}{4}j\omega_2 C_{gs3}v_{gs,\omega_2}^3 \tag{13}$$
$$i_{C_{gs},2\omega_2-\omega_1} = j(2\omega_2-\omega_1)\frac{3}{4}C_{gs3}v_{gs,\omega_2}^2 v_{gs,\omega_1}^* + j(2\omega_2-\omega_1) \times C_{gs2}\left[v_{gs,2\omega_2}v_{gs,\omega_1}^* + v_{gs,\omega_2}v_{gs,\omega_2-\omega_1}^*\right]. \tag{14}$$

From Fig. 5(a), the g_{m2} at the class-AB bias point (close to g_{m3} zero crossing point) is very large and the inter-modulations by the g_{m2} between the second harmonics of (11) and (12) from the C_{gs2} and fundamental voltages generate the significant third harmonics. The second harmonic of (12) and third harmonic of (13) generate the fifth harmonic by the g_{m2} related second-order term of (3). The C_{gs2} related third harmonic product is included in (14) [21] because the second-order harmonic is not always terminated at the input of a multi-stage PA. Fig. 7(a) shows the expansion coefficients of C_{gs}. From the graph, the coefficients of C_{gs2} and C_{gs3} have anti-phases. Therefore, the third harmonic of (14) has a cancellation effect. To effectively avoid

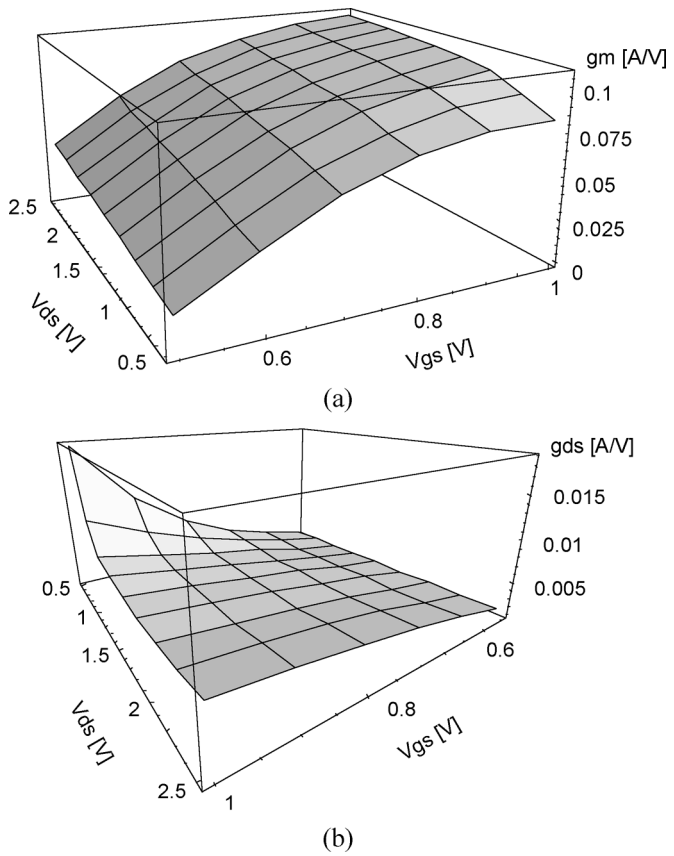

Fig. 4. Bias dependencies of g_m and g_{ds}. (a) Extracted g_m. (b) Extracted g_{ds}.

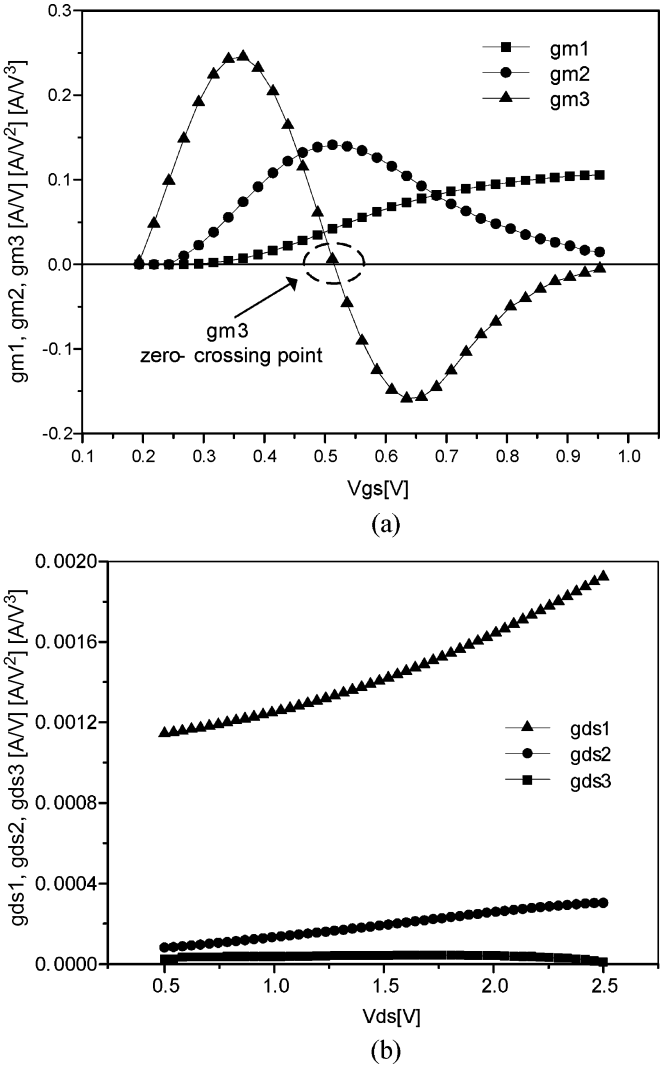

Fig. 5. Harmonic generation coefficients of g_m and g_{ds}. (a) Calculated power expansion coefficients of g_m at $V_{ds} = 2.5$ V. (b) Calculated power expansion coefficients of g_{ds} at $V_{gs} = 0.51$ V.

the harmonic generations from the C_{gs}, the second harmonic should be properly terminated at the input of a multi-stage PA.

The third-order inter-modulation current generated from the C_{jd} is as follows:

$$i_{C_{jd},2\omega_2-\omega_1} = j(2\omega_2 - \omega_1)\frac{3}{4}C_{jd3}v^2_{ds,\omega_2}v^*_{ds,\omega_1}. \qquad (15)$$

Fig. 7(b) shows the expansion coefficients of C_{jd}. From the figure, the third-order coefficient becomes large around the bias point of the PA ($V_{ds} = 2.5$ V), generating some third harmonic. The impedance ratio between the C_{jd} and the load is large at low frequency and gets smaller as the frequency increases. Therefore, the nonlinear effect by C_{jd} at high frequency becomes important [16].

B. Evaluation of Power Amplifier Linearity

The overall linearity of the amplifier is determined through additions and cancellations among the third-order inter-modulation components and it is dependent on the input and load impedances (Z_S, Z_L). To alleviate the complex calculation for the linearity analysis, computer simulations of the Volterra analysis are carried out. The total nonlinear circuit is shown in Fig. 8 and the nonlinear components of g_m, g_{ds}, C_{gs}, and C_{jd} can be replaced with the Volterra expansions of (1), (2), (9), and (10). The total nonlinear circuit is realized in the Symbolically Defined Device (SDD) of Agilent Design System (ADS). A second harmonic termination circuit for a linear PA is represented by a 2fo short. In this circuit, the harmonics of $(f_1 - f_2)$ are all terminated to short circuit. Fig. 9 shows the total IMD3 and its contributions from each nonlinear component through the harmonic-balance simulation. A 2 MHz spaced two-tone signal at 2.45 GHz center frequency is applied and Z_S and Z_L are conjugately matched. Since the nonlinear circuit of Fig. 8 is a small-signal model, a small input power is applied to keep the effectiveness of the used power expansion coefficients. The IMD3 contributions of each nonlinear component are calculated with zero for the second- and third-order expansion coefficients of other components. The linearity is compared by the IMD3, which is defined as follows:

$$\mathrm{IMD3} = 10\log\frac{P_{3\mathrm{rd}}}{P_{\mathrm{fund}}} \quad [\mathrm{dBc}] \qquad (16)$$

where $P_{3\mathrm{rd}}$ is the third-order inter-modulation distortion power and P_{fund} is the fundamental power. It can be seen that the g_m contribution to IMD3 is small. The low harmonic generation is attributed to the second harmonic termination at the output and biasing close to the g_{m3} zero crossing point. With the choice of

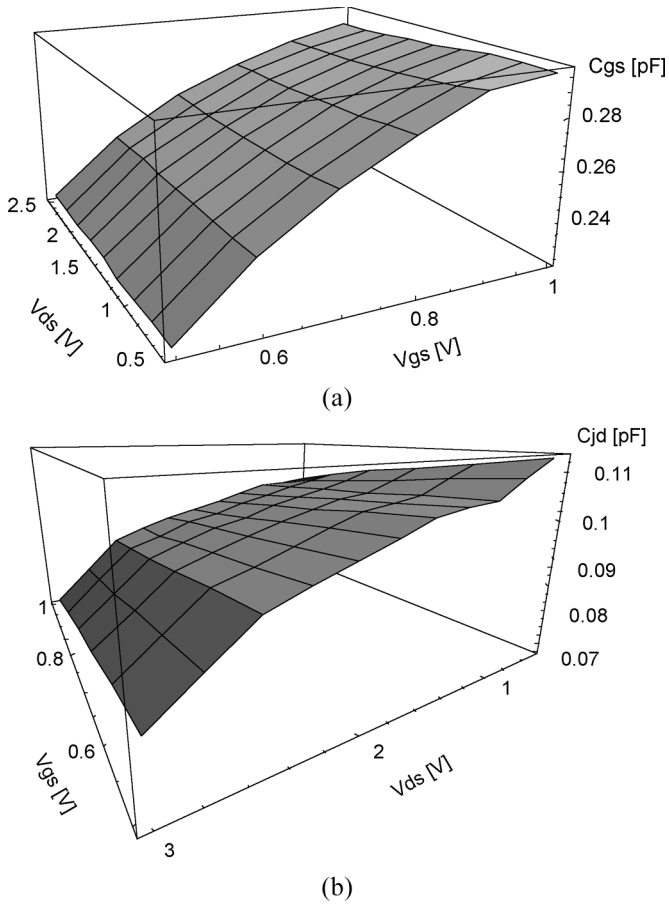

Fig. 6. Bias dependencies of C_{gs} and C_{jd}. (a) Extracted C_{gs}. (b) Extracted C_{jd}.

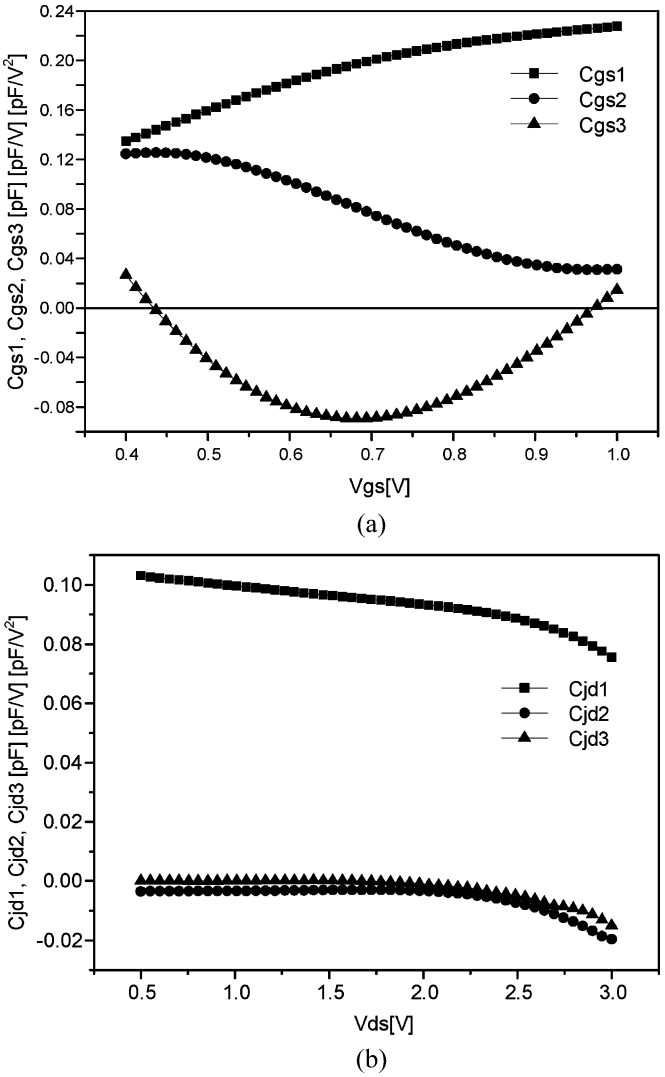

Fig. 7. Harmonic generation coefficients of C_{gs} and C_{jd}. (a) Calculated power expansion coefficients of C_{gs} at $V_{ds} = 2.5$ V. (b) Calculated power expansion coefficients of C_{jd} at $V_{gs} = 0.51$ V.

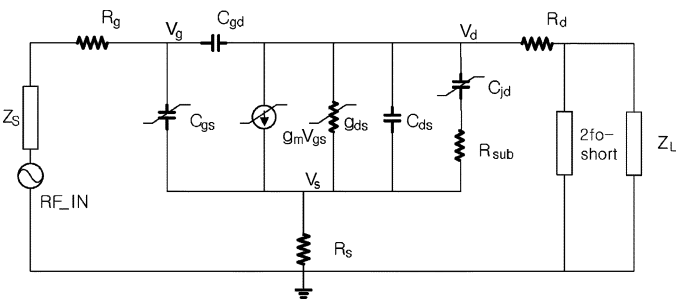

Fig. 8. Nonlinear equivalent circuit for Volterra series analysis.

the bias point, the nonlinear harmonic distortion generated from the C_{gs} determines the overall linearity of the PA and its contribution is about 10 dB higher than g_m nonlinearity. Compared to the contributions of the g_m and C_{gs}, the contributions of the g_{ds} and C_{jd} are small, but should not be neglected for the overall linearity. Fig. 10 shows the IMD comparisons for various methods of the second harmonic terminations. To investigate the effect of parasitic source inductance, 0.3 nH inductance is added to the source of Fig. 8. In this situation, the parasitic inductance enhances the harmonic distortions of the output and input and the 2fo short circuit at the drain cannot eliminate the output second harmonics completely. From the figure, IMD3 with 2fo short at the drain is about 10 dB higher than the total IMD3 of Fig. 9. But the second harmonic termination at the source completely terminates the residual second harmonics of the output and reduces the harmonic distortion of the input. The resultant IMD3 and IMD5 are improved by 7 dB and 10 dB, respectively. The additional second harmonic termination at the input completely removes the C_{gs2} related harmonic down-conversions and further improves the IMD3 and IMD5.

IV. Realization of the Optimized Linear CMOS PA

The fully differential two-stage PA of Fig. 2 adopts class-AB operations for both driver and output cells. To stabilize the PA, the driver cell employs series resistor feed-back to reduce gains at the driver and output cells. For the linear power operation, the power matching circuit includes the harmonic tunings. In the case of differential topology, the characteristics of even in-phase harmonics and odd anti-phase harmonics make it more feasible to control the even harmonics than the single-ended topology. As shown in Fig. 2, the matching between the balun and input of driver cell is realized with one MIM capacitor and the input balun is directly matched to 50-ohm input. To obtain a precisely balanced anti-phase signal after the balun, the center tab

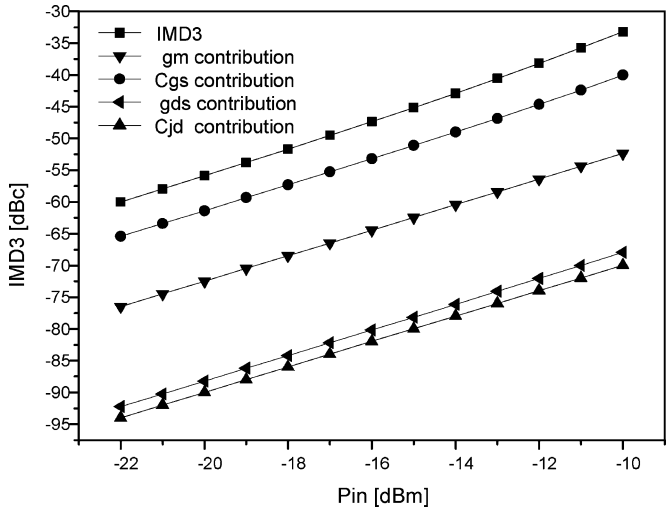

Fig. 9. Calculated IMD3 and the contributions of each nonlinear components.

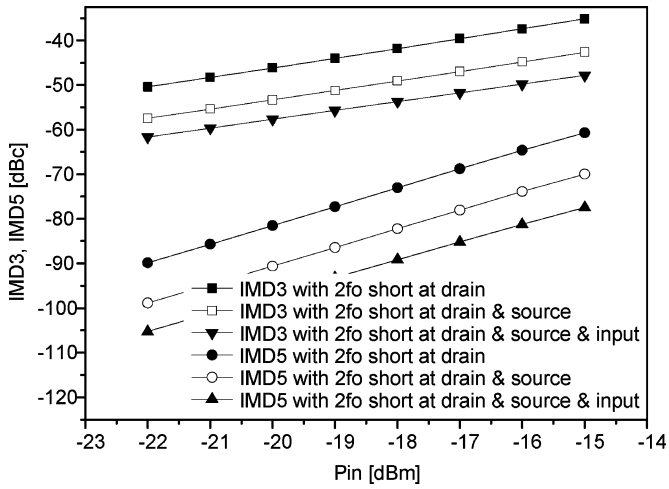

Fig. 10. IMD3 and IMD5 comparisons for various methods of the second harmonic terminations.

of the secondary inductor is connected to ground. Additionally, the grounded center tab provides nearly zero impedance at the second harmonic, improving the linearity of the driver cell. The load matching of the power cell is implemented with off-chip transformer and chip capacitor. To make an effective second harmonic short at the drain of the power cell, a resonant circuit is placed at the drain. The integrated MIM capacitor with a bond wire inductor provides a resonance at 2fo and the resonance frequency can be tuned by adjusting the length of the bond wire. The bond wire for the second harmonic short circuit can save chip area and provides the adjustability. Additionally, by placing this resonance circuit at the very end of the drain, the detuning effect of the matching is suppressed effectively. The inter-stage matching is realized using a high-pass filter circuit. This circuit provides the conjugate matching condition between the output of the driver cell and input of the power cell, blocking the DC current of each cell. Additionally, the circuit has zero impedance for the second harmonic at the output of the driver cell. But this circuit does not provide zero impedance for the second harmonic generated from the C_{gs} of the power

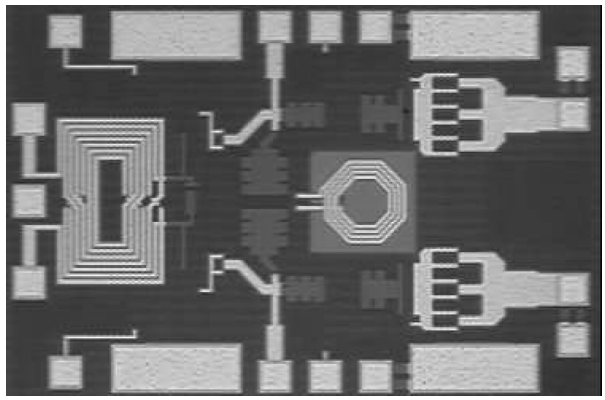

Fig. 11. Photograph of the fully differential CMOS PA.

cell because it is difficult to terminate it, while satisfying all matching conditions. Though the second harmonic of C_{gs} can be terminated by using more matching components, it makes the inter-stage matching circuit more complex and increases the chip size. The standard CMOS process must use bond wires for the grounding since via is not available. In case of a CMOS PA which has very low impedance, a small inductance at the source can severely degrade power gain and the linearity is also very sensitive to the source inductance. Multiple down bonds at the source must be used to maintain the inductance as low as possible but there are limits. The virtual ground of the differential PA can solve the gain reduction problem. But the linearity under the class-AB mode operation is another issue because the in-phase second harmonics of differential PA sees the source inductance directly. A simulation result confirms that despite the second harmonic termination at the drain, the nonzero inductance at the source increases the harmonic distortion and makes the linearity very sensitive to its variation. In this work, another second harmonic control circuit is placed at the common source of the power cell as shown in Fig. 2, whose implementation method follows that of the drain harmonic termination. By placing it at the common source, the in-phase second harmonics at the output is completely terminated and those of the input are reduced somewhat as shown in Fig. 10, removing the sensitivity of the linearity on the source inductance. Furthermore, because virtual ground of the fundamental frequency is made at the common source, the disturbance of power gain and PAE by the source harmonic termination circuit is almost negligible.

V. Experimental Results

Fig. 11 shows a photograph of the fabricated CMOS PA whose chip area is 1.43 mm $\times$ 0.94 mm. To verify the chip, an evaluation board is fabricated using FR-4 PCB and the chip is directly mounted on the ground plate of the evaluation board. Because the bond wire inductance is dependent on the geometry and has the mutual inductance of the multiple bonding, the inductances are estimated through EM-field simulation. On the basis of these data, the bond wire is adjusted for the tuning of the delicate impedance matching and harmonic control. To measure the RF performances and harmonic termination effects at the common source node, a two-tone test is performed at 2.45 GHz center frequency and 2 MHz tone-spacing. The bias

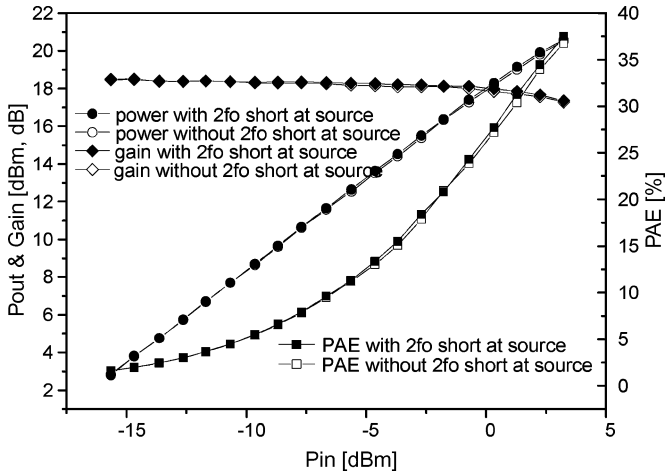

Fig. 12. Comparisons of the output power, gain, and PAE between two types of PAs with and without the second harmonic termination at the common source.

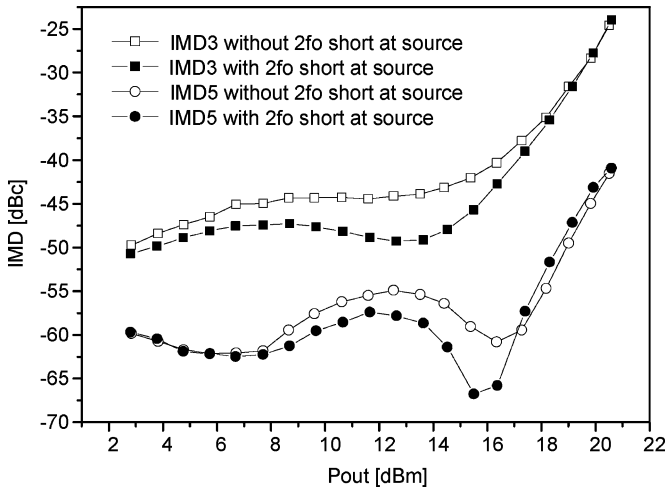

Fig. 13. Comparisons of the IMD between two types of PAs with and without the second harmonic termination at the common source.

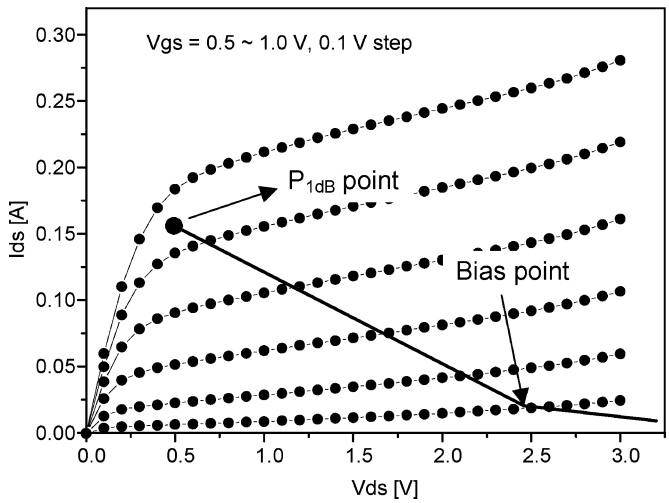

Fig. 14. Load line of the power cell.

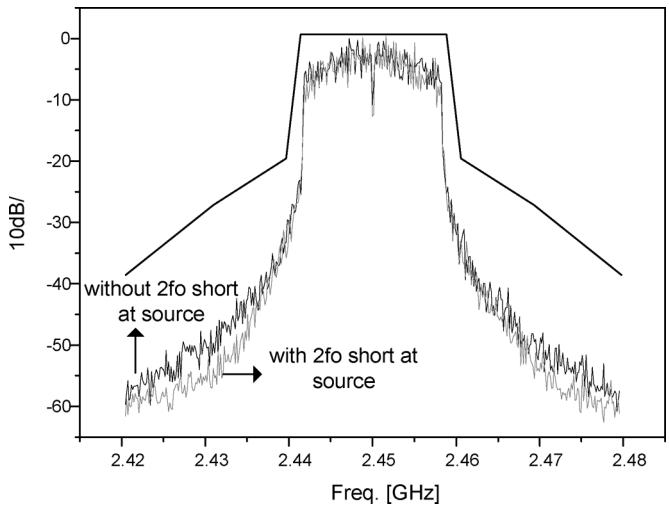

Fig. 15. Spectrum comparison with IEEE 802.11g OFDM signal at $P_{\rm out}$ = 14 dBm.

is applied at $V_{gs} = 0.51$ V and $V_{ds} = 2.5$ V. Comparisons are made between the PAs with and without the second harmonic termination at the common source. Both PAs terminate the second harmonic at the drain and 8-multiple bonding wires are provided at the source of the power cell to minimize the wire inductance.

Fig. 12 shows the power measurement results of the amplifiers. From the graph, $P_{\rm 1dB}$ and power gain of the PA with the second harmonic termination at the common source is 20.5 dBm and 17.5 dB, respectively, with PAE of 37%. Comparing the two PAs, the PA with the second harmonic termination at the common source shows slightly higher power gain and PAE, but the differences are negligible. This result verifies that the virtual ground at the common source is well formed inside the chip and the second harmonic termination circuit does not disturb the odd anti-phase signal. Fig. 13 shows the IMD comparisons. From the figure, the PA only with the second harmonic termination at the drain shows a high linearity and IMD3 and IMD5 are maintained low across a broad power range. The biasing close to the g_{m3} zero crossing point with a proper load line makes the IMD3 cancellation across the large signal level and maintains the low distortion. Fig. 14 shows the load line of the power cell which forms the output stage. The bias point is very close to the pinch-off point and the load line is located at a low current region which can help ensure high efficiency. The load line is tilted around the bias point due to the harmonic tuning. Despite the high linearity of the PA only with drain harmonic termination, both IMD3 and IMD5 of the PA with the second harmonic termination at the source are significantly improved across broad power range, maximally 6 dB and 7 dB, respectively. This result indicates that the second harmonic is effectively suppressed with the second harmonic resonance circuit at the common source. The improved linearity of this amplifier maintains under -45 dBc of IMD3 and -57 dBc of IMD5 for an output power backed-off over 5 dB from $P_{\rm 1dB}$. The reduced linearity improvement, comparing to the Volterra series analysis in Section III, is assumed to the slight mismatch. To validate the linearization for the EVM, IEEE 802.11g 54-Mbps/64-QAM OFDM signal with 12-dB PAR is applied. Fig. 15 shows the

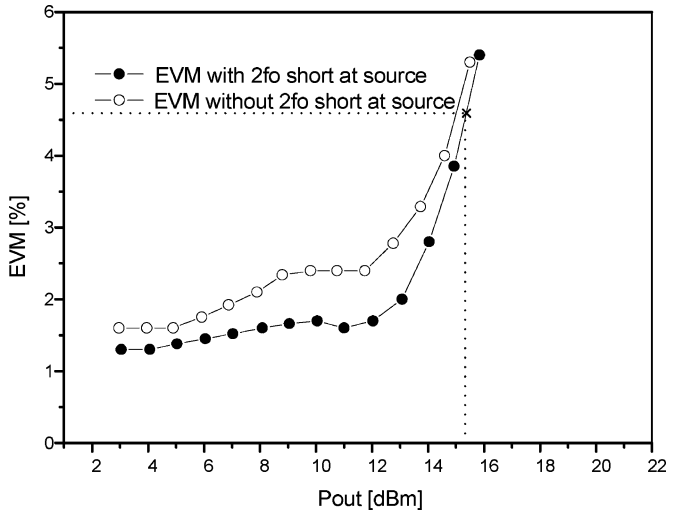

Fig. 16. Comparisons of the EVM between two types of PAs with and without the second harmonic termination at the common source.

spectrum comparisons at 14 dBm of $P_{\rm out}$. Despite the excellent adjacent channel leakage ratio (ACLR) of the spectrum, the second harmonic termination at source further improves the ACLR, which is an expected result from Fig. 13. Fig. 16 shows the EVM comparison according to the $P_{\rm out}$, where the signal source has 1% EVM. For the $P_{\rm out}$ satisfying 4.6% EVM Specification, the PA with the second harmonic termination at source shows an EVM improvement of over 1% over the counter-part PA. In other words, the EVM is improved over 40%. The PA delivers 14% PAE at EVM 4.6%.

VI. Conclusion

A differential linear power amplifier at 2.45 GHz is implemented using a 0.18-μm CMOS process. For an optimized linear PA, the nonlinear g_m is linearized by the second harmonic termination at the output and biasing close to the g_{m3} zero crossing point with a proper load line. Additionally, the newly adopted second harmonic termination at the common source completely terminates the residual second harmonic of the output due to the source inductance and significantly suppresses the harmonic distortion from the C_{gs}, which is a dominant nonlinear source for the class-AB PA. The simple and small sized second harmonic terminations are realized by connecting a MIM capacitor and a bond wire inductor to the drain and the source node. The second harmonic termination at the common source shows a significant improvement on linearity without degrading output power and PAE and the excellent linearity is maintained across a broad power range. The RF performance of this amplifier shows the $P_{\rm 1dB}$ of 20.5 dBm, power gain of 17.5 dB, and PAE of 37% at the point. The linearity of the amplifier is very good, below -45 dBc for IMD3 and -57 dBc for IMD5 across a broad power range. From the OFDM signal test, the linearity is improved about 40% EVM by the second harmonic termination at common source for the power level satisfying the 4.6% EVM specification. Additionally, these results show that linearity improvement at the average power level is important to the EVM enhancement, along with the increased $P_{\rm 1dB}$.

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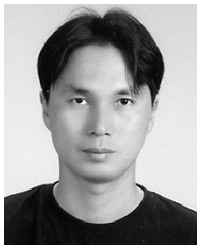

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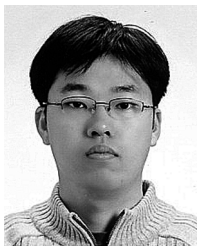

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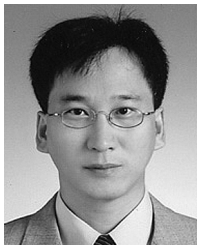

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