The Doherty Power Amplifier

The current wireless communication systems have made significant progress toward increased bandwidth and number of carriers for high-data-rate applications. Memory effects, however, make it very difficult to design a high-power amplifier with a wide instantaneous bandwidth. In addition to bandwidth concerns, the instantaneous transmit powers of the wireless communication systems, such as CDMA-2000, wide-band code division multiple access (WCDMA), orthogonal frequency division multiplexity (OFDM) and so on, vary widely and rapidly, carrying high peak-to-average ratio (PAR) signals. The base station power amplifiers for the systems require a high linearity to amplify the high PAR signal source without distortion. To satisfy linearity requirements, the power amplifiers are usually biased at class A or AB mode and must operate at a large amount of back-off from the peak output power.

Another requirement of the base station power amplifier for the modern wireless communication systems is high efficiency. As the communication systems are reduced in both size and cost, the cooling system should be simple and small, requiring a power amplifier with high efficiency. Because the base station power amplifiers have a low efficiency due to the back-off operation, efficiency enhancement techniques become very important. The design technique of the base station power amplifiers with high efficiency and linearity across a wide instantaneous bandwidth has become a hot issue [1].

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In this article, we show that the Doherty amplifier is capable of delivering the stringent requirements of the base station power amplifiers. We explain the operation principles, including both linearity and efficiency improvements, and the basic circuit configuration of the amplifier. Advanced design methods to operate across wide bandwidth and improve the linearity are also described. For verification, the Doherty amplifier is implemented using laterally diffused metal oxide semiconductor (LDMOS) transistors and measured using a WCDMA 4FA signal. These results show that the Doherty amplifier is a promising candidate for base station power amplifiers with wide bandwidth, high efficiency, and linearity.

Doherty Amplifier Operation

The Doherty amplifier was first proposed by W.H. Doherty in 1936 [2]. The original Doherty amplifier consisted of two tube amplifiers and an impedance inverting network. The efficiency of an RF power amplifier is increased using the RF Doherty amplifier technique, as described in detail in [3]. This amplifier consisted of a carrier amplifier and a peaking amplifier. The output load is connected to the carrier amplifier through an impedance inverter (a quarter-wave transmission line) and directly to the peaking amplifier. Figure 1(a) shows an operational diagram to analyze the Doherty amplifier circuit. Two current sources represent the amplifiers. It is assumed that each current source is linearly proportional to the input voltage signal, operating as a class AB or class B amplifier with harmonic short circuits after it is turned on, and the efficiency analysis can be carried out using the fundamental and dc components only. As shown in Figure 1(b), the peaking amplifier turns on at one-half the maximum input voltage.

The Doherty amplifier technique is based on the load impedance change of each amplifier, referred to as load modulation, according to the input power level. Figure 1(b) shows the fundamental currents from the amplifiers. The load impedances of two amplifiers are given by

$$Z_C = \begin{cases} \frac{Z_T^2}{Z_L}, & 0 < v_{in} < V_{\text{in, max}}/2 \\ \frac{Z_T^2}{Z_L \cdot \left(1+\frac{I_P}{I_C}\right)}, & V_{\text{in, max}}/2 < v_{\text{in}} < V_{\text{in, max}} \end{cases} \quad (1)$$

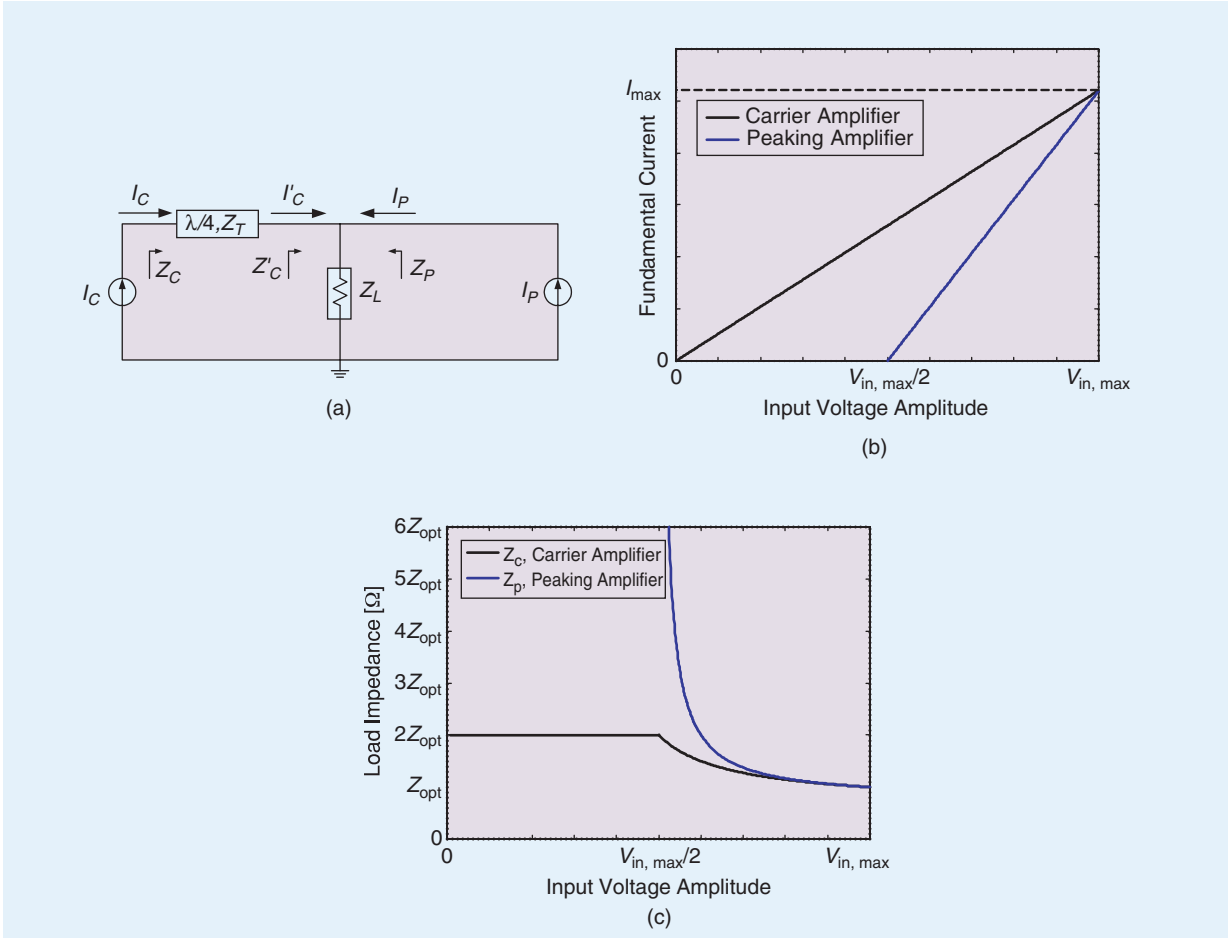

Figure 1. *(a) Operational diagram of the Doherty amplifier. (b) Fundamental currents versus input voltage. (c) Load impedances versus input drive.*

$$Z_P = \begin{cases} \infty, & 0 < v_{in} < V_{\text{in, max}}/2 \\ Z_L\left(1 + \frac{I_C}{I_P}\right), & V_{\text{in, max}}/2 < v_{\text{in}} < V_{\text{in, max}}, \end{cases} \quad (2)$$

where Z_L is the load impedance of the Doherty amplifier; I_C and I_P represent the fundamental currents of the carrier and peaking amplifiers, respectively; and Z_C and Z_P are the output load impedances of the carrier and peaking amplifiers, respectively, and are depicted in Figure 1(c).

In the low-power region ($0 \sim V_{\text{in, max}}/2$), the peaking amplifier remains in the cut-off state, and the load impedance of the carrier amplifier is two times larger than that of the conventional amplifier. Thus, the carrier amplifier reaches the saturation state at the input voltage $(V_{\text{in, max}})/2$ since the maximum fundamental current swing is half and the maximum voltage swing reaches V_{dc}. As a result, the maximum power level is half of the carrier amplifier's allowable power level (a quarter of the total maximum power or 6 dB down from the total maximum power), and the efficiency of the amplifier is equal to the maximum efficiency of the carrier amplifier as shown in Figure 2.

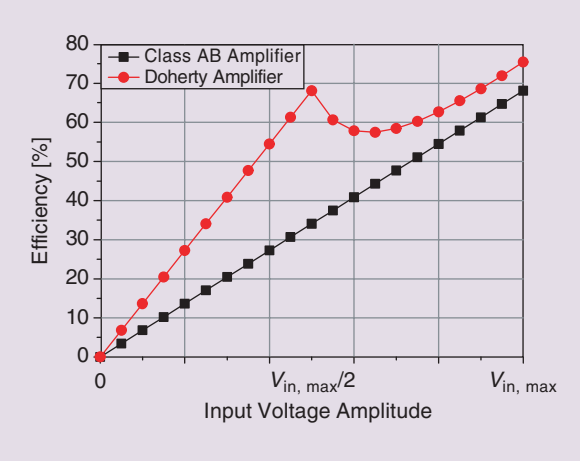

Figure 2. *Plot of efficiencies versus input drive level for the Doherty amplifier (the class AB biased carrier amplifier/the class C biased peaking amplifier) and the class AB amplifier.*

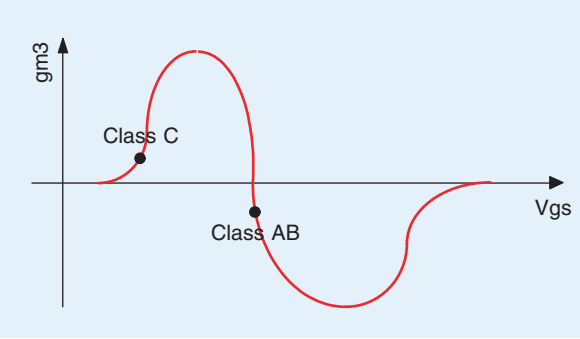

Figure 3. *Large-signal gm3 versus gate bias for general FET and bias points of the Doherty amplifier.*

In the high-power region ($V_{\text{in, max}}/2 \sim V_{\text{in, max}}$), where the peaking amplifier is conducting, the current level of the peaking amplifier plays an important role in determining the load modulation of the Doherty amplifier [see (1) and (2)]. Assuming that g_m of the peaking amplifier is twice as large as that of the carrier amplifier, the current and voltage swings of the peaking amplifier increase in proportion to the input voltage level and the voltage swing reaches the maximum voltage swing of V_{dc} only at the maximum input voltage. The load impedance of the carrier amplifier varies from $2Z_{\text{opt}}$ to Z_{opt}, and the peaking amplifier varies from ∞ to Z_{opt} according to the input voltage level as shown in Figure 1(c). The efficiency of the Doherty amplifier at the maximum input voltage is equal to the maximum efficiency of the amplifiers. When the peaking amplifier is the same size as the carrier amplifier, which is normally the case, g_m of the two amplifiers are identical and the peaking amplifier can not be fully turned on, so the power performance is degraded [4]. From the basic operation principle, we have explored the Doherty amplifier, which provides higher efficiency over whole power ranges compared to the conventional class AB amplifiers. The resulting Doherty amplifier can solve the problem of maintaining a high efficiency for a large PAR signal.

Linearity of the Doherty Amplifier

The linearity of the Doherty amplifier is more complicated than that of a class AB amplifier. The class AB biased carrier amplifier has a load impedance at the low power level that is twice as large and the high impedance of the carrier amplifier compensates the low gain characteristic due to the input power division. At high power levels, the two amplifiers generate full power using normal load impedances, equalizing the power gain. Additionally, in the low-power region, the linearity of the amplifier is entirely determined by the carrier amplifier. Therefore, the carrier amplifier should be highly linear even though the load impedance is high.

At a high power level, linearity of the amplifier is improved by the harmonic cancellation from the two amplifiers using appropriate gate biases. Figure 3 shows the third-order harmonic generation coefficient g_{m3} of an LDMOS transistor and the bias points of the two amplifiers. In terms of gain characteristics of each amplifier, a late gain expansion of the class C biased peaking amplifier compensates the gain compression of the class AB carrier amplifier. Thus, the Doherty amplifier, which is based on the load modulation technique, is capable of delivering more linear output power than a conventional class AB power amplifier. The third-order intermodulation (IM3) level from the carrier amplifier increases and the phase of the IM3 decreases because the gain of the carrier amplifier is compressed. In contrast, when the gain of the peaking amplifier is expanded, both the IM3 level and phase increase. To cancel out the IM3s from the

two amplifiers, the components must be 180° out of phase with the same amplitudes. Therefore, the peaking amplifier should be designed appropriately to cancel the harmonics of the carrier amplifier.

The Circuit Configuration of Doherty Amplifier

Figure 4 shows a schematic diagram of the fully matched microwave Doherty amplifier with offset transmission lines at the output circuits [5]. The carrier and peaking amplifiers have input/output matching circuits, which transform from the input impedances of the devices to 50 Ω and from the optimum load impedance Z_{opt} of the devices to 50 Ω, respectively. The additional offset transmission lines with characteristic impedance of 50 Ω are connected after the matching circuits of the carrier and peaking amplifiers. In the low-power region, the phase adjustments of the offset lines cause the peaking amplifier to be open-circuited and the characteristic load impedance of the carrier amplifier is doubled to $2R_o$ by a quarter-wave impedance transformer. This is illustrated in Figure 5(a) and (b). The offset line of the carrier amplifier varies from Z_{opt} to $2Z_{opt}$ for the proper load modulation as shown in Figure 5(a). Figure 5(b) illustrates that the offset line of the peaking amplifier adjusts to the high impedance so that it prevents power leakage. Figure 5(c) shows the appropriate transformations on a Smith chart to determine the offset line length of each amplifier. The lines do not affect the overall matching condition and load modulation because they are matched to the characteristic impedance of 50 Ω. The Doherty output combining circuit consists of a quarter-wave transmission line with the characteristic impedance of 50 Ω and a quarter-wave transmission line that transforms from 50 to 25 Ω to determine the load impedance of the output combining circuit. A phase delay line is needed at the input of the peaking amplifier to adjust the same delay between the carrier and peaking amplifiers [6].

The Doherty amplifier consists of a class AB biased carrier amplifier and a class C biased peaking amplifier. Due to the different biasing, the RF current from the amplifiers

To satisfy linearity requirements, the power amplifiers are usually biased at class A or AB mode and must operate at a large amount of back-off from the peak output power.

are different depending on the input drive level. The asymmetric powers are combined by the Doherty operation through a quarter-wave impedance converter.

Advanced Design Methods for the Doherty Amplifier

The fundamental operation principles of a Doherty amplifier were described in the previous section. We have seen that the advantages of the microwave Doherty amplifier are the simple circuit configuration and improved efficiency and linearity. In this section, we explain some typical issues with Doherty amplifiers and present proposed methods to address them.

The Doherty amplifier for the base station system usually has two amplifiers with identical size devices, matching circuits, and input drives. Because the peaking amplifier is biased lower than the carrier amplifier, the current level of the peaking amplifier at the maximum input drive cannot reach the maximum allowable current level. Thus, the load impedances of both amplifiers can not be fully modulated to the optimized

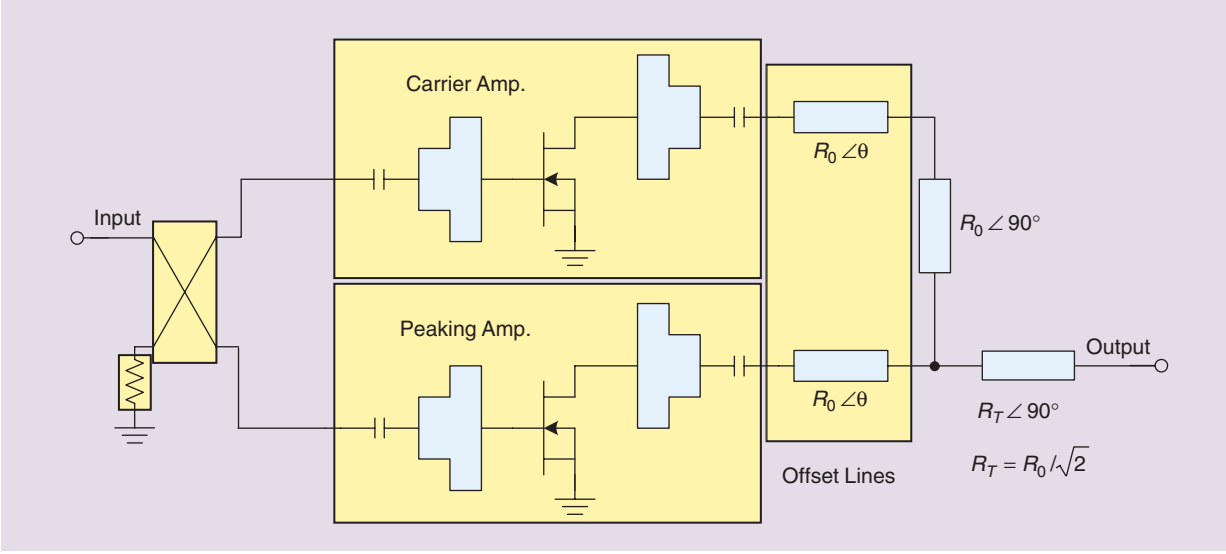

Figure 4. *Schematic diagram of the Doherty amplifier.*

impedance, Z_{opt}, and they are larger than the optimum values. As a result, the conventional Doherty amplifier is heavily saturated, and both linearity and power are degraded. It is difficult to improve the linearity of the Doherty amplifier across a wide bandwidth due to the memory effect. We propose the following three design methods for wide bandwidth, high linearity, and high power applications: 1) Uneven power drive, applying more power to the peaking amplifier, can open the peaking amplifier fully and modulate the load impedances optimally. Therefore, the amplifiers with uneven power drive operate more linear and produce more power than those with an identical input power drive. 2) Because of the improper load modulation, power matching circuits of both amplifiers should be appropriately designed to have low load impedances for better linearity. Due to the low bias point of the peaking amplifier, the power matching circuit of the peaking amplifier should be designed to have lower load impedance than that of the carrier amplifier. Moreover, the matching circuits of both amplifiers should be individually optimized to enhance the IM cancellation over power ranges across the wide bandwidth. 3) The bias circuit should be designed to minimize the memory effects. The linearizing techniques focused on harmonic cancellation such as Doherty amplifier and PD are restricted to a low cancellation limit because the memory effect brings about the different lower and upper spurious emissions. The bias circuit should not have any frequency dispersion of envelope impedance to minimize the memory effect. To reduce the memory effect, the bias circuit is optimized using a quarter-wave bias line and decoupling capacitors for each frequency. The tantalum capacitors are inserted within a quarter-wave bias line for the short at the envelope frequencies. Additionally, the biases of both amplifiers are properly adjusted to maintain optimized linearity and efficiency.

Bias Circuit Test to Reduce the Memory Effects

The effects on the memory effect for different bandwidths are ACLR or intermodulation distortion (IMD) asymmetry and bandwidth dependent adjacent channel leakage ratio (ACLR) or IMD characteristics. To reduce these effects or the memory effects, the load impedances of the bias circuit should be reduced to short the envelope frequency voltage component or maintained at the same value.

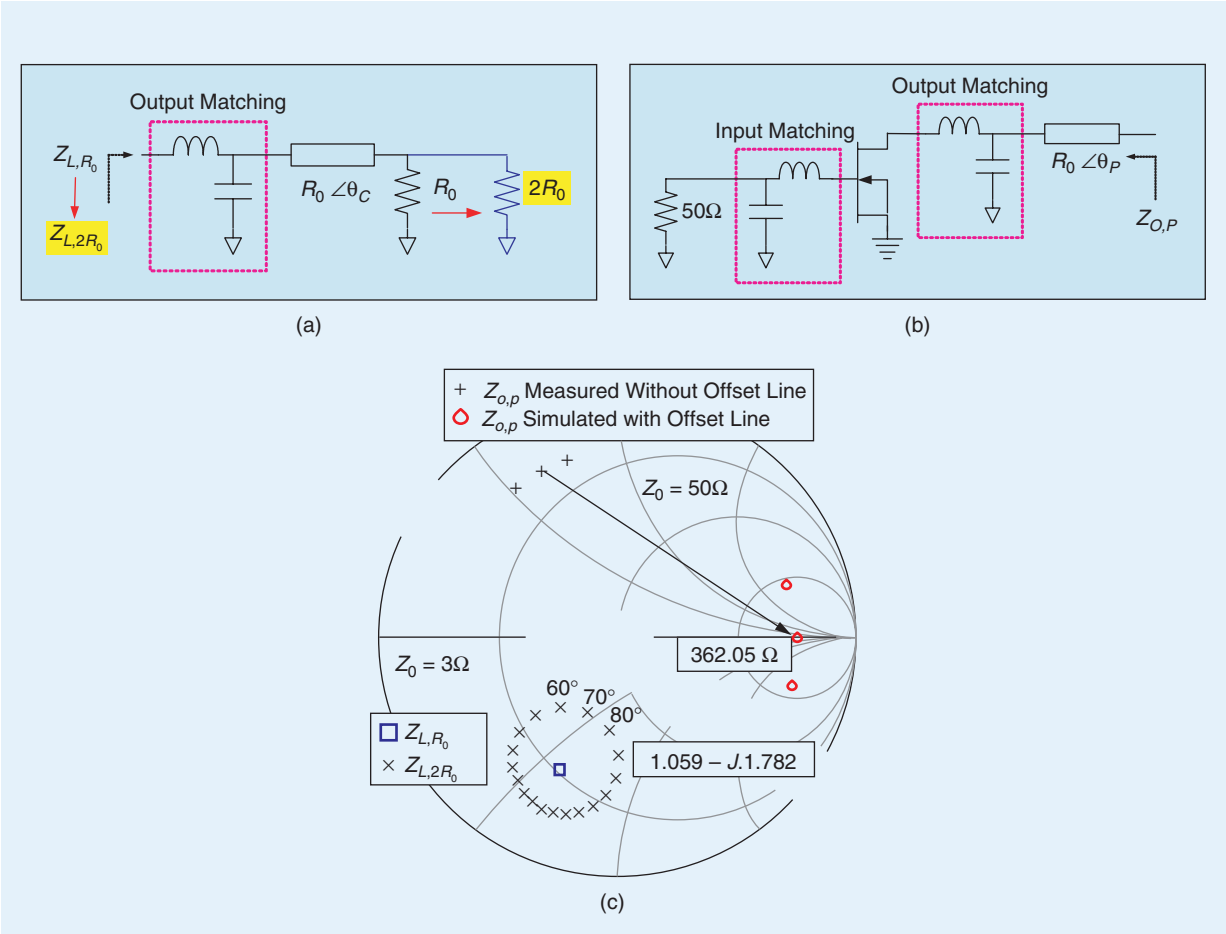

Figure 5. *Schematic diagram to determine the length of the offset line for (a) the carrier amplifier and (b) the peaking amplifier. (c) Smith chart plot of the impedance transformation to determine the length of the offset line; lower: carrier amplifier, upper: peaking amplifier.*

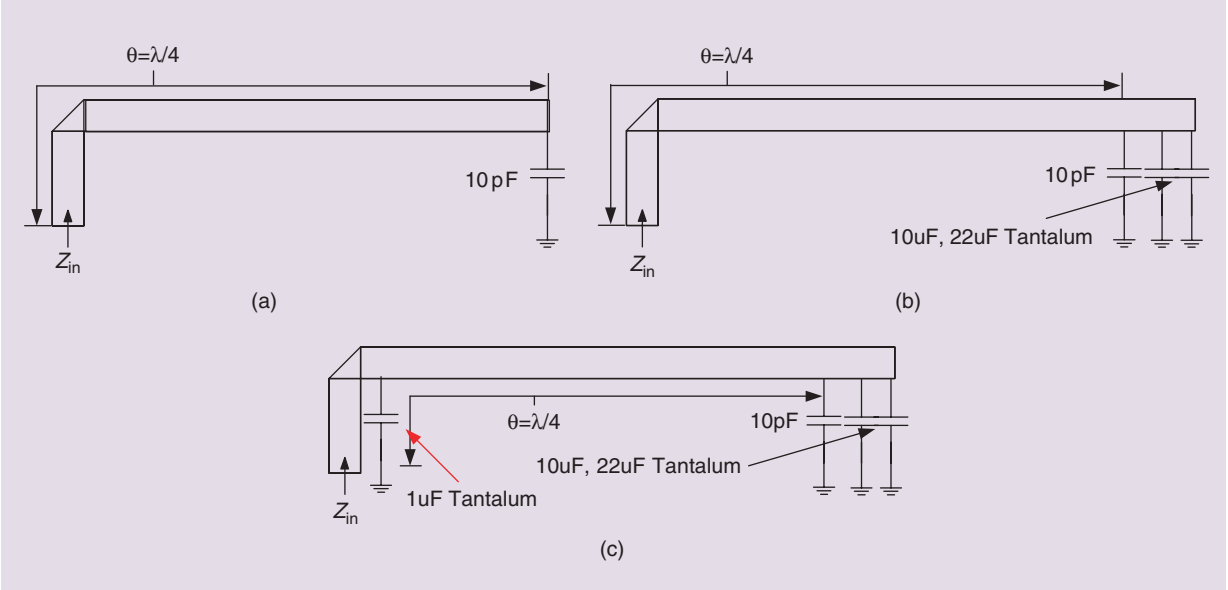

Figure 6. *Schematic diagram of the bias circuits: (a) only RF decoupling capacitor (10 pF), (b) RF decoupling capacitor (10 pF) and envelope frequency decoupling capacitor (22 uF and 10 uF), and (c) RF decoupling capacitor (10 pF) and envelope frequency decoupling capacitor [22 uF, 10 uF, and the tantalum capacitor (1 uF) located within a quarter-wave bias circuit].*

We have tested several bias circuits to reduce the memory effect as shown in Figure 6. Figures 7 and 8 represent measurement results of load impedances corresponding to the bias circuit. Unfortunately, we cannot measure the envelope frequency load impedance (dc–20 MHz), but we have tested the load impedances at 100 MHz–5 GHz. We can analogize the envelope frequency load impedance of the bias circuit from these test results.

The general bias circuit scheme of RF power amplifier is shown in Figure 6(b). From Figures 7 and 8, we have analogized that the envelope load impedances of the RF decoupling capacitor (10 pF) and envelope frequency decoupling capacitor (22 uF and 10 uF) were very small. Even though the envelope load impedances of this case are very small, the power amplifier has the serious memory effect. A cause of this result is that it is very difficult to short the envelope frequency voltage component because the load impedance of the high-power amplifier is very small. To minimize the memory effect, the load impedance of the bias circuit should be further reduced. Thus, we have proposed the bias circuit optimization method of the RF decoupling capacitor (10 pF) and envelope frequency decoupling capacitor [22 uF, 10 uF, and the tantalum capacitor (1 uF) located within a quarter-wave bias circuit], and Figures 7(c) and 8(c) show more small envelope load impedances and lower load impedance variation than the general bias scheme at the low frequency. However, the impedance at RF is reduced by tantalum capacitor located within a quarter-wave bias line as shown in Figure 7(c). Thus, we need to optimize the bias circuit along with the matching circuit considering these effects. As a result, the proposed bias circuit optimization method can reduce the memory effect more efficiently than the conventional bias circuit method, and ACLR asymmetry is reduced.

Implementation of the Doherty Amplifier and Measurement Results

In the previous section, we explained the basic Doherty operation and advanced design methods with uneven power drive, individually optimized matching, and bias circuit optimization. A 2.14-GHz Doherty

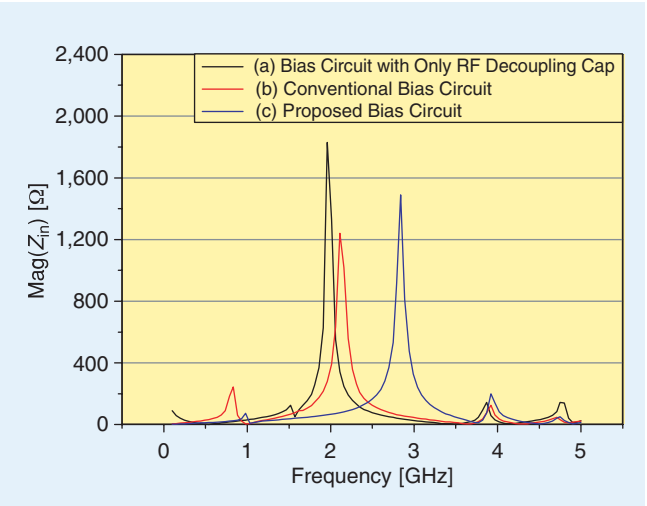

Figure 7. *Measured load impedances of each bias circuit: (a) only RF decoupling capacitor (10 pF), (b) RF decoupling capacitor (10 pF) and envelope frequency decoupling capacitor (22 uF and 10 uF), and (c) RF decoupling capacitor (10 pF) and envelope frequency decoupling capacitor [22 uF, 10 uF, and the tantalum capacitor (1 uF) located within a quarter-wave bias circuit].*

amplifier for the base station power amplifier is implemented using Freescale's MRF5P21180 LDMOSFET. Figure 9 shows a photograph of the implemented Doherty amplifier applying the advanced methods. The uneven power drive is implemented using an Anaren's 1A1305-5 (5 dB directional coupler) which delivers 4 dB more input power to the peaking amplifier than the carrier amplifier. The individual matching of the Doherty amplifier is further optimized to achieve high efficiency and linearity at 25 W (44 dBm) average output power. In the experiments, the suitable offset line is 80.4°, and the transformed output impedance of the peaking amplifier in the off state is 502 Ω.

Quiescent biases for the carrier amplifier and peaking amplifier are set to $V_c = 3.938$ V (1.1 A) and $V_p = 1.713$ V at $V_{dd} = 27$ V, respectively. We optimize the bias circuit to minimize the memory effect and improve the linearity and efficiency. For performance comparison, we also fabricated a class AB amplifier and Doherty amplifier with even power drive. The class AB amplifier represents a conventional base station power amplifier of the push-pull type. For specific comparison corresponding to uneven power drive, the Doherty amplifier with even drive is optimized using the individual matching and bias circuit to achieve linearity and efficiency as high as possible.

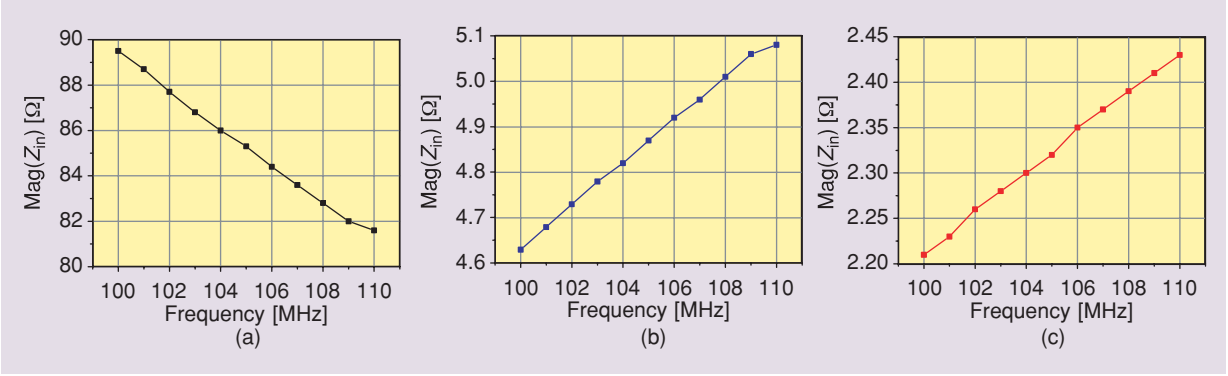

Figure 8. *Measured low frequency load impedances of each bias circuit: (a) only RF decoupling capacitor (10 pF), (b) RF decoupling capacitor (10 pF) and envelope frequency decoupling capacitor (22 uF and 10 uF), and (c) RF decoupling capacitor (10 pF) and envelope frequency decoupling capacitor [22 uF, 10 uF, and the tantalum capacitor (1 uF) located within a quarter-wave bias circuit].*

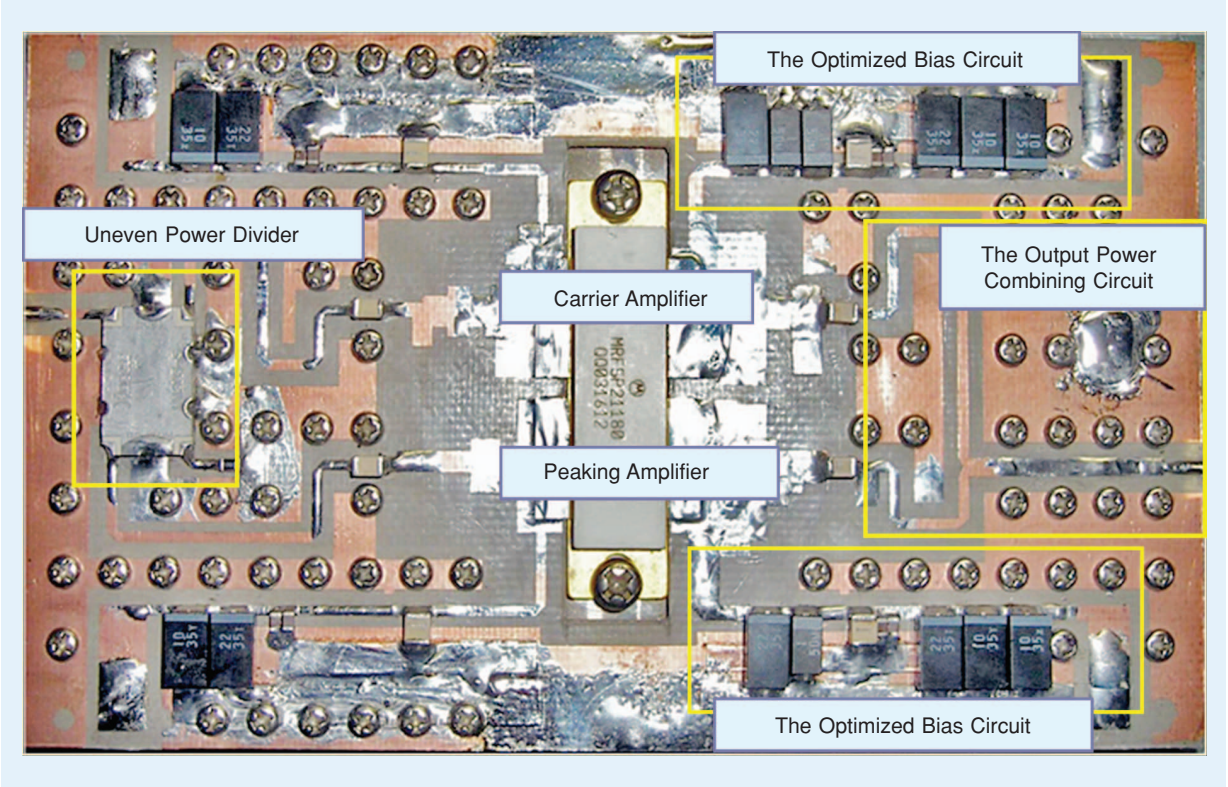

Figure 9. *A photograph of the Doherty amplifier applying the advanced design methods.*

Figure 10 shows the measured adjacent channel leakage ratio (ACLR) of the Doherty amplifier with uneven drive and class AB amplifier at offset 5 MHz for a 2.14-GHz forward link wideband code-division multiple-access (WCDMA) 4FA signal. The ACLR is improved by about 7 dB compared to the class AB amplifier at an output power of 44 dBm.

Figure 11 shows the measured ACLR of the Doherty amplifiers for both even and uneven drives. In comparison with the even case, the Doherty amplifier with uneven power drive delivers significantly improved ACLR performance, by 3 dB at the average output power of 44 dBm.

Figure 12 shows the measured ACLR performance of the uneven case as a function of the bias circuit optimization. The drain bias circuit incorporates a quarter-wave line and several decoupling capacitors which consist of 10 pF for the RF and 22 uF, 10 uF, 1 uF, 1 nF, 150 nF for the envelope frequency. The tantalum capacitors (22 uF, 1 uF) located within a quarter-wave bias line are especially important to minimize the memory effect, even though the impedance at RF is reduced by these capacitors. Thus, we have optimized the bias circuit along with the matching circuit considering these effects. As a result, the bias circuit becomes an active matching circuit, and the difference in ACLR with the bias circuit optimization between lower and upper ACLR is reduced below 2 dB over all average output powers. Figure 13 shows the spectrum of the Doherty amplifier with uneven power drive at an average output power of 44 dBm according to the bias circuit optimization.

Figure 14 shows the measured IMD3 of the Doherty amplifier with both even and uneven power drives for a two-tone signal. We measure a peak envelope power (PEP) using a two-tone signal with 1-MHz tone spacing. The PEP of the amplifier with uneven drive is improved by 15 W, from 165 to 180 W, compared to the even case. This result implies that

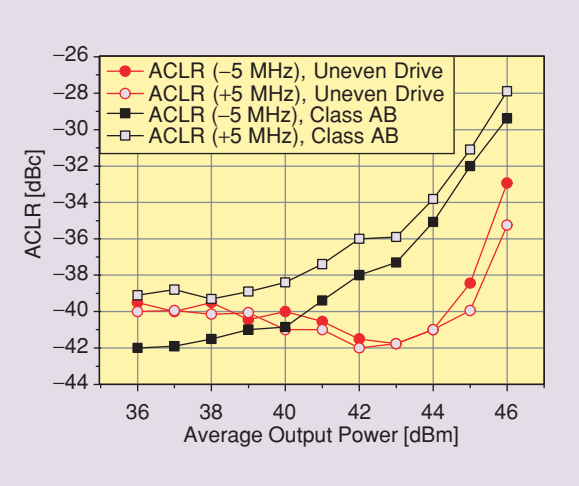

Figure 10. *Measured ACLR performance of the Doherty amplifier with uneven power drive and the class AB amplifier using WCDMA 4 FA signal.*

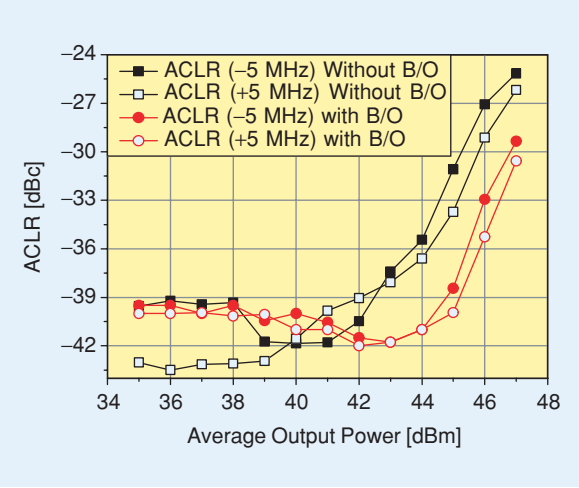

Figure 12. *Measured ACLR performance of the Doherty amplifier according to the bias circuit optimization (B/O).*

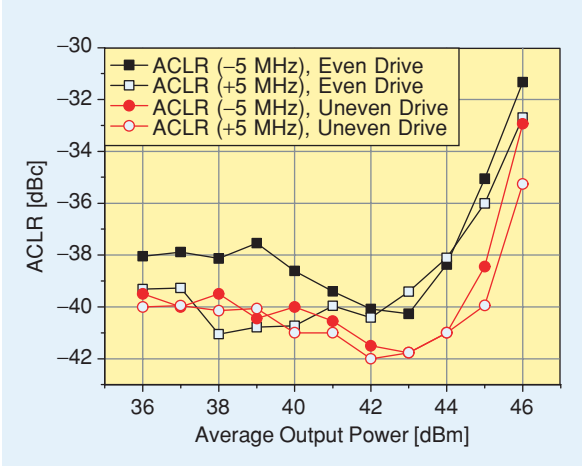

Figure 11. *Measured ACLR performance of the Doherty amplifier with even and uneven power drives using WCDMA 4FA signal.*

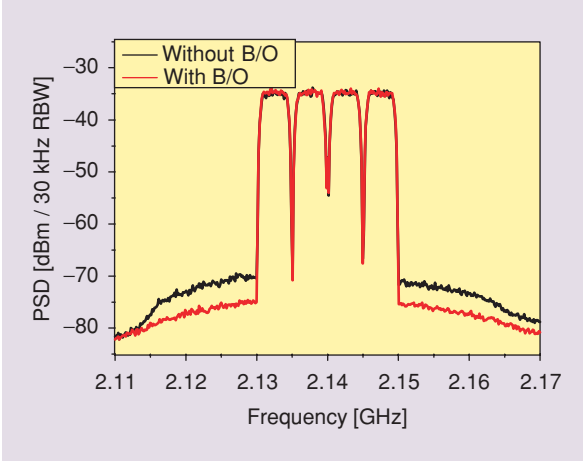

Figure 13. *Output spectrum of the Doherty amplifier with uneven power drive at an average output power of 44 dBm according to the bias circuit optimization (B/O) for WCDMA 4 FA signal.*

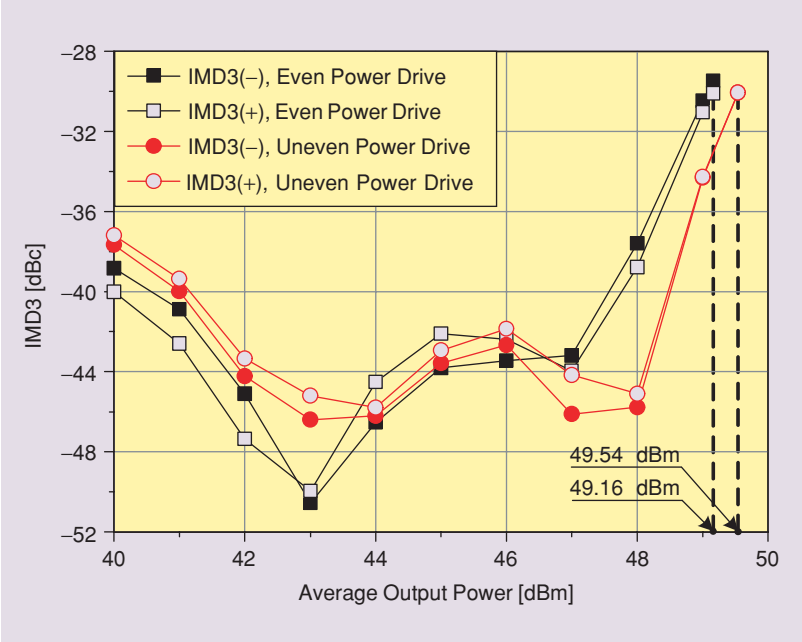

Figure 14. *Two-tone measurement results of the Doherty amplifier with even and uneven power drives.*

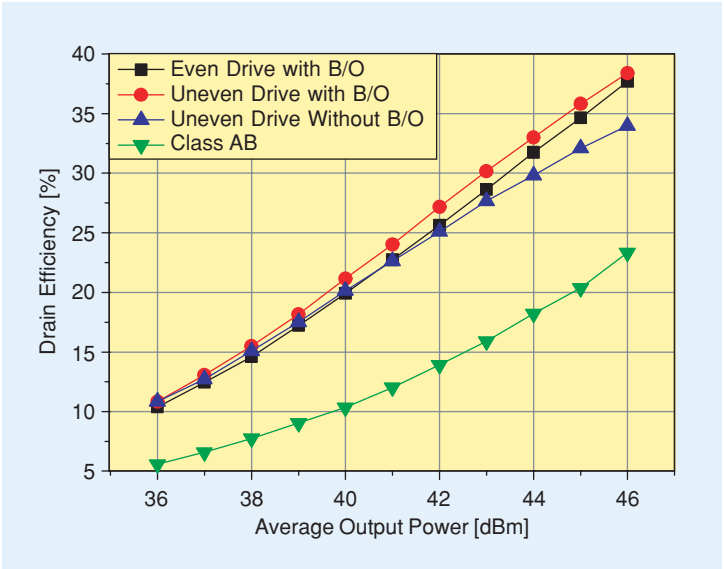

Figure 15. *Measured drain efficiency of the Doherty amplifier with even and uneven power drives according to the bias circuit optimization (B/O) and class AB amplifier for WCDMA 4 FA signal.*

the Doherty amplifier with uneven power drive generates full power from both amplifiers.

Figure 15 shows drain efficiencies of the Doherty amplifier with both even and uneven power drive and the class AB power amplifier for WCDMA 4 FA signal. The drain efficiency of the Doherty amplifier is significantly improved over the class AB amplifier.

These results show clearly that the Doherty amplifier is far superior to the class AB amplifier. The Doherty amplifier with uneven power drive, based on the individually optimized matching circuit and the bias optimization, provides highly efficient and linear operation compared to the normal Doherty amplifier. We can also see that the proposed design method is very helpful in achieving the Doherty amplifier with high performance over a wide bandwidth.

Conclusions

In this article, we explained the basic Doherty operation principle, including both efficiency and linearity improvements, and the circuit configuration of the normal Doherty amplifier. We proposed advanced design methods for highly efficient and linear Doherty amplifier operation across a wide bandwidth. The Doherty amplifier is implemented using Freescale LDMOS MRF5P21180. The amplifier utilizes uneven power drive, individually optimized matching, and bias circuit optimization.

For a 2.14-GHz WCDMA 4 FA signal, the Doherty amplifier has ACLR of −41 dBc and a drain efficiency of 33% at an average output power of 44 dBm. These experimental results clearly demonstrate the superior performance of the Doherty amplifier compared to class AB amplifiers and conventional Doherty amplifiers. The proposed design methods are well suited for the design of the Doherty amplifier for wide-bandwidth and high-power operation.

Acknowledgments

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Reference

[1] S.C. Cripps, *RF Power Amplifiers for Wireless Communications*. Norwood, MA: Artech House, 1999.

[2] W.H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proc. IRE*, vol. 24, no. 9, pp. 1163–1182, 1936.

[3] F.H. Raab, "Efficiency of Doherty RF power amplifier system," *IEEE Trans. Broadcast.*, vol. BC-33, no. 3, pp. 77–83, Sep. 1987.

[4] J. Kim, J. Cha, I. Kim, and B. Kim, "Optimum operation of asymmetrical-cells-based linear doherty power amplifiers-uneven power drive and power matching," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 5, pp. 1802–1809, May 2005.

[5] Y. Yang, J. Yi, Y.Y. Woo, and B. Kim, "Optimum design for linearity and efficiency of microwave doherty amplifier using a new load matching technique," *Microwave J.*, vol. 44, no. 12, pp. 20–36, Dec. 2001.

[6] B. Kim, Y. Yang, J. Yi, J. Nam, Y.Y. Woo, and J. Cha, "Efficiency enhancement of linear power amplifier using load modulation technique," in *Proc. ISMOT' 2001*, Montreal, Canada, June 2001, pp. 505–508.