A Low Phase-Noise CMOS VCO With Harmonic Tuned *LC* Tank

Huijung Kim, Seonghan Ryu, Yujin Chung, Jinsung Choi, and Bumman Kim, *Senior Member, IEEE*

***Abstract*—This paper presents a phase-noise reduction technique for voltage-controlled oscillators (VCOs) using a harmonic tuned (HT) *LC* tank. The phase-noise suppression is achieved through almost rectangular-shaped voltage at the switching differential cell, which effectively maximizes the slope of the switching cell output voltage at a zero crossing point. In addition, the proposed technique also suppresses the down-conversion of the noise around the second harmonic frequency by the second harmonic short of the tank. One second HT VCO and two third HT VCOs are designed and implemented to evaluate the concept using a 0.35- and 0.13-μm CMOS process. The figure-of-merit (FOM) of the second HT VCO, third HT VCO1, and third HT VCO2 are −180.7, −183.7, and −189.5, respectively. The best FOM performance of the VCO has phase noises of −100.4, −132.0, and −140.8 dBc/Hz at 100-kHz, 1-MHz, and 3-MHz offset frequencies at the 2-GHz carrier, respectively. This VCO consumes 3.29 mA from a 1.8-V supply with the silicon area of 500 μm × 750 μm.**

***Index Terms*—CMOS, harmonic tuned (HT) *LC* tank, low phase noise, voltage-controlled oscillator (VCO).**

I. Introduction

A MAJOR challenge in the wireless industry is the high-level integration of functional blocks using low-cost CMOS technology. Among the efforts for the single-chip radio integration, the implementation of a low phase-noise voltage-controlled oscillator (VCO) attracts a lot of attention because a phase noise of the VCO is one of the most critical parameters for the quality of service of the information transfer function. As CMOS downscaling is in progress for high level integration at a low cost, the $1/f$ corner frequency of the small-size transistors tends to increase and this is the crucial problem of the CMOS VCO. Moreover, the integration of a high-Q *LC* tank is not easy due to the low resistivity of the silicon substrate, and this greatly affects the phase-noise performance. This paper presents an optimization technique for the phase-noise performance of the CMOS *LC* VCO, which reduces the flicker noise dominated $1/f^3$-shaped part and thermal noise dominated $1/f^2$-shaped part of the noise spectrum. The phase-noise suppression is achieved through almost rectangular-shaped voltage at the switching differential cell, which effectively maximizes the slope of the switching cell output voltage at the zero crossing point. In addition, the proposed technique also suppresses down-conversion of the noise around $2f_0$ to the phase noise by the second harmonic short of the tank. The optimized CMOS differential VCO delivers a measured phase noise, which is 10 dB lower than a conventional one in both $1/f^3$ and $1/f^2$ regions.

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II. Phase-Noise Issues and VCO Design

A. Phase-Noise Minimization

Recently, the theory and analysis for the physical processes of the phase noise in differential oscillators have made significant progress, and the techniques to lower the phase noise have advanced through the understanding of these phase-noise mechanisms [1], [2]. The phase noise is mainly induced from various mixing phenomena of the negative g_m switching differential pair. One of the main mixing phenomena is up- and down-conversion from the thermal noise component at the baseband and the harmonics of the oscillation frequency. The other one is up-conversion from the flicker noise in baseband to the phase noise in the fundamental frequency. The well-known phase-noise model for an oscillator is Leeson's proportionality [3]

$$L\{\Delta\omega\} \propto \frac{1}{V_o^2} \cdot \frac{kT}{C} \cdot \left(\frac{\omega_o}{Q}\right)^2 \cdot \frac{1}{\omega_m^2}. \tag{1}$$

In (1), the phase noise is given as kT/C noise that is shaped in the frequency domain by an *LC* tank and normalized to the power in the tank. Phase noise is scaled by a specific noise factor F, which has been extracted recently for an *LC* oscillator [1] from the noise model of mixer with a switching differential pair [4]. The noise factor is given by

$$F = 2 + \frac{8\gamma IR}{\pi V_o} + \gamma\frac{8}{9} \cdot g_{m\mathrm{bias}} \cdot R \tag{2}$$

where $\mathbf{I}$ is the bias current, γ is the channel noise coefficient of the field-effect transistor (FET), R is the load resistance, and $g_{m\mathrm{bias}}$ is the transconductance of the current–source FET [4]. The first and second terms in (2) describe the phase-noise contributions from the resonator loss and differential-pair FETs, respectively. The third term in (2) signifies the phase noise produced by down-conversion of the CS noise component at the second harmonic of the oscillation frequency. The second term can be reduced by increasing V_o, which is the voltage across the

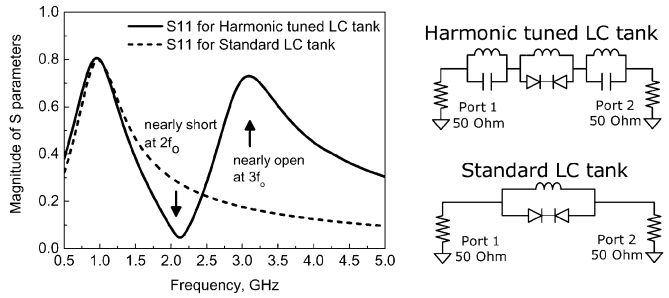

Fig. 1. Simulated S-parameters of the two tanks for 50-Ω terminations.

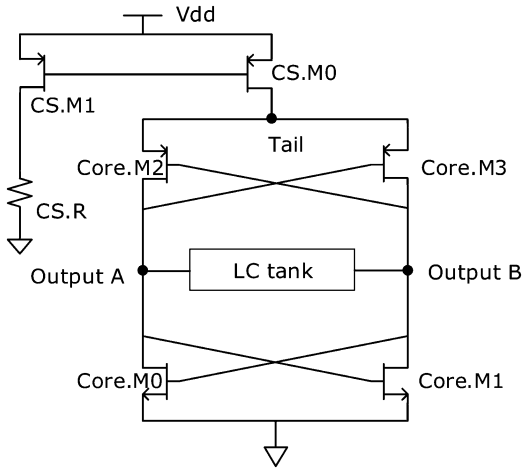

Fig. 2. Schematic view of the third HT *LC* VCO.

resonator and is proportional to the slope at the zero crossing voltage of the switching cell [4]. Thus, increasing V_o means a steep rise at the zero crossing point. To realize the concept, we have employed a harmonic tuned (HT) *LC* tank, which can deliver a square waveform voltage to the cell [5]. From this concept, we have fabricated three VCOs and compared them with the standard VCOs.

B. Third HT LC Tank Design

The proposed *LC* tank is tuned up to the third harmonics, open at the fundamental frequency and third harmonic, and short at the second harmonic, as shown in Fig. 1. The center tank resonates at the fundamental frequency and the two side tanks resonate at the third harmonic, while the combined one provides the second harmonic short. Fig. 2 shows the schematic of the differential *LC* VCO with the tanks. The simulated output waveforms of the oscillator at the output node A and B of Fig. 2 are shown in Fig. 3. This waveform indicates the reduced noise from the switching core. The HT *LC* tank presents shortness at the second harmonic and stabilizes the tail voltage fluctuation, as shown in Fig. 4. Thus, through harmonic tuning, we can reduce the phase noise induced by the CS. Actually, since the phase noise from the resonator loss is also induced via modulation of zero crossing instants of the differential pair, harmonic tuning can also reduce the resonator noise portion.

The phase-noise close-in to the oscillation frequency is dominated by the flicker noise up-conversion and has a slope of

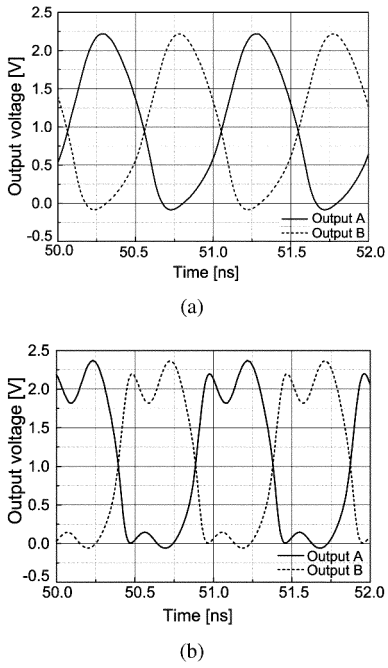

Fig. 3. Simulated output voltage waveform for: (a) standard *LC* VCO and (b) third HT *LC* VCO.

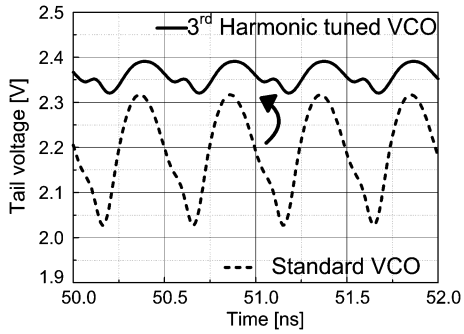

Fig. 4. Stabilization of the tail voltage fluctuation by the third harmonic tuning.

-30 dB/decade. The noise sources for the up-conversion are the tail current source (CS) and negative g_m switching differential pair. The flicker noise from the tail CS is converted to f_0 due to the mixing action of the VCO circuit and the noise is delivered to the resonator as an AM noise [6]. After that, the AM noise is converted into an FM noise by the tuning varactor [1]. The FM sidebands appear as the close-in phase noise. The AM to FM conversion depends on the gain of the varactor and can be minimized by reducing the size of the CMOS varactor, while a wide tuning can be implemented by a capacitor array, which is switched on and off in parallel with the *LC* tank [2]. The switched tuning method is not adopted in this paper for a simple structure. Instead, a pMOS CS with a large gate length of 3 μm is used for less $1/f$ noise generation.

Additionally, the tail node (the common mode node of the CS) oscillates at twice of the oscillation frequency $2f_0$ because the CS is pulled every time each nMOS (PMOS) transistor of the differential pair switches on. As a result, the flicker noise of the CS is up-converted to $2f_0$ through channel length modulation and it is mixed down to the oscillation frequency again

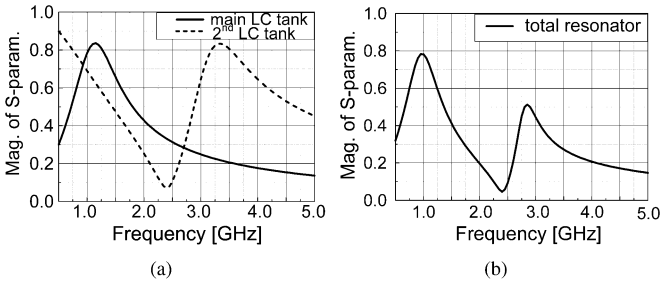

Fig. 5. Simulated result of the magnitude of the S-parameter of: (a) main and second harmonic tuning *LC* tanks and (b) total second HT *LC* tank.

and presents the close-in phase noise [6]. Therefore, to minimize the up-conversion of flicker noise from the tail CS, all even harmonics must be suppressed. The suppression of $2f_0$ made by the second harmonic short circuit at the tail node (the common-mode node of the CS) can minimize the phase noise from the CS. The flicker noise from the switching differential pair modulates the second harmonic voltage waveform at the common source node in every half period, which induces a noisy current in the parasitic capacitance at the source of each switching pair. This current is mixed down to the fundamental frequency by the switching pair, inducing the close-in phase noise. This phase noise is actually a small portion due to the switching nature of the oscillator, but this portion can be increased with downscaling of CMOS to nanosize. Though the CS flicker noise can be minimized by using MOS transistors with relatively large gate length, the nanosize transistors should be used for the switching pair for high-frequency operation and can be a problem in the nano-CMOS process. The $1/f$ noise in MOSFET is mainly caused by the carrier (de)trapping in localized oxide states. The switching with 50% duty cycle removes all memory in a silicon oxide state and it can be a means to reduce the $1/f$ noise itself by forcing the trap to release its captured electron [7]. The proposed harmonic tuning makes the oscillating wave rectangular, much like an ideal switching with 50% duty cycle. As a result, it can reduce the $1/f$ noise at the switching core.

C. Second HT LC Tank Design

The third HT *LC* tank can reduce the phase noise significantly by maximizing the slope of the output voltage wave at the zero crossing point and by suppressing the second harmonic at the tail node. However, it needs two inductors, which increase the chip area. To compromise the tradeoff between the slope at the zero crossing point and chip size, we have tried the second HT *LC* tank. Similar to the third HT tank, the second HT *LC* tank is open at the fundamental frequency and short at the second harmonic, as shown in Fig. 5. Fig. 6 shows the proposed VCO with the second HT *LC* tank. It reduces the second harmonic power at the drain of the CS. The VCO also increases the slope of the output voltage wave at the zero crossing point, as shown in Fig. 7. Table I shows the simulated phase-noise contribution for the standard and second tuned *LC* VCOs at 100-kHz offset from the center frequency. The proposed second harmonic tuning technique can suppress the phase noise from various noise sources including the negative g_m core transistors. Fig. 8

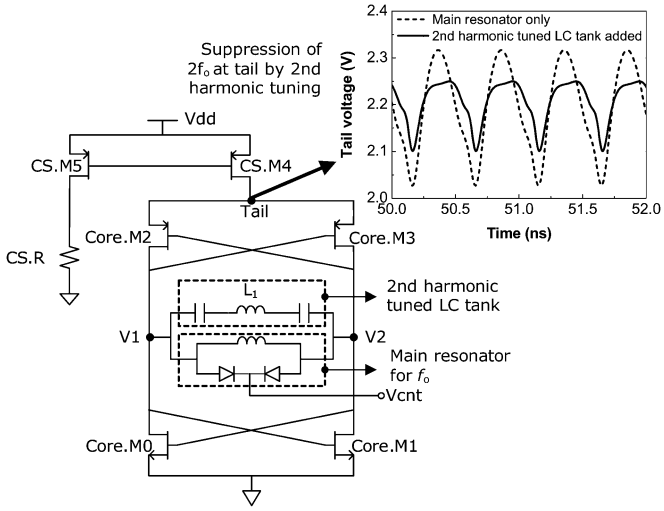

Fig. 6. VCO with the second HT *LC* tank.

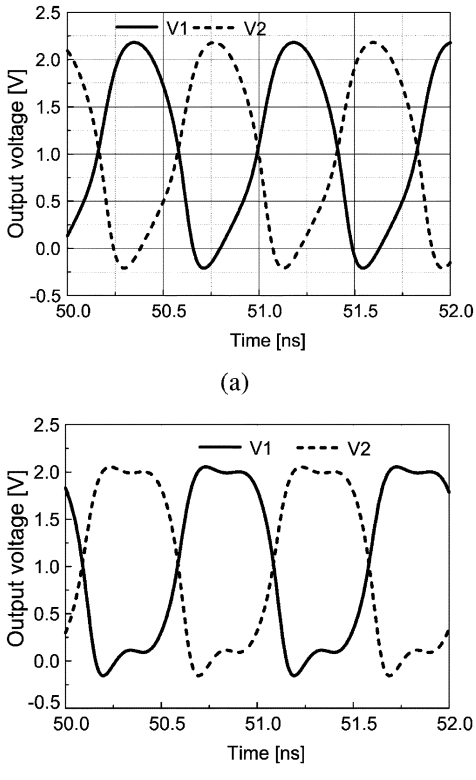

Fig. 7. Simulated output voltage waveform for: (a) standard *LC* VCO and (b) second HT *LC* VCO.

shows the simulated phase noises of VCO1, VCO2, and VCO3 at 1-GHz carrier frequency as a function of the offset frequency and at offset frequencies of 100 kHz and 3 MHz as a function of carrier frequency. VCO1 is a standard *LC* VCO, VCO2 is the second HT *LC* VCO, and VCO3 is a standard VCO, which has bigger capacitor to fit the oscillation frequency to VCO2. Since the VCO2 has larger parasitic capacitance than VCO1 due to some additional component, the VCO1 has slightly higher carrier frequencies than VCO2. To compare phase noises between VCOs with the same carrier frequency, the phase noise of

TABLE I
PHASE-NOISE CONTRIBUTION OF THE SECOND HT *LC* VCO

VCO 1 (1.18 GHz)			VCO 2 (1 GHz)		
Noise sources	Noise Contribution (V^2/Hz)	% of Total	Noise sources	Noise Contribution (V^2/Hz)	% of Total
CS.M5,th	3.90e-12	13.76	CS.M5, th	1.05e-12	17.49
Core.M1, th	3.61e-12	12.75	CS.M4, th	8.07e-13	13.41
Core.M0, th	3.61e-12	12.75	CS.M5, fl	7.34e-13	12.18
CS.M4, th	3.60e-12	12.73	Core.M1,th	6.90e-13	11.46
CS.M5, fl	2.71e-12	9.58	Core.M0,th	6.90e-13	11.46
Core.M0,fl	2.29e-12	8.08	CS.M4,fl	3.50e-13	5.81
Core.M1,fl	2.29e-12	8.07	CS.R, rn	3.08e-13	5.11
CS.M4, fl	1.44e-12	5.09	Core.M2, th	2.24e-13	3.72
CS.R, rn	1.14e-12	4.02	Core.M3, th	2.24e-13	3.72
Core.M2, th	1.06e-12	3.75	Core.M0,fl	1.90e-13	3.15
Core.M3, th	1.06e-12	3.75	Core.M1,fl	1.90e-13	3.15

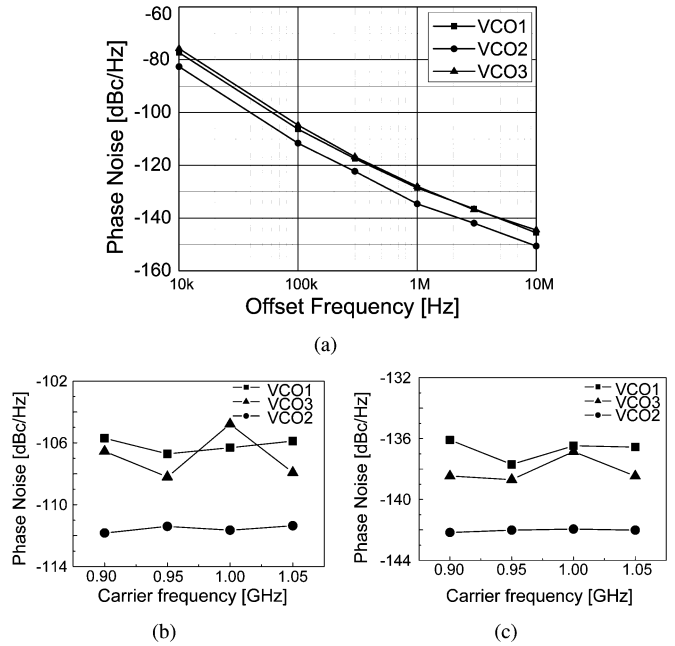

Fig. 8. Simulated phase noise of the three VCOs: (a) at 1-GHz carrier frequency and at (b) 100-kHz and (c) 3-MHz offset frequencies.

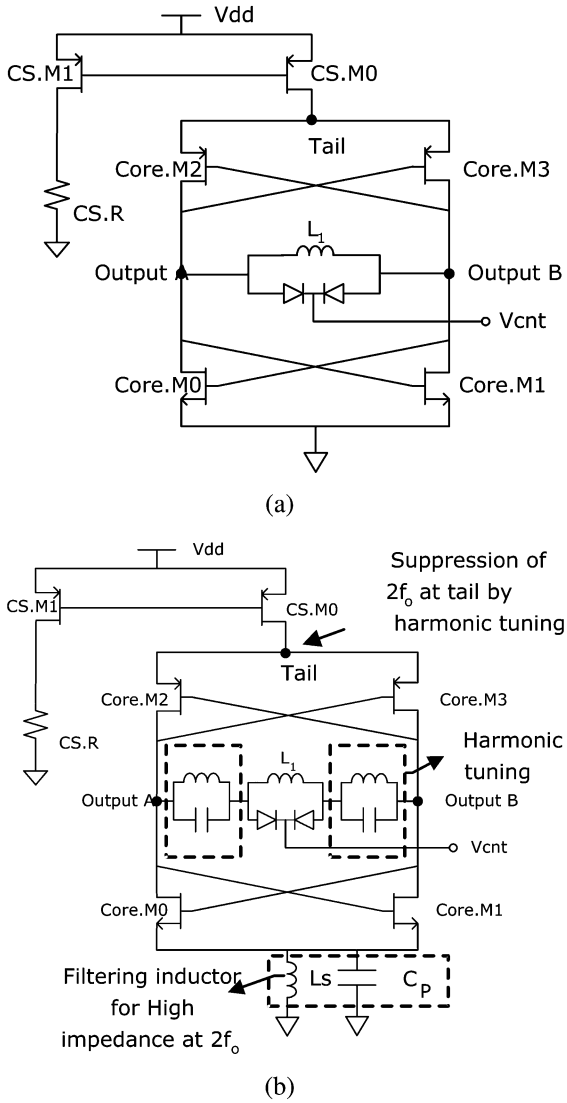

Fig. 9. Simplified schematic diagrams of: (a) standard VCO and (b) optimized HT VCO.

VCO3 is added in Fig. 8. The phase-noise improvement of the second HT *LC* VCO is 3–6 dB in all oscillation frequencies.

D. Third HT LC Tank With Noise Filtering Technique

The harmonic tuning technique reduces the switching time, from the on to the off state, of the negative g_m cell by increasing the slope of the output voltage wave at the zero crossing point. However, it cannot reduce the phase noise from the device itself. To reduce the phase noise effectively, the noise filtering technique is commonly adopted [2]. In a standard top-biased VCO, the common-source node of the N-MOS switching pair is connected to the ground. It forces one of the N-MOSs into the triode region as the rising differential oscillation voltage crosses V_T. Thus, the average resonator Q factor over a full oscillation cycle is reduced, degrading the overall phase noise. The filtering, by parallel resonation at $2f_0$ frequency using an inductor with the parasitic capacitor at the common source, stops the differential-pair FETs in the triode region from loading the resonator, preventing the degradation of the resonator Q [2]. As shown in Fig. 9, an L_S is used to make a parallel resonation with the parasitic capacitance C_P at $2f_0$ frequency. This technique has an independent phase-noise reduction effect and the combination of the harmonic tuning and filtering techniques can reduce the phase noise significantly for $1/f^3$ and $1/f^2$ regions [8]. Using these techniques, a complementary VCO is designed to achieve the minimum phase noise. The phase-noise simulation results in Fig. 10 show the phase-noise reduction effect of each technique independently and also that of the combined case. The phase-noise contributions of the various noise components of the test VCO at 100-kHz offset frequency are summarized in Table II. The contribution of the phase noise from the $1/f$ noise at the negative g_m cell is dramatically reduced, as shown in Table II.

III. MEASUREMENT RESULTS

In this study, three types of VCOs are designed, implemented, and measured. The first one is the VCO with the second HT LC

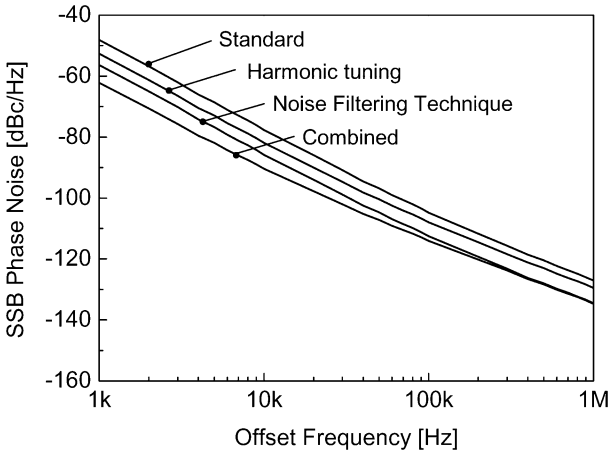

Fig. 10. Simulated phase-noise results for each technique.

TABLE II
PHASE-NOISE CONTRIBUTION OF THE OPTIMIZED VCO

Standard LC VCO			Optimized LC VCO		
Noise sources	Noise Contribution (V^2/Hz)	% of Total	Noise sources	Noise Contribution (V^2/Hz)	% of Total
Core.M0, fl	4.53e-12	18.23	CS.M0, th	4.24e-13	11.03
Core.M1, fl	4.53e-12	18.23	CS.M1, th	4.24e-13	11.03
CS.M1, th	3.77e-12	15.16	Core.M3, th	4.00e-13	10.43
CS.M0, th	2.69e-12	10.81	Core.M2, th	4.00e-13	10.43
CS.M1, fl	2.39e-12	9.60	Core.M0, th	2.75e-13	7.16
Core.M1, th	1.50e-12	6.04	Core.M1, th	2.75e-13	7.16
Core.M0, th	1.50e-12	6.04	CS.M1, th	2.68e-13	6.97
CS.R, rn	1.17e-12	4.70	Reso.L1,rn	1.76e-13	4.58
CS.M0, fl	1.09e-12	4.38	Core.M0, fl	7.74e-14	2.1
Reso.L1,rn	3.61e-13	1.45	Core.M1, fl	7.74e-14	2.1

tank, the second one is the VCO with the third HT LC and noise filtering technique [8], and the last one [9] is the same architecture of the second one, but it is designed with another process to check the dependency for another process and frequency. The first is called the "second HT VCO," the second one is called the "third HT VCO1," and the last one is called the "third HT VCO2."

The "second HT VCO" and "third HT VCO1" are fabricated in a 0.35-μm CMOS process of STMicroelectronics, Paris, France. The "third HT VCO2" is fabricated in a 0.13-μm CMOS process of the Samsung Electronic Company Ltd., Yongin, Gyeunggi, Korea. The chips are measured on an HP4352S VCO/phase locked-loop (PLL) signal test system.

A. *Second HT VCO*

The microphotograph of the fabricated chip with a 0.6 mm $\times$ 0.65 mm area is shown in Fig. 11. The frequency of oscillation could be tuned from 900 MHz to 1.05 GHz, which yields a tuning range of approximately 15%. Fig. 12(a) shows the phase noise versus the offset frequency for the standard VCO and second HT VCO at 1 GHz. Fig. 12(b) and (c) shows the phase noise of the two VCOs as a function of the carrier frequency, measured at offset frequencies of 100 kHz and 3 MHz, respectively. The phase-noise reduction by the second harmonic tuning is from 4 to 7 dB. These measurement results show a good agreement with the simulation results, as shown in Fig. 8.

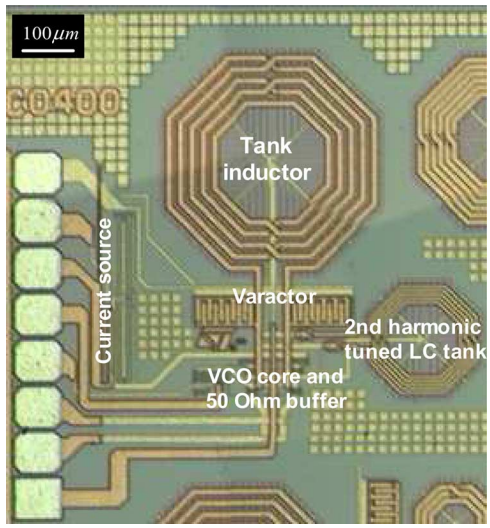

Fig. 11. Microphotograph of the second HT VCO. (Color version available online at: http://ieeexplore.ieee.org.)

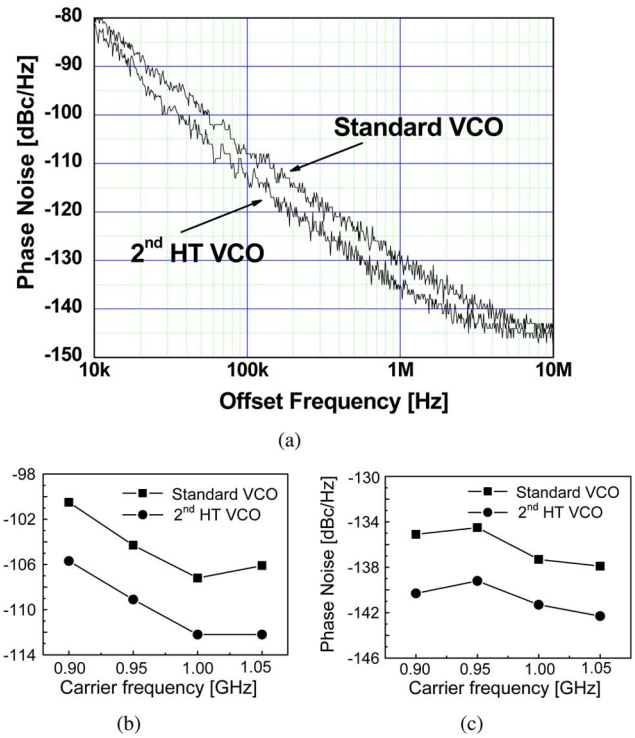

Fig. 12. Measured phase noise of the standard VCO and second HT VCO: (a) at 1-GHz carrier frequency and at (b) 100-kHz and (c) 3-MHz offset frequencies. (Color version available online at: http://ieeexplore.ieee.org.)

B. *Third HT VCO1*

The microphotograph of the fabricated chip with 1.2 mm $\times$ 0.43 mm area is shown in Fig. 13. The VCO is tunable between 800 MHz and 1.1 GHz. Fig. 14 shows the phase noise versus the offset frequencies for the standard VCO and third HT VCO. The phase-noise reduction by the third harmonic tuning and noise filtering techniques is from 7 to 11 dB for the entire frequency range. The VCO achieves -89, -116, and -135 dBc/Hz at 10-kHz, 100-kHz, and 1-MHz offset frequencies from the carrier, respectively.

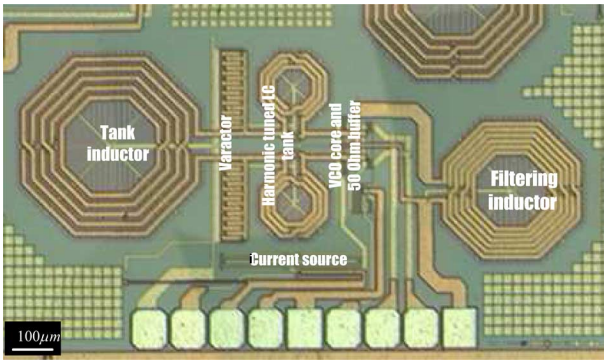

Fig. 13. Microphotograph of the third HT VCO1. (Color version available online at: http://ieeexplore.ieee.org.)

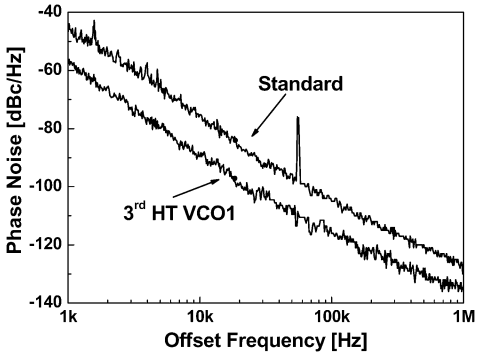

Fig. 14. Measured phase noises of the standard VCO and third HT VCO1.

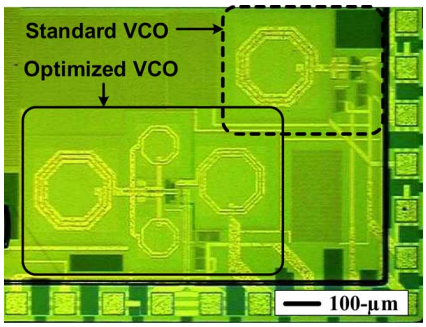

Fig. 15. Microphotograph of the third HT VCO2. (Color version available online at: http://ieeexplore.ieee.org.)

C. Third HT VCO2

The microphotograph of the fabricated chip is shown in Fig. 15 with 0.3 mm $\times$ 0.5 mm and 0.5 mm $\times$ 0.85 mm areas for the standard and optimized VCO, respectively. Since the area of the optimized VCO is not effectively utilized for these test chips due to the location of the RF PADs, the increment of the area is relative large for the third HT VCO1. The VCO is tunable from 1.89 to 2.17 GHz. Fig. 16 shows the phase noise versus the offset frequencies for the standard VCO and third HT VCO2. The phase-noise reduction due to the third harmonic tuning and the noise filtering techniques is over 10 dB at the same frequency shown in Fig. 17. The VCO achieves -101.3, -132.0, and -140.8 dBc/Hz at 100-kHz, 1-MHz, and 3-MHz offset frequencies from the carrier, respectively. Fig. 17 shows the phase-noise improvements for all control voltages for the standard and optimized VCOs at 100-kHz offset frequency.

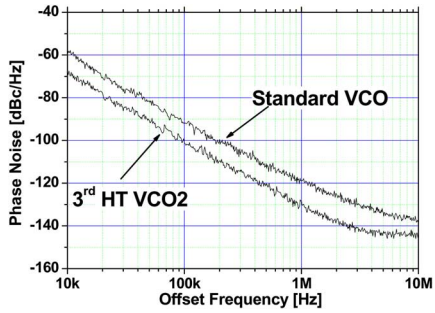

Fig. 16. Measured phase noises of the standard VCO and third HT VCO2. (Color version available online at: http://ieeexplore.ieee.org.)

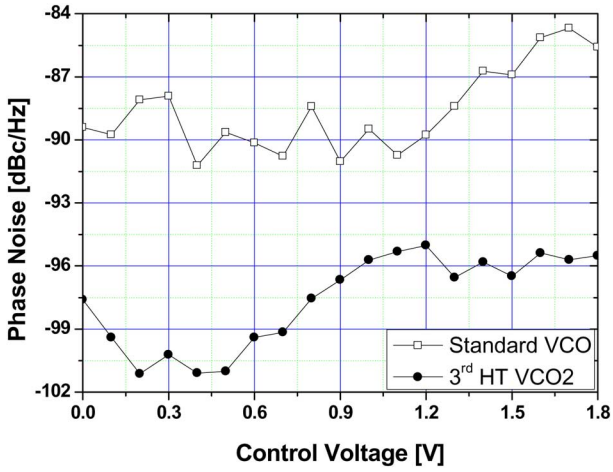

Fig. 17. Measured phase noise versus control voltage at 100-kHz offset frequency. (Color version available online at: http://ieeexplore.ieee.org.)

TABLE III
SUMMARY OF THREE VCO PERFORMANCES

VCO	Tech.	Frequency [GHz]	Power (V_{DD} * I_{DD})	Phase Noise [dBc/Hz] type	@100KHz	@ 1MHz
2nd HT VCO	0.35um CMOS	0.9~1.05	2.7V * 5.4mA	basic	-106.2	-126.9
				Opt.	-111.2	-132.4
3rd HT VCO1[8]	0.35um CMOS	0.8~1.1	2.7V * 5.4mA	basic	-106.2	-126.9
				Opt.	-115.8	-135.4
3rd HT VCO2[9]	0.13um CMOS	1.89~2.17	1.8V * 3.3mA	basic	-91.24	-121.0
				Opt.	-100.4	-132.0

Table III shows the summary of three VCO performances. A figure-of-merit (FOM) has been defined in [10] to compare the VCOs' performances

$$\mathrm{FOM} = L(\Delta\omega)\left[\frac{\mathrm{dBc}}{\mathrm{Hz}}\right] + 10\cdot\log(P_{\mathrm{DC}}[\mathrm{mW}]) - 20\cdot\log\left(\frac{\omega_o}{\Delta\omega}\right) \quad (3)$$

where $L(\Delta\omega)$ is the total single-sideband phase-noise spectral density at an offset frequency $\Delta\omega$, P_{DC} is total VCO power consumption, and ω_0 is the pulsation of oscillation. The FOMs of the second HT VCO, third HT VCO1, and third HT VCO2 are

TABLE IV
VCO PERFORMANCE COMPARISON

VCO	Tech.	Freq. [GHz]	Power [mW]	Phase Noise [dBc/Hz]	FOM
[5]	0.35um Bi-CMOS	1	14.5	-130.4 @1 MHz	-178.8
[11]	0.35um Bi-CMOS	1.91	10	-121 @600 KHz	-181.1
[12]	0.35um Bi-CMOS	5.6	13.5	-117 @1 MHz	-180.7
[13]	0.13um CMOS	3.0-5.6	2	-114.5 @1 MHz	-186.5
[14]	0.18um CMOS	5.2	17.25	-126 @1 MHz	-188.2
[15]	0.35um CMOS	2.19	12.6	-139 @3 MHz	-185.3
2nd HT VCO	0.35um CMOS	1	14.58	-132.4 @1 MHz	-180.7
3rd HT VCO1 [8]	0.35um CMOS	1	14.58	-135.4 @1 MHz	-183.7
3rd HT VCO2 [9]	0.13um CMOS	2.17	5.92	-132 @1 MHz	-189.5

-180.7, -183.7, and -189.5, respectively. Table IV compares the FOMs of our VCOs with those of state-of-the-art VCOs reported [11]–[15].

IV. CONCLUSIONS

We have presented a technique to lower the phase noise of *LC* oscillators using the HT *LC* tank. The phase-noise suppression is achieved through almost rectangular-shaped voltage at the switching differential cell, which effectively maximizes the slope of the switching cell output voltage at zero crossing point. Beside the sharp switching, the proposed technique suppresses the down-conversion of the noise around the second harmonic frequency by the second harmonic short of the tank. It also reduces the differential pair flicker noise itself and is useful to down-scaling of CMOS technology. Three VCOs are implemented and measured to check the concept. To compromise the tradeoff between the slope at a zero crossing point and chip size, we have tried the second HT *LC* tank. The second HT *LC* VCO has less phase-noise improvement than the third HT *LC* VCO, but is smaller than the third one. The improvement of the proposed technique appears over a broad control voltage range. The measured FOM of the second HT VCO, third HT VCO1, and third HT VCO2 are -180.7, -183.7, and -189.5, respectively. The best performance of the VCO has phase noises of -100.4, -132.0, and -140.8 dBc/Hz at 100-kHz, 1-MHz, and 3-MHz offset frequencies from the 2-GHz carrier, respectively.

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