# A $\Delta\Sigma$-Digitized Polar RF Transmitter

Jinsung Choi, *Student Member, IEEE*, Jounghyun Yim, Jinho Yang, Jingook Kim, Jeonghyun Cha, Daehyun Kang, Dongsu Kim, and Bumman Kim, *Fellow, IEEE*

***Abstract*—This paper demonstrates a new polar transmitter architecture, which uses the digitized envelope signal to control the drain voltage of a switching mode power amplifier (PA). It is based on a novel polar modulation using the constant envelope modulated signal. Among the various constant envelope modulators, the $\Delta\Sigma$ modulator is chosen for its noise-shaping characteristic. It enables the use of a highly efficient switching amplifier with high linearity. For demonstration, the overall transmitter is implemented and tested with a code-division multiple-access IS-95A signal. The class-D and class-F amplifiers are designed and compared for the optimum operation. The experimental results show that the amplifier with small device size is suitable for this application because of the fast switching requirement. For the class-F amplifier, the measured power-added efficiency is 51.7% at 22.1 dBm and the overall efficiency (considering the amplified quantization noise) is 31%. The adjacent channel power ratios at 885 kHz and 1.98 MHz are lower than −44.9 and −55.6 dBc at the output power range from 10.8 to 22.1 dBm without any pre-distortion techniques. The overall efficiency is improved to 48.6% with a three-level quantized $\Delta\Sigma$ modulator. The results clearly show that the highly efficient switching mode PA can be controlled efficiently using a digital signal from the $\Delta\Sigma$ envelope modulation technique.**

***Index Terms*—Code division multiple access (CDMA), constant envelope modulator, efficiency, IS-95A, linearity, multibit, polar modulator, power amplifier (PA), RF transmitter, sigma–delta, $V_{\mathrm{DS}}$-to-phase modulation ($V_{\mathrm{DS}}/\mathrm{PM}$).**

## I. Introduction

FLEXIBLE transmitters handling multimode and multiband are inevitable for the evolution of the wireless communication system. The flexibility of the digital signal processing (DSP)-based system has enabled the multimode operation of the baseband modem chips, but the multimode and multiband operation in the analog and RF area is not familiar yet. Recently, as the CMOS-based DSP technology evolves, there are many efforts to migrate the radio function into the DSP and to control the radio function using the DSP [1]–[6].

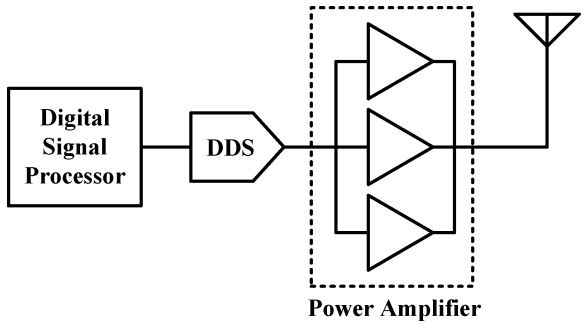



Fig. 1. Next-generation transmitter architecture.

Digital radio provides many benefits including robustness to variations from component inaccuracies and aging. Moreover, a smaller circuit area from a higher integration level of Si CMOS technology and lower fabrication cost are allowed. As the technology advances toward higher speed of operation, the transmitter, employing a direct-digital synthesizer (DDS), as shown in Fig. 1, will arrive at the terminal. It directly synthesizes the microwave signal from the digital processor and the only analog component in the transmitter chain is the power amplifier (PA).

The PA should be highly linear for the increased bandwidth and peak-to-average power ratio (PAPR) of the signals as the wireless services move to fourth generation (4G) for higher data rate. It also requires high efficiency for long battery lifetime, but the linear operation necessitates the tradeoff with the efficiency, i.e., the approach for the next-generation transmitter should be accompanied by the highly efficient and linear PA. The switching mode PA is so efficient that it is suitable for the portable handset applications requiring long battery time. However, the nonlinear characteristic of the switching amplifier makes it hard to deal with the time-varying envelope signals, and the direct adoption of switching amplifier is inappropriate. The linear amplification using nonlinear components (LINCs) [10], bandpass $\Delta\Sigma$ modulation ($\mathrm{BP}\Delta\Sigma\mathrm{M}$) [7]–[9], and polar modulator/envelope elimination and restoration (EER) [11]–[16] enables the linear amplification with the switching amplifier by modulating the input signals or power supply.

The LINC system generates two constant envelope signals by adding the error signals, then amplifies and combines two signals. Since the error signal is dissipated as heat in the combining process, the efficiency of the system is not high.

Manuscript received April 26, 2007; revised July 28, 2007. This work was supported in part by the Korean Ministry of Education under the BK21 Project and by the Center for Broadband Orthogonal Frequency Division Multiplex Mobile Access, Pohang University of Science and Technology, under the Information Technology Research Center Program of the Korean Ministry of Information Technology, supervised by the Institute for Information Technology Advancement (IITA-2006-C1090-0603-0037).

J. Choi, D. Kang, D. Kim, and B. Kim are with the Department of Electrical Engineering, Pohang University of Science and Technology, Pohang, Gyungbuk 790-784, Korea (e-mail: jinsungc@ieee.org; daehkang@postech.edu; rookieds@postech.edu; bmkim@postech.edu).

J. Yim is with the RF Team, System Large Scale Integration Division, Semiconductor Business, Samsung Electronics Company Ltd., Yongin, Gyeonggi 431-836, Korea (e-mail: im1004@postech.edu).

J. Yang is with the Access Network Development Team, SK Telecom, Seoul 100-999, Korea (e-mail: jinhoy@sktelecom.com).

J. Kim is with the Department of Information Technology Engineering, Handong Global University, Pohang, Gyeongbuk 791-708, Korea (e-mail: iamaramis@empal.com).

J. Cha is with the XRONet Corporation, Seongnam, Gyeonggi 463-020, Korea (e-mail: jhcha@xronet.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2007.907137

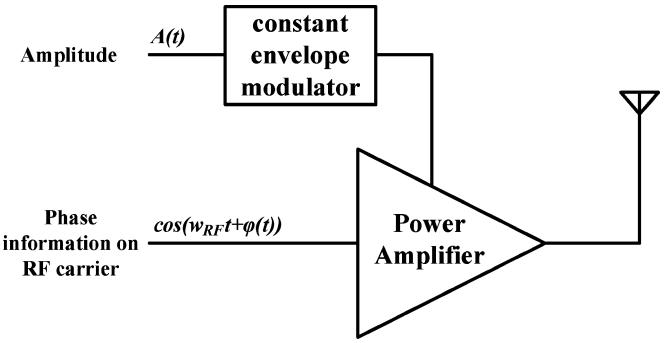



Fig. 2. Operation principle of constant envelope supply-modulated PA.

The RF transmitter employing a BP$\Delta\Sigma$M, seemingly the closest solution for the digital radio, converts a modulated signal into a pulse train in the time domain by adding noise in out-of-band, while preserving the signal. The pulse train can be amplified using a highly efficient switching mode PA. However, the added noise degrades the transmitter efficiency. The BP$\Delta\Sigma$M requires unrealistically high sampling frequency, usually four times the RF carrier frequency. Such a high-speed digital circuit consumes significant power so that the efficiency of the system gets worse.

The polar modulator/EER system ideally delivers 100% efficiency even for the high PAPR signals. The switching PA is modulated by the envelope signal through power supply so the high efficiency is maintained with assumption of a 100% amplitude modulator [17], [18]. However, the nonlinear characteristic of the switching amplifier induces some distortion at the output, mainly due to the $V_{\rm DS}$/PM. It is so serious a problem in designing the polar modulator/EER system that the pre-distortion technique is required to minimize the distortion effects. Recently, there are some good results to solve the problem [11]–[16], but they require complex circuitries for implementation.

The constant envelope modulator solves the problem by converting the time-varying envelope signal into a just 1-bit information assisted by added noise [19], [20]. Instead of continuously modulating the power supply, it turns the amplifier on and off. The discrete switching action linearly combines the phase signal with the constant envelope modulated signal. The concept of the constant envelope supply-modulated PA is described in Fig. 2. The number of quantization levels can be increased to reduce the quantization noise using the multibit quantizer. In this case, the nonlinearity from the multilevel $V_{\rm DS}$ can be easily corrected for its discrete characteristic. In this architecture, any modulated signal is converted to a pulse train and the signal can control a highly efficient switch amplifier in the RF domain. Therefore, the transmitter is easily reconfigured in the digital domain for SDR application.

In this paper, we have designed and demonstrated the transmitter employing the constant envelope modulator. Although the basic idea has been discussed in [21], this study presents a more detailed description and further experimental results. After reviewing various constant envelope modulators and their characteristics with a CDMA IS-95A signal in Section II, Section III discusses the design of the overall transmitter from the digital baseband processors to the switching mode RF PAs. It presents the optimum design of the PA with switching action. Section IV shows the experimental results of the designed transmitter for the CDMA IS-95A signal. In Section V, we extend our research to the multibit operation for better performances. No digital predistortion technique is applied for this system to purely demonstrate the effect of the constant envelope modulation.

## II. Various Constant Envelope Modulators

In the proposed transmitter architecture, the PA roles as the signal multiplier in the time domain. The multiplication in the time domain is mathematically the convolution in the frequency domain. Therefore, the constant envelope modulators, which can provide the previously mentioned advantages, produce the convolution output spectrum at the amplifier output. It means the quantization noise in the modulator's output influences to the output spectrum of the PA. It should be carefully decided which one is the optimum for the transmitter applications among the various constant envelope modulators.

### A. Design Considerations of Constant Envelope Modulators

The square-shape pulse of the modulator's output signal contains the quantization noise and the PA amplifies not only the signal, but also the quantization noise. For exact estimation of the efficiency, the portion of the quantization noise should be subtracted from the PA's efficiency. The efficiency of the 1-bit modulator $\eta_{\rm overall}$ is defined as

$$\eta_{\rm overall}[\%] = \eta_{\rm mod} \times \eta_{\rm PA} \tag{1}$$

$$\eta_{\rm mod}[\%] \cong \frac{\rm PQPR}{\rm PAPR} \times 100 \tag{2}$$

where $\eta_{\rm PA}$ is the efficiency of the PA. $\eta_{\rm mod}$ represents the input signal portion contained in the output pulse of the constant envelope modulator. The peak-to-quantization power ratio (PQPR) and PAPR are defined as

$$\rm PQPR = \frac{\text{permissible peak input signal power}}{\text{output quantization level power}} \tag{3}$$

$$\rm PAPR = \frac{\text{peak input signal power}}{\text{average input signal power.}} \tag{4}$$

The permissible signal peak power is restricted by the stability of the modulator. Usually, for the modulator employing the low-order loop filter, the permissible signal peak power is the same to the quantization level power. As the order of the loop filter increases, however, the permissible signal peak power decreases. The quantization level power is determined by the quantization level, as the word says. For the envelope signal, which is always positive, the quantization level can be set to 1 and 0 for the two-level quantization. The criteria level can be optimized to minimize the amount of the quantization noise. The $\pm 1$ quantization can be used for ease of combining the envelope and phase signals, which enables just flipping the up-converted phase signal. However, the signal efficiency is lower than the 1/0 quantization since the negative quantization value generates more quantization noise than the 1/0 quantization. The quantization noise can be reduced by the multibit quantization, resulting in the efficiency enhancement over the predicted value

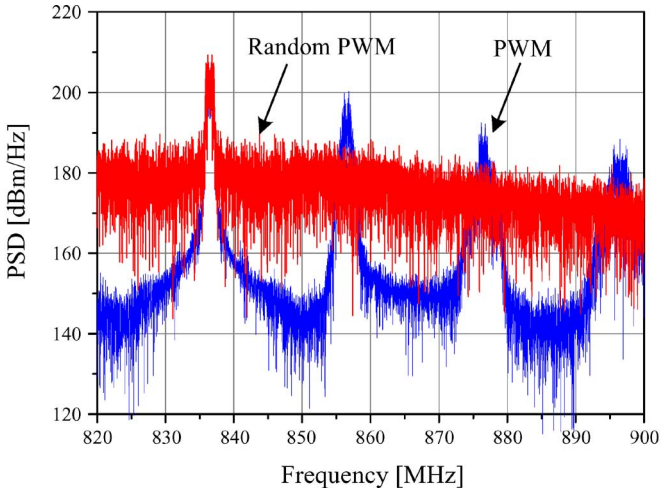



Fig. 3. Spectra of the envelope PWM and RPWM for CDMA IS-95A signal.

from (1)–(4). In the case, the PQPR term increases as the output quantization level power decreases.

The constant envelope modulator is inherently nonlinear due to the existence of the quantizer. It adds the quantization noise to the input signal to make the square shape. The quantization noise influencing the efficiency of the modulator is also related to the spectral linearity. As the quantization noise reduces, the spectral linearity of the output signal gets better. With multibit quantization, the higher oversampling of the signal allows the reduced quantization noise. A more specific mechanism determining the linearity depends on the transfer function of the modulators.

### *B. Various Constant Envelope Modulators*

There are many types of modulators, which convert the time-varying envelope signal into the constant envelope signal. Here, pulsewidth modulation (PWM), random pulsewidth modulation (RPWM), $\Delta$ modulation, and $\Delta\Sigma$ modulation are reviewed in the aspect of the modulation efficiency and linearity.

*1) Pulsewidth Modulator:* PWM uses a square wave whose duty cycle is modulated according to the variation of the waveform's average value. The absence of a feedback loop enables a high-speed operation of the modulator. Moreover, the amount of quantization noise is not large so that the signal efficiency of the modulator is high. For the CDMA IS-95A signal, the signal efficiency is 75%. However, the PWM waveforms are composed of a component at the desired fundamental frequency and a number of undesired harmonics centered at each integer multiple of the switching frequency, as shown in Fig. 3. Thus, the strict post filtering is required to alleviate the harmonics.

*2) Random Pulsewidth Modulator:* RPWM has evolved to solve the harmonic problem of the PWM. Instead of a sawtooth or a triangle waveform based on a fixed switching frequency, it employs the random number generator and voltage-controlled oscillator. The control voltage of the oscillator varies randomly so that there is no specific switching frequency. It has an effect to remove the discrete harmonics, but the continuous noise level increases. Thus, it has higher quantization noise than the PWM so the signal efficiency gets lower to 62%. The spectra of RPWM compared with PWM is presented in Fig. 3. The noise level is too high to be useful for the transmitter.

*3) $\Delta$ and $\Delta\Sigma$ Modulator:* The $\Delta$ modulator is a kind of predictive encoder, whose output is based on the difference between a sample of the input and a predicted value of that sample. The advantage of this structure is that larger input signals are allowed because the difference is smaller than the input signal itself for the oversampled signal. However, the order of the loop filter in the feedback path is limited for the stability issue so that the high-order circuitry for an accurate prediction is difficult to design. The $\Delta\Sigma$ modulator shown in Fig. 4 employs oversampling and noise-shaping techniques to lower the quantization noise [22], [23]. The oversampling occurs whenever a signal is sampled at a frequency larger than twice its bandwidth. It widens the spectrum unnecessarily. Regardless of increased sample rate, however, the quantization noise power remains unchanged. Thus, the oversampling makes the noise power density go down as the spectrum widens. The benefit obtained from the oversampling is supplemented by a filtering operation that shifts part of the noise to a high frequency, leaving less in the baseband. The simple equivalent model described in Fig. 4 shows that the signal and quantization noise have different transfer functions; low-pass filter for the signal and high-pass filter for the quantization noise as

$$y = H \cdot (x - y) + e_{\text{rms}} \tag{5}$$

$$y = H_x \cdot x + H_n \cdot e_{\text{rms}} \tag{6}$$

where

$$H_x = \frac{H}{1+H} \tag{7}$$

$$H_n = \frac{1}{1+H}. \tag{8}$$

Thus, the oversampling effect can be expressed as follows:

$$e_0^2 = \int_0^{f_0} S\left(e_{\text{rms}}^2\right) df = e_{\text{rms}}^2 \frac{2f_0}{f_s} = \frac{e_{\text{rms}}^2}{\text{OSR}} \tag{9}$$

and the noise within the signal boundary is given by

$$\begin{aligned} e^2 &= \int_0^{f_0} S\left(e_{\text{rms}}^2\right) \cdot |H_n(jf)|^2 \, df \\ &= e_{\text{rms}}^2 \frac{2}{f_s} \int_0^{f_0} |H_n(jf)|^2 \, df \\ &\approx e_{\text{rms}}^2 \frac{\pi^{2n}}{(2n+1)(\text{OSR})^{2n+1}} \end{aligned} \tag{10}$$

where $n$ is the order of the loop filter. The above equations clearly show that the high over-sampling ratio (OSR) and loop filter order reduces the quantization noise at the signal boundary so that high signal-to-noise ratio (SNR) is acquired. Note that the $n$ does not increase $\eta_{\text{mod}}$, but the SNR, as observed from the simulation results with the CDMA IS-95A signal in Fig. 5. For $n = 2$, as the OSR increases from 8 to 100, the amount

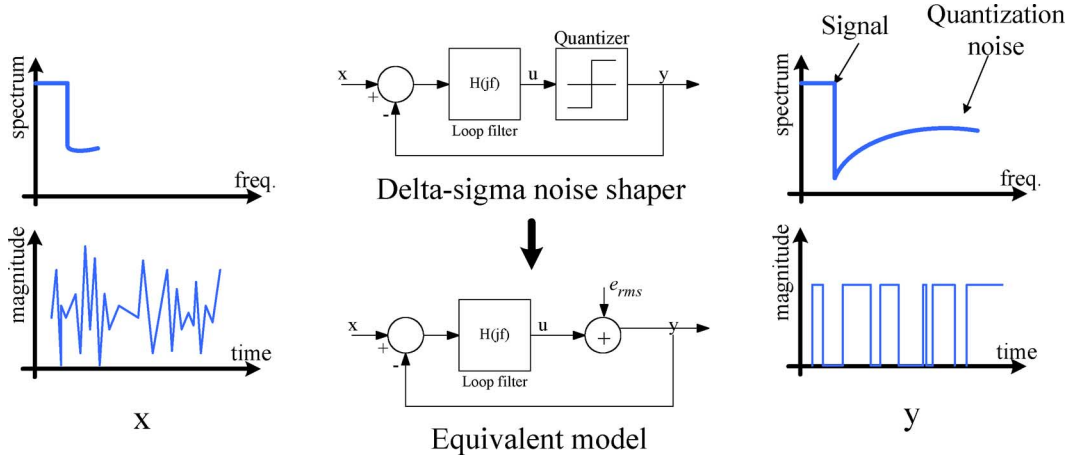



Fig. 4. Operation principle of $\Delta\Sigma$-modulator.

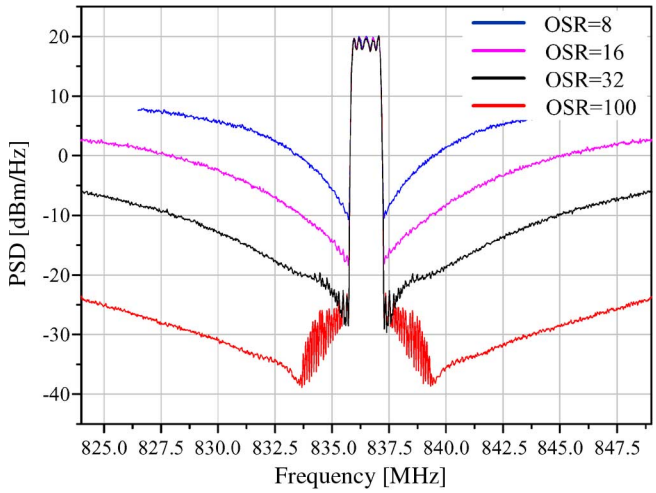



Fig. 5. Simulated output spectra of 1-bit (two-level) second-order $\Delta\Sigma$-digitized transmitter versus OSRs for CDMA IS-95A signal. The noise (closely related to the spectral linearity) reduces as the OSR increases. The ACPR of the signal source is approximately $-61$ dBc at 885-kHz offset.

of quantization noise near the signal boundary effectively decreases. With $\mathrm{OSR} = 100$, the $\Delta\Sigma$ modulator operates at a 250-MHz sample rate, and it satisfies the regulation for the spectrum emission mask over the transmit band of CDMA IS-95A.

The multibit quantization in the $\Delta\Sigma$ modulation also improves the SNR. For the $N$-bit quantizer, the SNR is defined as follows:

$$\mathrm{SNR} = \frac{\frac{2^N\Delta}{2\sqrt{2}}}{\frac{\Delta}{\sqrt{12}}} = 2^N\sqrt{1.5} \tag{11}$$

In the decibel scale,

$$20\cdot\log_{10}(\mathrm{SNR}) = 20[N\cdot\log_{10}(2)+0.5\cdot\log_{10}(1.5)] \tag{12}$$

$$(\mathrm{SNR})_{\mathrm{dB}} = 6N+1.8. \tag{13}$$

This expression links the number of bits to the SNR. The simulation result in Fig. 6(a) demonstrates that the above description is pretty accurate. For 1-bit increment (from two- to four level), there is approximately 6-dB improvement in the noise power spectrum density. In Fig. 6(b), we have shown the noise density at the receive band of the CDMA IS-95A system. One zero at the receive band is included in the loop filter of the $\Delta\Sigma$ modulator to reduce the noise. In this case, the noise is suppressed approximately 7.5 dB/bit. Combining with the filtering effect of the duplexer positioned behind the PA, the 250-MHz fourth-order $\Delta\Sigma$ modulator employing the three-level quantizer satisfies the noise-level requirement at the receive band, as shown in Fig. 7.

Compared to the other constant envelope modulation techniques mentioned above, the $\Delta\Sigma$ modulator provides the most suitable performance due to the accurate noise-shaping characteristic. The signal efficiency of the 1-bit $\Delta\Sigma$ modulator is 60% at an 80-MHz sample rate for the CDMA IS-95A signal.

## III. Design of $\Delta\Sigma$-Digitized RF Transmitter

The $\Delta\Sigma$-digitized transmitter architecture we have studied is shown in Fig. 8. It takes advantages of relatively low OSR and low-speed digital circuitry by the envelope $\Delta\Sigma$ modulation (EDSM) [19], [20]. Even though the sample rate of the $\Delta\Sigma$-digitized envelope signal is higher than the bandwidth of the complex signal, it is still lower than the RF carrier frequency. Compared to the transmitter architecture employing a bandpass $\Delta\Sigma$ modulator (BPDSM) [7]–[9], the sampling frequency decreases from a few gigahertz to dozens of megahertz range. Moreover, the role of the $\Delta\Sigma$ modulator in this case is as a DAC and the main function of the $\Delta\Sigma$ modulation is performed in the digital domain, which can provide efficient and precise signal processing. The $\Delta\Sigma$-digitized envelope signal turns the switching mode PA on and off and is combined with an RF up-converted phase signal through the PA. The phase modulated input power level and dc bias of the PA can be easily controlled by a field-programmable fate array (FPGA) for linear amplification [10].

### A. Digital Baseband Processor

In the $\Delta\Sigma$-digitized transmitter architecture, the majority of the functions can be done digitally, except the frequency up-con-

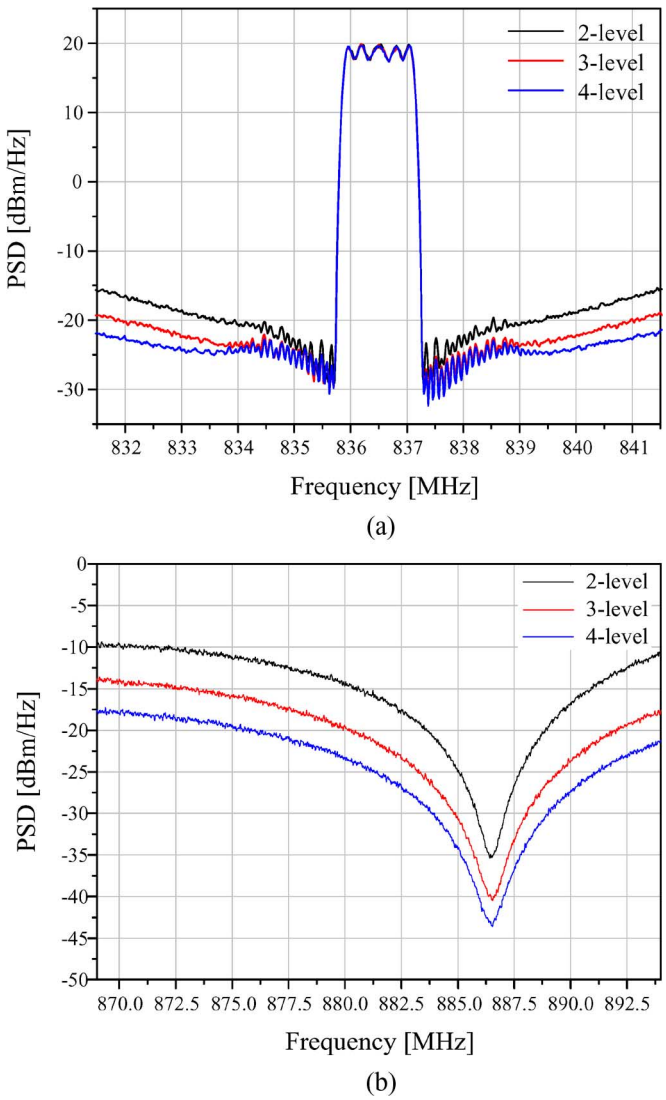



Fig. 6. (a) Simulated transmitter (Tx) band output spectra with $\mathrm{OSR} = 32$ versus quantization levels. (b) Simulated receiver (Rx) band output spectra of $\Delta\Sigma$-digitized transmitter with $\mathrm{OSR} = 100$ versus quantization levels for CDMA IS-95A signal; The noise at Rx band is reduced as the quantization level increases. The order of the loop filter is increased to four by inserting the zero.

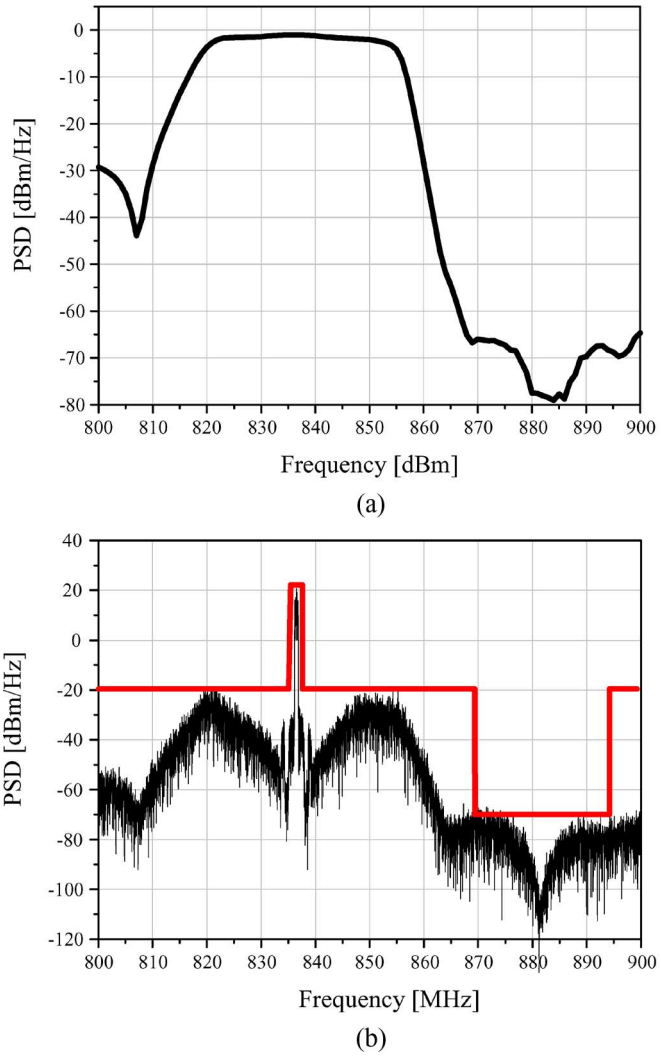



Fig. 7. (a) Measured $S21$ of the duplexer from CTS Wireless, Elkhart, IN. (b) Spectra of 250-MHz fourth-order three-level $\Delta\Sigma$-digitized transmitter simulated with the measured duplexer's $S$-parameters.

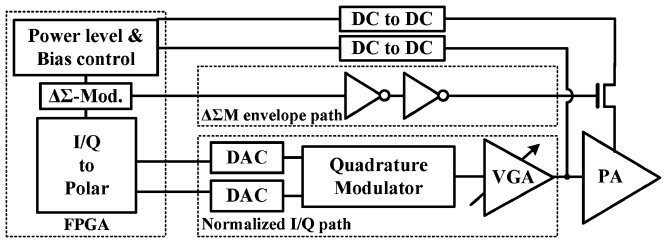



Fig. 8. Proposed transmitter architecture.

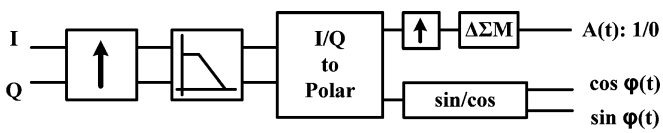



Fig. 9. Digital part of the proposed transmitter implemented in FPGA.

version, amplification, and filtering. The high-performance DSP engine is the elementary unit for this architecture. The DSP engine, shown in Fig. 9, creates two types of signals: the envelope and constant envelope I/Q signals. It consists of the interpolation filter, vector translation, $\sin/\cos$ modulator, and $\Delta\Sigma$ modulator. The purpose of the interpolation filter is to take advantage of the increased clock frequency, and to suppress all unnecessary replicas of the signal spectrum occurring between the baseband and $\mathrm{OSR} \cdot f_s$. The cascade of the root-raised cosine (RRC) and comb filter are used as the interpolation filter to up-sample the baseband in-phase/quadrature (I/Q) signal. The vector translation from the I/Q to the polar is conducted by a coordinate rotation digital calculation (CORDIC) processor. It generates the envelope and phase signals, of which the latter is in the range of $-\pi$ to $\pi$. The phase signal from the CORDIC is then applied to $\sin/\cos$ block to generate the normalized I/Q signal $\cos\ \varphi(t)$ and $\sin\ \varphi(t)$ for up-conversion, and the envelope signal is up-sampled again and modulated by the digital $\Delta\Sigma$ modulator.

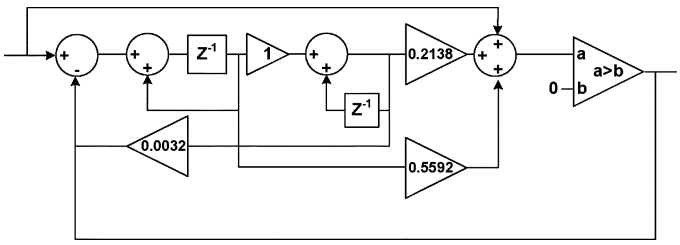



Fig. 10. Single-bit second-order CRFF $\Delta\Sigma$-modulator.

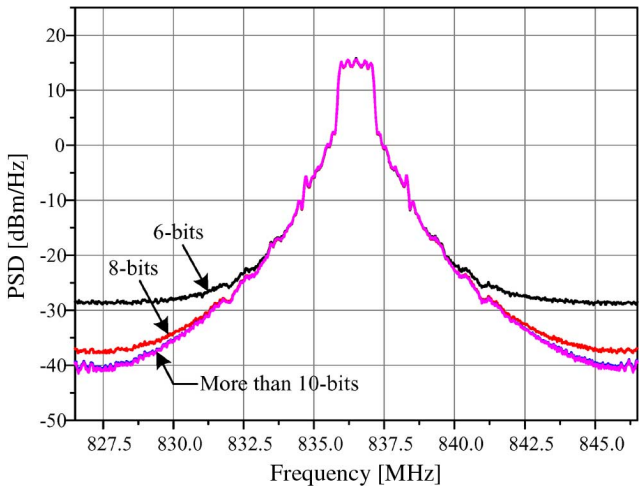



Fig. 11. CDMA IS-95A phase signal with various information bits.

In the noise-shaping loop, all signals are digital, and hence, no internal data conversion is required. For the same reason, the signal processing in the loop is highly accurate, and we do not need to take any analog imperfections into account when predicting the actual behavior of the loop, compared with the conventional switched-capacitor discrete-time $\Delta\Sigma$ modulator (SC$\Delta\Sigma$M) or the continuous time $\Delta\Sigma$ modulator (CT$\Delta\Sigma$M). Moreover, for its simple 1-bit characteristic of the output pulse stream, the simple zero-order sample and hold (ZOH) circuit can replace the high-resolution DAC. Even for the multibit modulator, what is needed are the multiple simple ZOH circuits, which are also very simple structures.

From the simulation, we found that 80-MHz (OSR $= 32$) single-bit second-order cascade-of-resonator with a distributed feed-forward (CRFF) low-pass $\Delta\Sigma$ modulator satisfies the minimum linearity requirements for the CDMA IS-95A signal. The block diagram of the modulator is shown in Fig. 10, whose coefficients are generated using MATLAB [23].

### B. Analog and RF Processors

The analog/RF parts of the transmitter consist of two DACs, pulse amplifier, quadrature modulator, variable gain amplifier, and switching mode PA, as shown in Fig. 8. For the phase path, two DACs operate with a 20-MHz update rate. From the simulation, we have found that more than 10 bits are needed to represent the phase information for CDMA IS-95A. The spectra with various information bits are presented in Fig. 11. The quadrature modulator upconverts the normalized I/Q signals and drives the variable gain amplifier. The input power levels and dc bias of

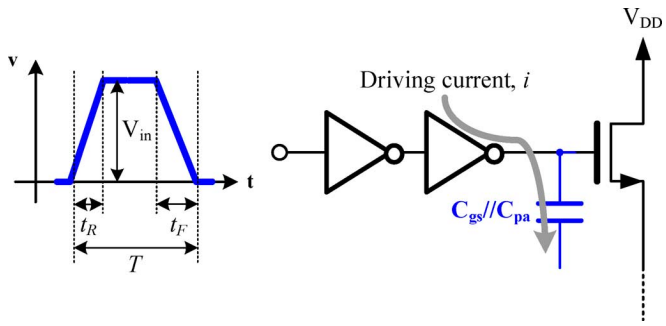



Fig. 12. Pulse driving to switch.

the PA can be controlled by the FPGA through dc-to-dc converters [10]. For the envelope path, the $\Delta\Sigma$-digitized envelope pulse stream is amplified to the level suitable for turning on and off the PA. An inverter can act as the pulse amplifier with an appropriate driving current for a high slew rate switching action, as shown in Fig. 12. From the relation between the voltage and current with the capacitive charging, the slew rate is

$$\mathrm{SR} = \frac{dV_{\mathrm{in}}}{dt} = \frac{i}{C_{\mathrm{gs}}//C_{\mathrm{pa}}} \tag{14}$$

where $C_{\mathrm{gs}}$ is the gate–source capacitance of the switching device and $C_{\mathrm{pa}}$ is the drain–source capacitance of the main amplifier device. When $C_{\mathrm{gs}}//C_{\mathrm{pa}}$ is fixed for certain devices, the available switching speed is determined by the driving current. Similarly, when there is a limitation to the driving current, $C_{\mathrm{gs}}//C_{\mathrm{pa}}$ should be small. However, the on resistance of the switch is inversely proportional to the size of the device, which is proportional to $C_{\mathrm{gs}}$, and there should be a compromise between the switching speed and device size.

The switching mode PA for the $\Delta\Sigma$-digitized transmitter should be turned on and off at a high sample rate. The key design factor is to deliver the pulse signal to the PA, while isolating the amplified RF signal from the bias line. The ratio of the pulse to the carrier frequency is more than 10%, and the usage of the choke inductor on the bias line prevents the pulse signal from being delivered to the drain node. Moreover, the capacitances on the bias line can cause slewing of the pulse signal. The minimum pulsewidth $T$ should be larger than the sum of rising time $t_R$ and falling time $t_F$ of the pulse

$$T > t_R + t_F. \tag{15}$$

If the capacitance is large enough to overrule the above condition, there is a power loss and, hence, the efficiency is degraded. The MOS switch with low on resistance is positioned at the drain to turn on and off the PA. The on resistance causes the voltage drop through the switch device, which results in efficiency degradation.

The class-D PA employs the transformer whose center tap can be used for drain biasing. It basically has a push–pull architecture so the drain bias node forms a virtual ground. It means that the fundamental frequency component does not exist at this point, while the second harmonic is shorted by the small capacitor [18]. The pulse signal is now delivered to the drain without any interferences, and turns the PA on and off. The schematic

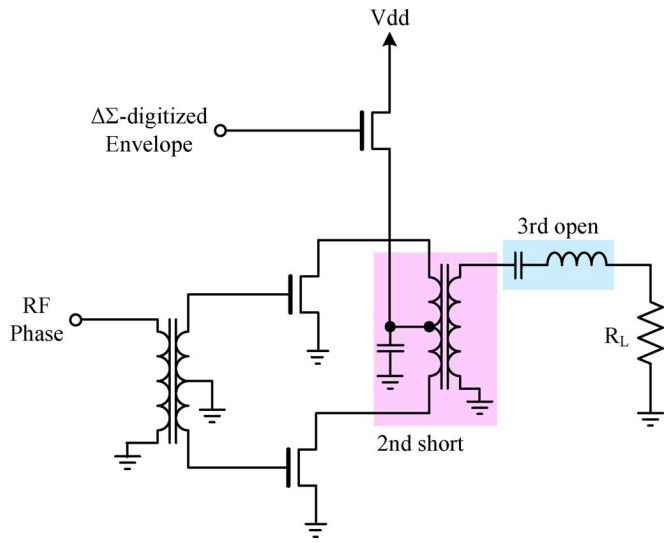



Fig. 13. Class-D PA with control switch.

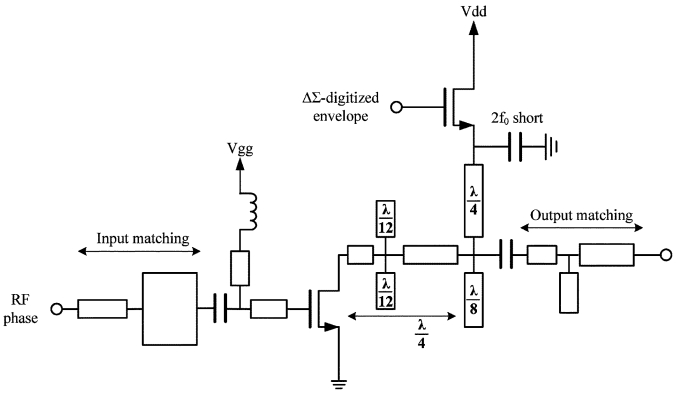



Fig. 14. Class-F PA with control switch.

of the class-D PA with a control switch is shown in Fig. 13. However, the push–pull architecture inherently has three capacitances on the bias line; two device capacitances $C_{\rm ds}$ and second harmonic short capacitance. The high speed switching is difficult to achieve for the limited slew rate by these capacitances, i.e., the increase of $t_R$ and $t_F$. The class-F PA is very similar with the class-D PA, class-B bias, and harmonic tuning network, except that it has just one device for amplification [17]. In fact, the class-F amplifier is not a switching amplifier, but a saturation amplifier. By overdriving the amplifier, it generates harmonics and controls them using the harmonic tuning network. The harmonic tuning network consists of the harmonic trap circuits and the tuning line for compensating the detuning effect of the device parasitic components [24]. The drain bias voltage is supplied through the quarter-wavelength line. Fig. 14 shows the schematic of the class-F PA with the MOS switch. Compared to the class-D PA, it has the reduced device capacitance so that the slewing effect by $C_{\rm ds}$ decreases by one-half. In Section IV, the implementation and measurement results are shown and compared for each amplifier.

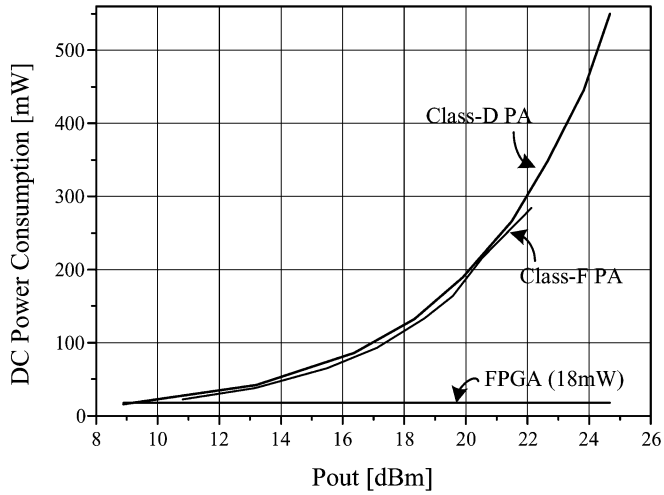



Fig. 15. DC power consumption of the implemented PA and FPGA.

## IV. Implementation and Measurement Results

The overall functions in Fig. 9 are realized with a high-performance FPGA board employing Xilinx Virtex-4. The implemented FPGA, manufactured in 1.2-V 90-nm triple-oxide technology, consumes approximately 18 mW at the 80-MHz sample rate. The power consumption is already low, but can be further reduced by optimizing the circuit. For the lack of a high-speed pMOS device, it is hard to design the inverter for pulse amplification, so we have replaced it with the broadband amplifier using the device GALI 84+ InGaP HBT from Mini-Circuits, Brooklyn, NY, to verify the concept of the proposed architecture. A Sirenza SHF-0289 MESFET is used to implement the PAs. The designed class-D and class-F PAs have 51.7% and 69% continuous wave (CW) PAE at 29 and 27 dBm, respectively. It is valuable to compare the power consumption of the digital baseband processor and PA. The dc power consumption of the FPGA is relatively small compared to that of the PA, as shown in Fig. 15, thus the effect on the overall efficiency is not significant.

The efficiency and output power degrade from the above value due to the on resistance of the switch device on the drain node. Moreover, due to the $\Delta\Sigma$ switching effect, the output power is also degraded. Since the average duty ratio of the $\Delta\Sigma$-digitized CDMA IS-95A envelope signal is approximately 50%, one-half of the full current of the device flows under the switching operation so that the output power is reduced by 3 dB.

Fig. 16 shows the time-domain output signal of the class-D amplifier. Since the response time of the designed class-D amplifier for the pulse is 10 ns, it shows the limitation in following the pulse stream when the width of minimum pulse period is less than 20 ns, according to (15). As a result, it is hard for the PA to exactly respond to the pulse stream as the sample rate increases more than 50 MHz. Compared to the class-D PA, the class-F PA has the reduced device capacitance, which allows the higher sample rate. The rising and falling times decrease to nearly half so that it can follow the pulse stream up to 100 MHz. Fig. 17 shows the time-domain output signal of the class-F PA. The detailed view of the time-domain output signals are presented in

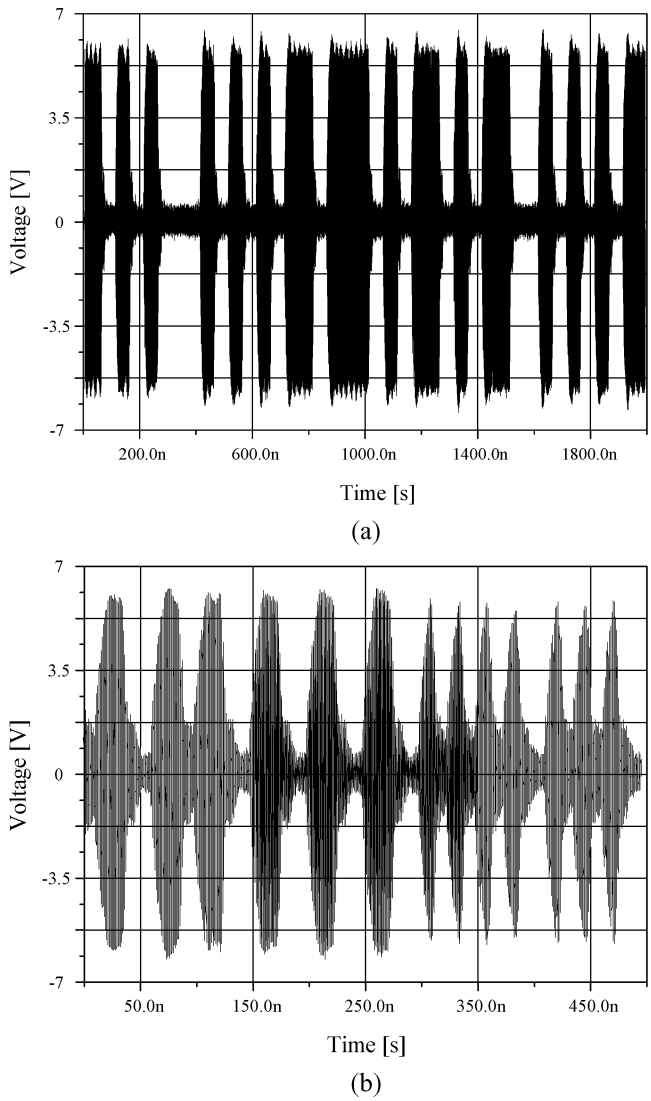



Fig. 16. Time-domain output signal of the class-D PA at: (a) sample rate $=$ $20-$ MHz and (b) sample rate $=$ $80-$ MHz.

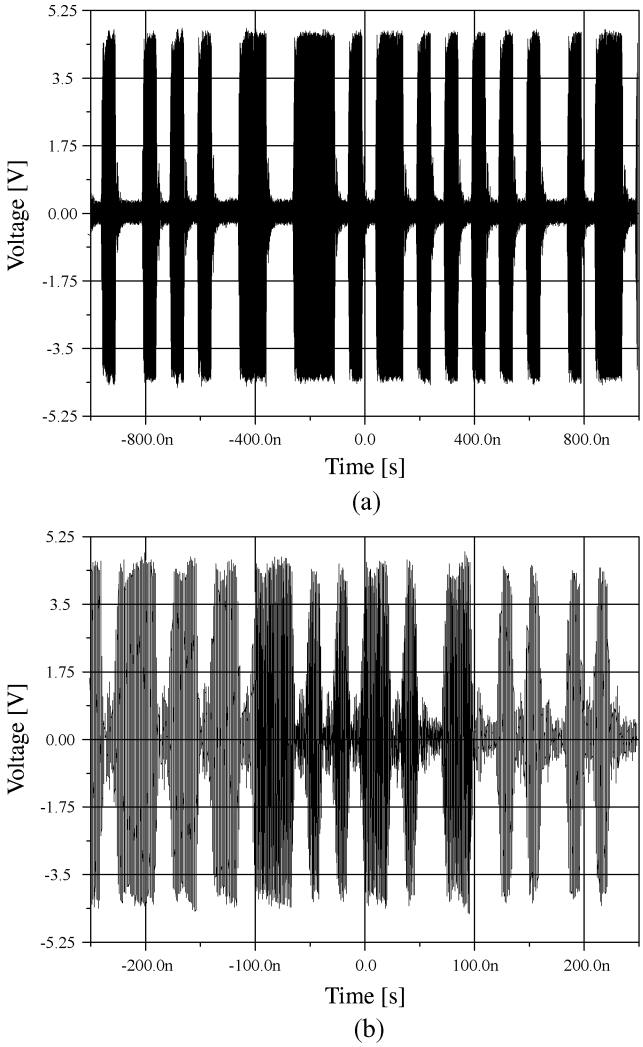



Fig. 17. Time-domain output signal of the class-F PA at: (a) sample rate $=$ $20-$ MHz and (b) sample rate $=$ $80-$ MHz.

Fig. 18. They explain the decrease of the output power and efficiency caused by the imperfect switching (slew effect depending on $C_{\rm ds}$) at the high sample rate. The variation in the pulsewidth is not so significant that the linearity degradation by slewing is not serious.

The maximum efficiency of the $\Delta\Sigma$-digitized transmitter is obtained by optimizing the input power with the proper dc-bias voltage, whose control is conducted by the FPGA. The dc-bias conditions with appropriate input powers for various average output power levels are presented in Tables I and II, and Fig. 19 shows the efficiency versus output power. For the average output power range of 10.8–22.1 dBm, the measured power-added efficiency (PAE) of the class-F PA are 48.6%–51.7%. The $\eta_{\rm overall}$ of the $\Delta\Sigma$-digitized PA calculated using the value obtained in Section II-B is 31%, which can be improved using the better amplifier. Fig. 19 also shows that the class-F PA has a relatively low drop in PAE versus sampling frequency than the class-D PA.

As mentioned above, the 80-MHz $(\mathrm{OSR}=32)$ sample rate satisfies the minimum linearity requirements for the CDMA IS-95A signal. The lower sample rate (lower OSR) of the $\Delta\Sigma$ modulator generates more quantization noise, as presented in (10) and Fig. 5. The measured results in Fig. 20 match quite well with the simulation results. It also verifies that the sample rate of 80 MHz satisfies the specification, while the sample rates of 20 and 40 MHz are not enough. At the maximal average output power, the measured adjacent channel power ratios (ACPRs) are $-46.6$ and $-57.9$ dBc at 885-kHz and 1.98-MHz offsets, respectively. Figs. 21 and 22 show that the $\Delta\Sigma$-digitized transmitter achieves high linearity over the broad range of average output power levels.

The out-of-band noise is the critical issue in this transmitter. For the 80-MHz sample rate, the implemented transmitter requires an additional bandpass filter to reduce the noise in the Rx band. If the sample rate can be increased higher than 250 MHz, with the help of a duplexer positioned behind the PA, the fourth-order $\Delta\Sigma$-modulator enables the transmitter without the additional bandpass filter, as shown in Fig. 7(b). Another possible method is to utilize the sinc filtering mechanism occurred in the discrete to analog conversion process. For 20- and 40-MHz sample rates, the zero of the sinc filter is located at the Rx band

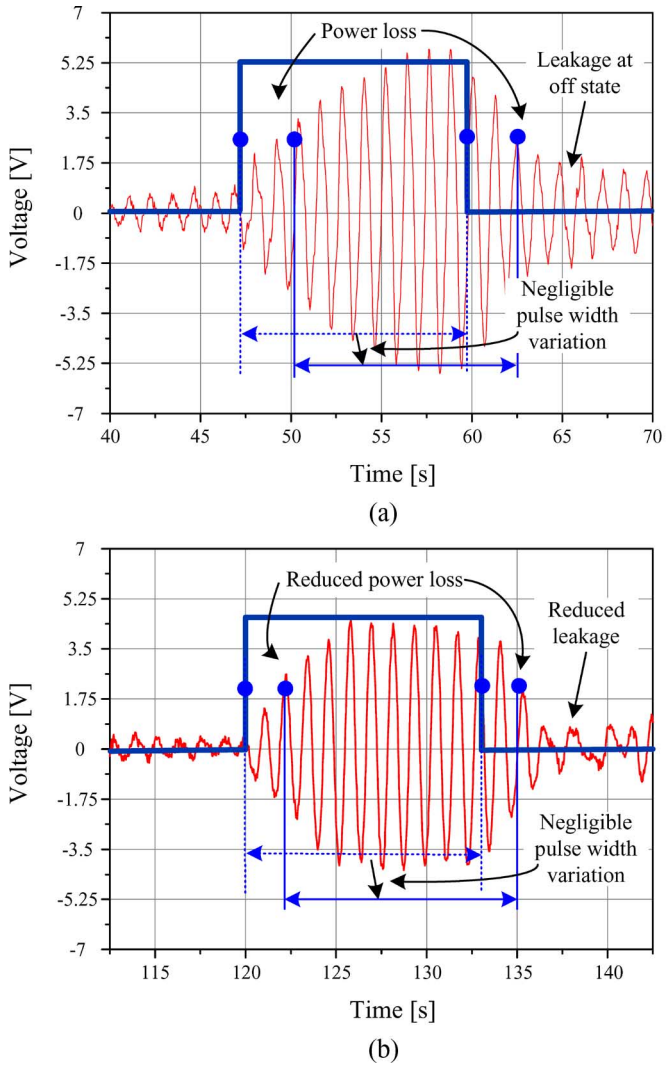



Fig. 18. Measured time-domain output signals of: (a) the class-D amplifier and (b) the class-F amplifier at 80-MHz sample rate: The degradation of the output power and efficiency comes from the limited slew rate of the PA. The pulsewidth does not significantly change.

TABLE I
DC BIAS AND $P$in CONDITIONS OF CLASS-D PA AT OSR = 32

| Drain voltage | Gate voltage | Pin | Pout |
|---|---|---|---|
| 1 V | –1.3 V | 4 dBm | 8.39 dBm |
| 2 V | –1.4 V | 10 dBm | 15.71 dBm |
| 3 V | –1.6 V | 12 dBm | 19.24 dBm |
| 4 V | –1.7 V | 15 dBm | 21.94 dBm |
| 5 V | –1.8 V | 17 dBm | 24 dBm |

so that the out-of-band noise reduces. In that case, however, the noise in the Tx band is not low enough that the multibit approach is required.

## V. MULTIBIT APPROACH

The multibit quantizer reduces the amount of the quantization noise at the overall band. This means the enhancement of the efficiency and linearity. As the number of quantization bits increases, however, it gets harder to control the PA. Moreover,

TABLE II
DC BIAS AND $P$in CONDITIONS OF CLASS-F PA AT OSR = 32

| Drain voltage | Gate voltage | Pin | Pout |
|---|---|---|---|
| 1.5 V | –1.2 V | 1 dBm | 10.82 dBm |
| 2 V | –1.4 V | 3 dBm | 13.17 dBm |
| 3 V | –1.6 V | 7 dBm | 17.11 dBm |
| 4 V | –1.9 V | 9 dBm | 19.57 dBm |
| 5 V | –2 V | 12 dBm | 22.12 dBm |

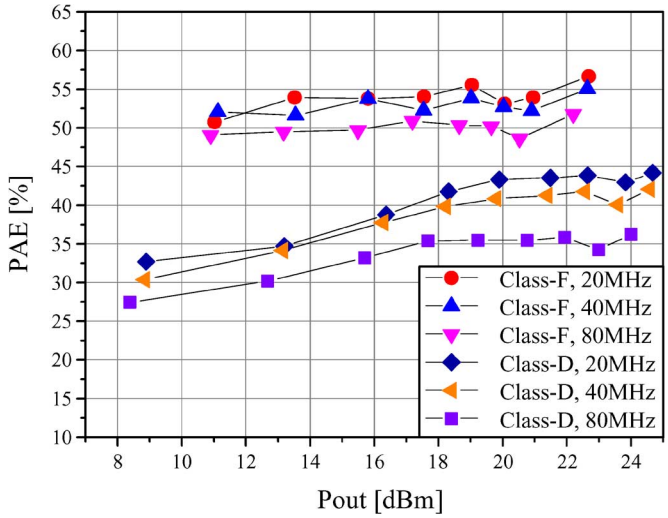



Fig. 19. Measured efficiency of class-D and class-F PAs with the ΔΣ-digitized envelope signal for CDMA IS-95A signal. The sampling frequency varies from 20 to 80 MHz. For the class-D PA, the efficiency suddenly drops as the sampling frequency is higher than 50 MHz. (The efficiency of the dc/dc converter is not considered here.)

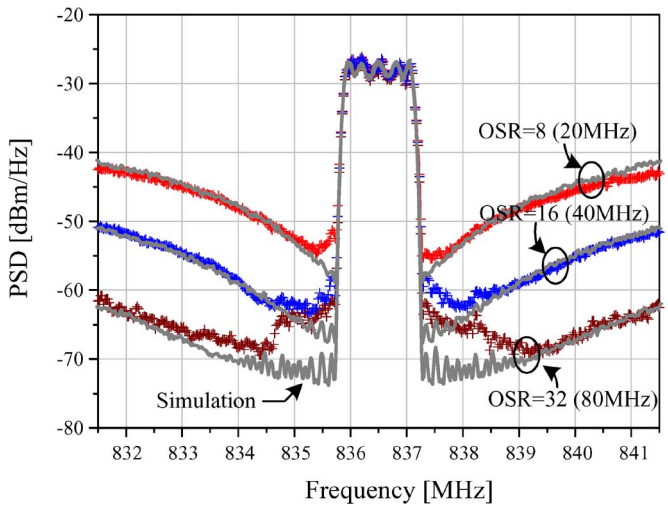



Fig. 20. Measured output spectra of 1-bit ΔΣ-digitized transmitter with various OSRs. They show good match with the simulation results.

to amplify the envelope signal efficiently, 1-bit characteristic is preferred. It can be done by using the cell array of the unit PAs. Each unit PA is turned on and off according to the control signal. This is a conceptually good candidate for the multibit PA, but there is a problem in combining the power signals from the multiple PA cells, which can be solved using the uneven power-combining concept of the Doherty amplifier [25].

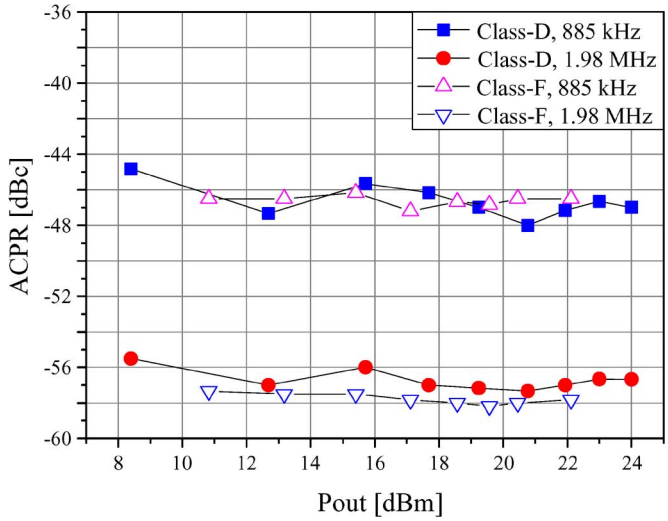



Fig. 21. Measured ACPRs of class-D and class-F PAs with 80-MHz $\Delta\Sigma$-digitized envelope signal for CDMA IS-95A signal.

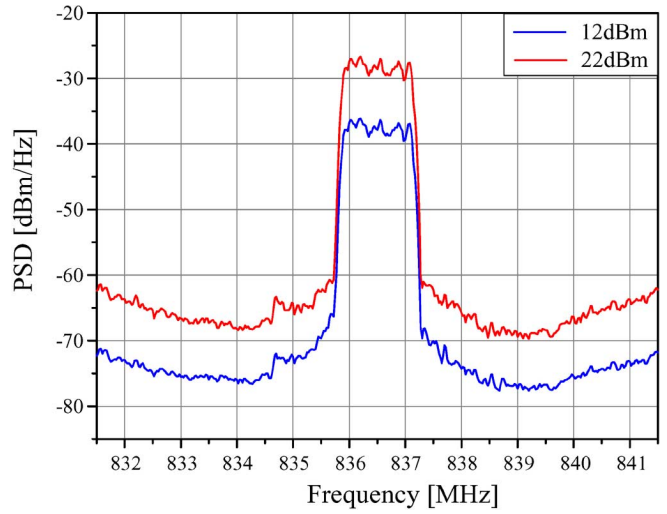



Fig. 22. Power spectrum densities of the output signal at 12 and 22 dBm.

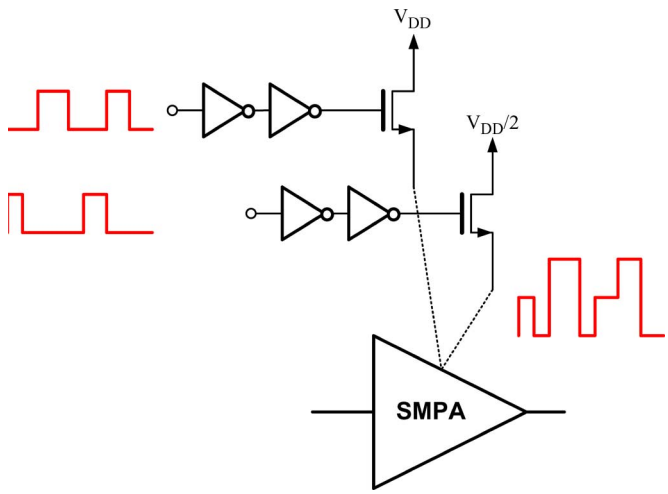



Fig. 23. $\Delta\Sigma$-digitized transmitter employing three-level quantizer.

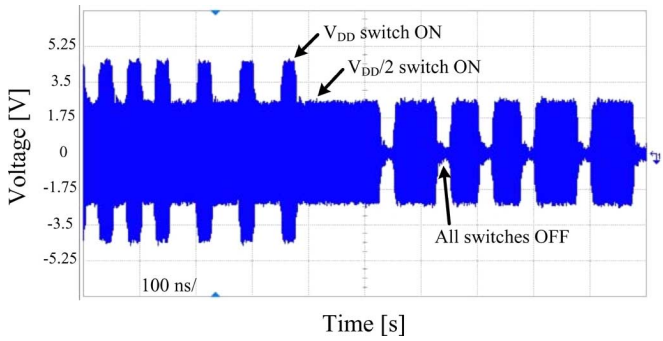



Fig. 24. Time-domain output signal of $\Delta\Sigma$-digitized transmitter employing three-level quantizer.

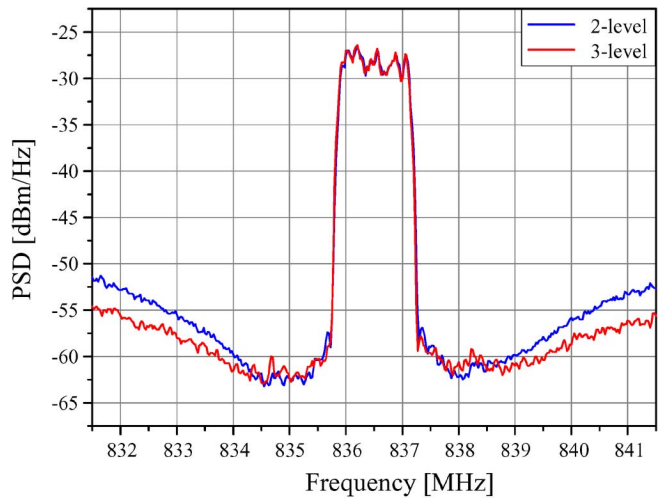



Fig. 25. Output spectra of 40-MHz second-order $\Delta\Sigma$ digitized transmitter employing two-level (1 bit) and three-level quantizers with $\mathrm{OSR} = 16$ (40 MHz).

To remove the power-combining loss, we utilize just one PA while the multibit information is delivered through the multiple power supply array. They consist of switches and multiple voltage sources having different dc voltages. The array of switches are orthogonally turned on, thus there is no power-combining problem in this structure. To verify the concept of the multibit PA, the $\Delta\Sigma$ modulator employing a three-level quantizer is designed. The output signal from the three-level quantizer is encoded to two-way 1-bit signals in the FPGA and delivered to the switch in the same way as described in Section IV. Fig. 23 describes how the three-level digitized PA works. The three-level system is implemented with the 40-MHz sample rate due to the speed limitation of the FPGA. The experimental results in Figs. 24 and 25 show that the output signal of the PA has a three-level digitized envelope with reduced quantization noise. It also reduces the Rx band noise quite well with one zero by sinc filtering, as shown in Fig. 26. The modulation efficiency $\eta_{\mathrm{mod}}$ of the $\Delta\Sigma$ modulator is improved to 89% and the PAE of the PA is 54.6% at 20 dBm of the average output power with the CDMA IS-95A signal. The consequent overall efficiency $\eta_{\mathrm{overall}}$ is 48.6%, which is already very good.

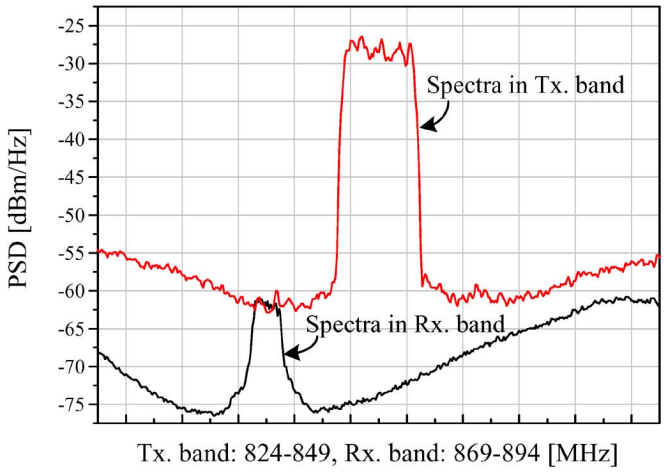



Fig. 26. Measured Tx and Rx band spectra for ΔΣ-modulator employing three-level quantizer. The zero induced by sinc filtering lowers the amount of the quantization noise at Rx band, but the mismatch by the "dirty"clock deteriorates the filtering effect.

## VI. Conclusions

The RF transmitter employing the constant envelope modulator has been designed and implemented. Among the various modulators, the ΔΣ modulator has been chosen for its noise-shaping characteristic. The linearity and efficiency of the transmitter highly depends on the quantization noise, and the appropriate quantization level and OSR have been determined to reduce the quantization noise. The 80-MHz ΔΣ modulator with $1/0$ quantization satisfies the minimum linearity specification of the CDMA IS-95A signal. To realize the circuit, we have heavily utilized the digital environment (FPGA) and combined the modulated envelope signal with the up-converted phase signal through the PA. The class-D and class-F PAs have been fabricated and compared for the optimum operation with the digitized envelope. The measurement results have verified that the most important factor in the digitized operation of the PA is to alleviate the slewing effect by the device capacitances, and the amplifier with small device capacitance is suitable for this application. For the experiment using the CDMA IS-95A signal, the measured overall efficiency is 31% at 22.1-dBm average output power, while the linearity requirements have been satisfied. This transmitter has provided high efficiency and linearity over all usable output power levels. The noise power at the receiver band can be suppressed successfully by introducing zeros in the ΔΣ modulator and with the help of the duplexer. To enhance the performance further, a multibit quantizer has been employed with a new combining method. It eliminates the efficiency degradation from the power-combining loss by using the multiple switch array. The implemented 40-MHz three-level ΔΣ-digitized RF transmitter has presented 48.6% of the overall efficiency at 20-dBm average output power. The performance can be further enhanced by developing the higher multibit digital PA with better efficiency. For the full utilization of the transmitter architecture, we should solve the switching speed limitation of the PA and the out-of-band noise problem in the ΔΣ modulator, hopefully without employing the output filter. However, this architecture can be easily applied to the modulator application as it is.

## Acknowledgment

The authors would like to thank Prof. A. Khandani and S. Chaudhuri, both with the University of Waterloo, Waterloo, ON, Canada, for their great support. The authors also thank to J. Moon, Pohang University of Science and Technology (POSTECH), Pohang, Gyungbuk, Korea, for his help with printed circuit board (PCB) fabrication.

## References

[1] P. M. Asbeck, L. E. Larson, and I. G. Galton, "Synergistic design of DSP and power amplifiers for wireless communication," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 11, pp. 2163–2169, Nov. 2001.

[2] V. W. Leung, L. E. Larson, and P. S. Gudem, "Digital-IF WCDMA handset transmitter IC in 0.25 $\mu$m SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2215–2225, Dec. 2004.

[3] P. Nagle, R. M. Husseini, A. Grebennikov, W. K. M. Ahmed, and F. McGrath, "A novel wideband digital power amplifier and transmitter architecture for multimode handsets," in *IEEE Radio Wireless Conf. Dig.*, Sep. 2004, pp. 171–174.

[4] R. Hitt, W. Littlefield, and A. Gerner, "Digital-RF linearizer for improved broadband multi-carrier power amplifiers," in *IEEE Military Commun. Conf. Dig.*, Oct. 2005, vol. 4, pp. 2602–2609.

[5] L. Larson, P. Asbeck, and D. Kimball, "Digital control of RF power amplifiers for next-generation wireless communications," in *Proc. 35th Eur. Solid-State Device Res. Conf.*, Sep. 2005, pp. 39–44.

[6] R. B. Staszewski, R. Staszewski, J. L. Wallberg, T. Jung, C.-M. Hung, J. Koh, D. Leipold, K. Maggio, and P. T. Balsara, "SoC with an integrated DSP and a 2.4-GHz RF transmitter," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 11, pp. 1253–1265, Nov. 2005.

[7] A. Jayaraman, P. F. Chen, G. Hanington, L. Larson, and P. Asbeck, "Linear high-efficiency microwave power amplifiers using bandpass delta–sigma modulators," *IEEE Microw. Guided Wave Lett.*, vol. 8, no. 3, pp. 121–123, Mar. 1998.

[8] J. Keyzer, J. Hinrichs, A. Metzger, M. Iwamoto, I. Galton, and P. Asbeck, "Digital generation of RF signals for wireless communications with bandpass delta–sigma modulation," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2001, vol. 3, pp. 2127–2130.

[9] P. Asbeck, J. Rode, I. Galton, and L. Larson, "Algorithm and amplifiers for digital generation of microwave signals with time-varying envelope," presented at the IEEE MTT-S Int. Microw. Symp. Workshop, Aug. 2005.

[10] Y. Y. Woo, J. Yi, Y. Yang, and B. Kim, "SDR transmitter based on LINC amplifier with bias control," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2003, vol. 3, pp. 1703–1706.

[11] T. Sowlati, D. Rozenblit, R. Pullela, M. Damgaard, E. McCarthy, D. Koh, D. Ripley, F. Balteanu, and I. Gheorghe, "Quad-band GSM/GPRS/EDGE polar loop transmitter," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2179–2189, Dec. 2004.

[12] G. Norris, R. Alford, J. Gehman, B. Gilsdorf, S. Hoggarth, G. Kurtzman, R. Meador, D. Newman, D. Peckham, R. Sherman, J. Staudinger, G. Sadowniczak, and K. Traylor, "Optimized closed loop polar GSM/GPRS/EDGE transmitter," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2006, vol. 2, pp. 893–896.

[13] F. Wang, D. F. Kimball, J. D. Popp, A. H. Yang, D. Y. Lie, P. M. Asbeck, and L. E. Larson, "An improved power-added efficiency 19-dBm hybrid envelope elimination and restoration power amplifier for 802.11g WLAN applications," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4086–4099, Dec. 2006.

[14] P. Raynaert and S. Steyaert, "A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2598–2608, Dec. 2005.

[15] D. K. Su and W. J. McFarland, "An IC for linearizing RF power amplifiers using envelope elimination and restoration," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2252–2258, Dec. 1998.

[16] J. N. Kitchen, I. Deligoz, S. Kiaei, and B. Bakkaloglu, "Polar SiGe class E and F amplifiers using switch-mode supply modulation," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 5, pp. 845–856, May 2007.

[17] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Norwood, MA: Artech House, 2006.

[18] P. B. Kenington, *High-Linearity RF Amplifier Design*. Norwood, MA: Artech House, 2000.

[19] Y. E. Wang, "An improved Kahn transmitter architecture based on delta–sigma modulation," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2003, vol. 2, pp. 1327–1330.

[20] C. Berland, I. Hibon, J. F. Bercher, M. Villegas, D. Belot, D. Pache, and V. Le Goascoz, "A transmitter architecture for nonconstant envelope modulation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 1, pp. 13–17, Jan. 2006.
[21] J. Choi, J. Yim, Y. Yang, J. Kim, J. Cha, and B. Kim, "A $\Delta\Sigma$-digitized RF transmitter," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2007, vol. 1, pp. 81–84.
[22] P. G. A. Jespers, *Integrated Converters*. Oxford, U.K.: Oxford Univ. Press, 2001.
[23] R. Schreier and G. C. Temes, *Understanding Delta–Sigma Data Converters*. Piscataway, NJ: IEEE Press, 2005.
[24] Y. Y. Woo, Y. Yang, and B. Kim, "Analysis and experiments for high-efficiency class-F and inverse class-F power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 5, pp. 1969–1974, May 2006.
[25] Y. Yang, J. Cha, B. Shin, and B. Kim, "A fully matched $N$-way Doherty amplifier with optimized linearity," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 3, pp. 986–993, Mar. 2003.

**Jinsung Choi** (S'07) received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Gyungbuk, Korea, in 2004, and is currently working toward the Ph.D. degree at POSTECH.

His main interests are CMOS RF circuits for wireless communications, mixed-mode signal-processing integrated-circuit design, and highly efficient and linear RF transmitter architectures.

**Jounghyun Yim** received the B.S. degree in electronics engineering from Yonsei University, Seoul, Korea, in 2000, and the Ph.D. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Gyungbuk, Korea, in 2007.

In 2007, he joined the Samsung Electronics Company Ltd., Yongin, Gyeonggi, Korea, where he is currently a Senior Engineer involved with the design of RF CMOS transceiver for mobile communications. His research interests include RF PA design and CMOS RF circuits for wireless communications.

**Jinho Yang** received the B.S. and M.S. degrees in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Gyungbuk, Korea, in 2005 and 2007, respectively.

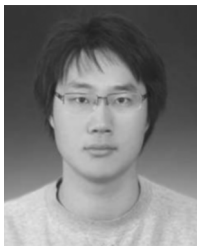
In 2007, he joined the SK Telecom, Seoul, Korea, where he is currently a Manager of the Access Network Development Team. His research interests include the Universal Mobile Telecommunications System (UMTS) access network, optimization of wireless network and next-generation communication system (LTE, HSPA+).

**Jingook Kim** received the B.S. degree in mechanical and control system engineering from Handong Global University, Pohang, Gyungbuk, Korea, in 2003, and is currently working toward the Master degree in information technology engineering at Handong Global University, Pohang, Gyeongbuk, Korea.

His current interests include CMOS RF circuits for wireless communications and sensor network system design.

**Jeonghyun Cha** was born in Gimje, Korea, in 1975. He received the B.S. degree in electronics and information engineering from Chon-buk National University, Chonju, Korea, in 2001, and the Ph.D. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Gyungbuk, Korea, in 2007.

In 2005, he joined the XRONet Corporation, Seongnam, Gyeonggi, Korea. His current research interests include phase-locked loop (PLL) frequency synthesizers, RF transceivers, and PAs for wireless communications.



**Daehyun Kang** received the B.S. degree in electronic and electrical engineering from Kyungpook National University, Daegu, Korea, in 2006, and is currently working toward the Ph.D. degree at the Pohang University of Science and Technology (POSTECH), Pohang, Gyungbuk, Korea.

His research interests include the design of PAs and highly efficient transmitters.

**Dongsu Kim** received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Gyungbuk, Korea, in 2007, and is currently working toward the Ph.D. degree at POSTECH.

His research interests are CMOS RF circuits for wireless communications with a focus on highly efficient and linear RF transmitter design.

**Bumman Kim** (M'78–SM'97–F'07) received the Ph.D. degree in electrical engineering from Carnegie–Mellon University, Pittsburgh, PA, in 1979.

From 1978 to 1981, he was engaged in fiber-optic network component research with GTE Laboratories Inc. In 1981, he joined the Central Research Laboratories, Texas Instruments Incorporated, where he was involved in development of GaAs power field-effect transistors (FETs) and monolithic microwave integrated circuits (MMICs). He has developed a large-signal model of a power FET, dual-gate FETs for gain control, high-power distributed amplifiers, and various millimeter-wave MMICs. In 1989, he joined the Pohang University of Science and Technology (POSTECH), Pohang, Gyungbuk, Korea, where he is a Namko Professor with the Department of Electrical Engineering, and Director of the Microwave Application Research Center, where he is involved in device and circuit technology for RF integrated circuits (RFICs). He was a Visiting Professor of electrical engineering with the California Institute of Technology, Pasadena, in 2001. He has authored over 200 technical papers.

Dr. Kim is a member of the Korean Academy of Science and Technology and the Academy of Engineering of Korea. He was an associate editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and a Distinguished Lecturer of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S).