A Sub-2 dB NF Dual-Band CMOS LNA for CDMA/WCDMA Applications

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***Abstract*—This letter presents the design and experimental results of a 1.8/2.14 GHz dual-band CMOS low-noise amplifier (LNA), which is usable for code division multiple access and wideband code division multiple access applications. To achieve the narrow-band gain and impedance matching at both bands, an extra capacitor in parallel with the C_{gs} of the main transistor and a harmonic tuned load are switched. Except for the output blocking capacitor and series inductor, all components are integrated on a single-chip. The LNA is designed using a 0.13-μm CMOS process and employs a supply voltage of 1.5 V and dissipates a dc power of 7.5 mW. The measured performances are gains of 14.54 dB and 16.6 dB, and noise figures of 1.75 dB and 1.97 dB at the two frequency bands, respectively. The linearity parameters of $\mathrm{P1dB}_{in}$ and IIP3 are -16 dBm and -5.8 dBm at the 1.8 GHz, and -14.8 dBm and -5.3 dBm at the 2.14 GHz, respectively.**

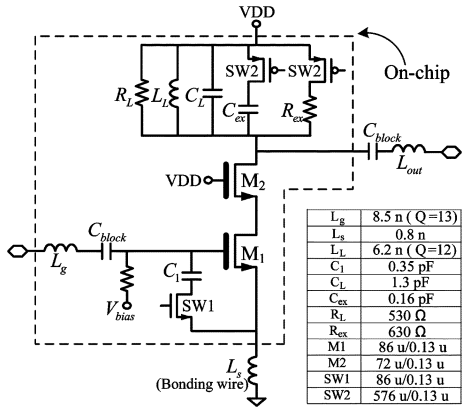
***Index Terms*—Cascode amplifier, CMOS, code division multiple access (CDMA), dual-band, low-noise amplifier (LNA), wideband code division multiple access (WCDMA).**

I. Introduction

CURRENTLY, several wireless standards are in use and new standards are coming into markets continuously. To handle the market demand, a single mobile device should handle the multi-mode/multi-band signals. In the radio frequency (RF) front-end, a low noise amplifier (LNA) plays an important role in the noise of the total system. To meet the trend of market, a multi-band LNA with a good noise performance is a very important component to be developed. Recently, the broadband LNA receiving multiple signals at once is developed [1], but it shows a high noise figure. It is hard to get a noise matching across the wide frequency range. On the other hand, the peaking LNA receiving the selected signal among the various operating frequency slots has a good noise performance by optimizing the performance in each frequency with different matching components.

A dual-band peaking LNA can be achieved by two LNAs in parallel for each narrow band frequency [2], [3]. Even though the LNA provides a good performance at each frequency band, it demands a large chip size, thus a high cost for integration. The LNAs using the switching inductor and concurrent method are also reported [4], [5]. They are compact and consume low power, but require additional inductors. A simple and compact sized LNA is reported in [6], but the series switch degrades the gain and noise figure. Moreover, the buffer used for the output matching increases the power consumption and degrades the linearity.

In this letter, by switching the extra capacitor in parallel with the C_{gs} of the main TR at the input [7] and the harmonic tuned load at the output, a dual-band LNA is realized using the same input/output matching components with a minimum form factor. The 1.8/2.14 GHz dual-band LNA is fabricated in the 0.13-μm CMOS process. Except the output blocking capacitor and series inductor, all components are integrated on a single-chip.



L_g	8.5 n (Q=13)
L_s	0.8 n
L_L	6.2 n (Q=12)
C_1	0.35 pF
C_L	1.3 pF
C_{ex}	0.16 pF
R_L	530 Ω
R_{ex}	630 Ω
M1	86 u/0.13 u
M2	72 u/0.13 u
SW1	86 u/0.13 u
SW2	576 u/0.13 u

Fig. 1. Schematic of the proposed dual-band LNA with switching components.

II. Topology of the Proposed LNA

Fig. 1 shows the proposed LNA. It adopts a cascode structure which has a lot of advantages such as an excellent input/output isolation, high gain, and reduced Miller effect [8]. The switches are made of NMOS and PMOS on the chip, whose performance degradation are minimized by employing the parallel connection. The sizes of the SW1 and SW2 are determined by considering the on-resistance and capacitance of the switches. The LNA uses the same input/output matching components for both frequencies except the switch controlled elements such as C_1, C_{ex}, and R_{ex}.

A. Input Matching and Noise Matching

Fig. 2 shows the S_{11} contours on a smith chart for the two operation bands. It is assumed that the resistance of the matching circuit (R_g) is small. As the SW1 is turned off for the 2.14 GHz, Fig. 2(a), the input impedance of the LNA is given by

$$Z_{in_1} = j\left(\omega_1 L_g + \omega_1 L_s - \frac{1}{\omega_1 C_{gs_{M_1}}}\right) + \frac{g_{m_{M_1}} L_s}{C_{gs_{M_1}}} \quad (1)$$

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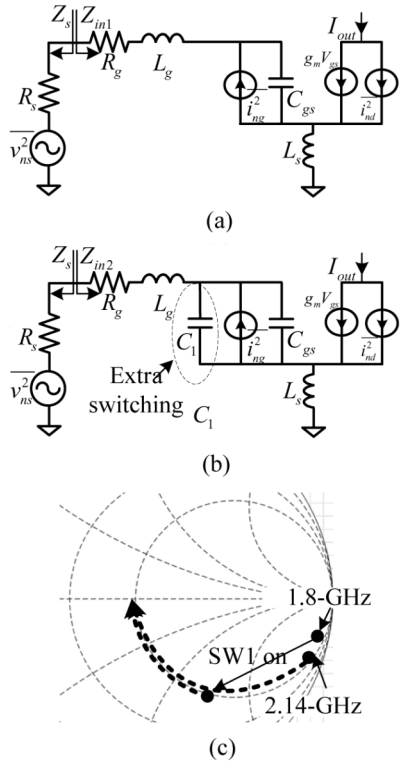

Fig. 2. (a) Small-signal equivalent model of input circuit for 2.14 GHz operation. (b) Small-signal equivalent model of input circuit for 1.8 GHz operation. (c) Input matching in smith chart.

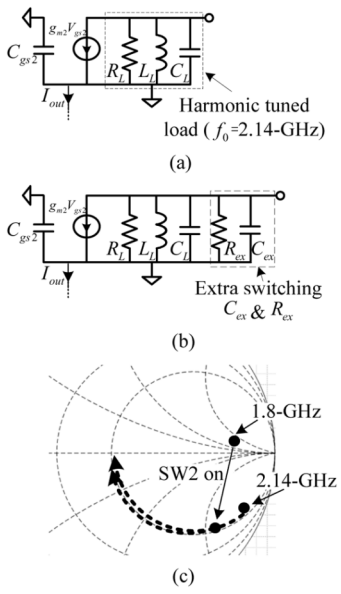

Fig. 3. (a) Small-signal equivalent model of output circuit for 2.14 GHz operation. (b) Small-signal equivalent model of output circuit for 1.8 GHz operation. (c) Output matching in smith chart.

where $g_{m_{M_1}}$, $C_{gs_{M_1}}$, and ω_1 are the transconductance, the gate-source capacitance of M1, and the operating frequency, respectively. For the simultaneous impedance and noise matching, the following condition should be satisfied

$$Z_{opt} = Z_{in}^* = Z_s. \tag{2}$$

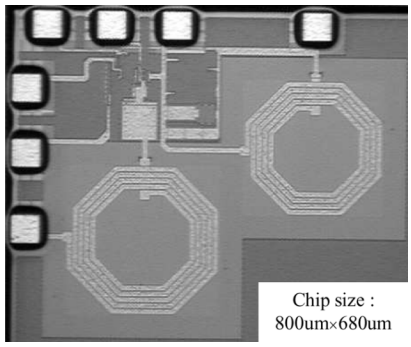

Fig. 4. Die photograph of the proposed LNA.

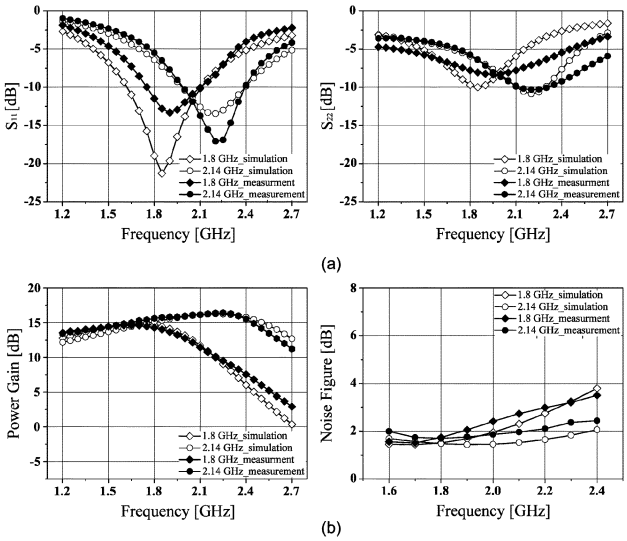

Fig. 5. Simulated and measured (a) S11 and S22. (b) Power gain and noise figure.

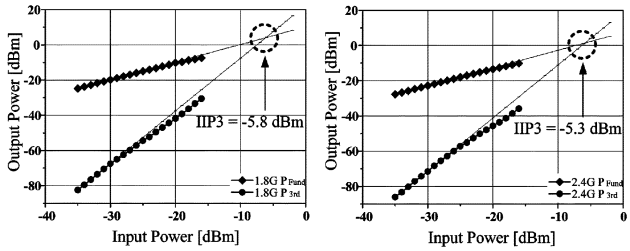

Fig. 6. Measured IIP3 at 1.8 GHz/2.14 GHz.

To satisfy the optimum matching conditions in (2), the L_s, L_g, and W/L should be selected properly with an appropriate bias condition. Especially, the optimum L_s enables the simultaneous impedance and noise matching without any significant degradation of $F_{\min}$ and R_n [9].

For the 1.8 GHz operation, the SW1 is turned on, Fig. 2(b), and the input impedance of LNA is now given by

$$Z_{in_2} = j\omega_2(L_g+L_s) - \frac{j}{\omega_2(C_{gs_{M_1}}+C_1)} + \frac{g_{m_{M_1}}L_s}{C_{gs_{M_1}}+C_1}. \tag{3}$$

As shown in Fig. 2(c), the input impedance at the 1.8 GHz is changed by the SW1. Based on the design parameters optimized

TABLE I
SUMMARY OF THE MEASURED PERFORMANCE AND COMPARISON TO OTHERS

Parameter	This Work		[10]		Single-Band LNA [11]
Process	0.13-μm		0.18-μm		0.35-μm
Supply Voltage	1.5 V		1.8 V		2.5 V
Frequency	1.8 GHz	2.14 GHz	2.4 GHz	5.2 GHz	1.8 GHz
DC Power	7.5 mW	7.5 mW	11.75 mW	5.7 mW	40 mW
S_{11}/S_{22}	–11.52 dB/–8.42 dB	–15.18 dB/–10.97 dB	–10.1 dB/–10.5 dB	–11 dB/–17 dB	NA
Power Gain	14.54 dB	16.6 dB	10.1 dB	10.9 dB	10.5 dB
NF	1.75 dB	1.97 dB	2.9 dB	3.7 dB	4 dB
Input P1dB/IIP3	–16 dBm/–5.8 dBm	–14.8 dBm/–5.3 dBm	–7 dBm/4 dBm	–16 dBm/–5 dBm	–2.4 dBm

for the 2.14 GHz operation, the value of C_1 satisfying (2) at the 1.8 GHz is determined. Then, just by switching the capacitor C_1, the simultaneous noise and input matching at the 1.8 GHz are achieved.

B. Output Matching

For high gains at both frequencies, the proposed LNA has the switched harmonic tuned load. Basically, the resonance frequency of the harmonic tuned load is designed for the 2.14 GHz operation, and the R_L reduces the Q factor of the load to guarantee the channel bandwidth. The output matching circuit transforms the output impedance to 50 Ω. In this state, the SW2 is turned off. For the 1.8 GHz operation, the SW2 is turned on. The additional parallel capacitance C_{ex} and resistance R_{ex} appear now and they change the resonance frequency and the output impedance. It enables the usage of the same components for the output impedance matching at the two bands and provides high gains at both frequencies (see Fig. 3).

III. MEASURMENT RESULTS

The proposed LNA is fabricated using a 0.13-μm CMOS process. A die photograph of the LNA is shown in Fig. 4 whose size is 800 μm$\times$ 680 μm. The LNA is biased at $I_{DS} = 5$ mA with $V_{DS} = 1.5$ V. The measurement results of the LNA are plotted in Figs. 5 and 6. At the 1.8 GHz operation, S_{11} and S_{22} are -11.52 dB and -8.42 dB, respectively. The gain is 14.54 dB and the noise figure is 1.75 dB. The measured P1dB and IIP3 are -16 dBm and -5.8 dBm, respectively. At the 2.14 GHz operation, S_{11} and S_{22} are -15.18 dB and -10.97 dB, respectively. The gain is 16.6 dB and the noise figure is 1.97 dB. The measured P1dB and IIP3 are -14.8 dBm and -5.3 dBm, respectively.

The experimental results show that there is no significant performance degradation by the switching for the operation frequency change. The performance of the proposed LNA is compared to the other LNA's, and summarized in Table I [10], [11].

IV. CONCLUSION

A dual-band LNA for the 1.8 GHz and 2.14 GHz operations with on chip switches is proposed in this letter. By switching the extra capacitor in parallel with the C_{gs} of the main transistor for input matching and the harmonic tuned load for output matching, the LNA achieves the minimal performance degradation by the switching operation. Using a 0.13-μm CMOS process, the designed compact dual-band LNA consumes 7.5 mW. All components are integrated on a single-chip except the blocking capacitor and series inductor. It exhibits a 14.54 dB/16.6 dB gains and a 1.75 dB/1.97 dB noise figures at the 1.8 and 2.14 GHz, respectively.

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