Optimized Design of a Highly Efficient Three-Stage Doherty PA Using Gate Adaptation

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***Abstract*—We demonstrate an optimized design of a highly efficient three-stage Doherty power amplifier (PA) for the 802.16e mobile world interoperability for microwave access (WiMAX) application at 2.655 GHz. The "three-stage" Doherty PA is the most efficient architecture among the various Doherty PAs for achieving a high peak to average power ratio (PAPR) signal. However, it has a problem in that the carrier PA has to maintain a saturated state with constant output power when the other peaking PAs are turned on. We solved the problem using a gate envelope tracking (ET) technique. For the proper load modulation, the gate biases of the peaking PAs were adaptively controlled, and the peak power and maximum efficiency characteristics along the backed-off output power region were successfully achieved. Using Agilent's Advanced Design System and MATLAB simulations, the overall behavior of the three-stage Doherty PA with the ET technique employed was fully analyzed, and the optimum design procedure is suggested. For the WiMAX signal with a 7.8-dB PAPR, the measured drain efficiency of the proposed three-stage Doherty PA is 55.4% at an average output power of 42.54 dBm, which is an 8-dB backed-off output power. Digital predistortion was used to linearize the proposed PA. After linearization, a −33.15 dB relative constellation error performance was achieved, satisfying the system specifications. This is the best performance of any 2.655-GHz WiMAX application ever reported, and it clearly shows that the proposed three-stage Doherty PA is suitable as a highly efficient and linear transmitter.**

***Index Terms*—Efficiency, envelope tracking (ET), GaN, HEMT, linearity, peak to average power ratio (PAPR), power amplifier (PA), RF transmitter, three-stage Doherty PA, world interoperability for microwave access (WiMAX).**

I. Introduction

FOR A modulation signal with a high peak to average power ratio (PAPR), the transmitter has to be operated in a backed-off average output power region to achieve an acceptable linearity and it has a low efficiency due to the backed-off operation. To achieve a high efficiency and high linearity at the same time, an architecture with efficiency enhancement and linearization techniques should be utilized. As a linearization technique, digital predistortion (DPD) is a powerful and reliable solution and is the most favored method for the linearization of base-station power amplifiers (PAs) [1]. As an efficiency enhancement technique, the hybrid envelope elimination and restoration/envelope tracking technique (H-EER/ET) and Doherty technique can be considered [2]–[8]. Theoretically, the H-EER/ET transmitter has an excellent efficiency and linearity along with a high output power capability. However, its performance is limited due to the difficulties in building a bias modulator with a high efficiency and a wide bandwidth. On the other hand, the Doherty technique is not an optimum architecture for the efficient amplification of a high PAPR signal because the nonoptimum efficiency region exists due to the unsaturated operation of the peaking PA [3], [10]. In spite of this imperfection, the Doherty PA delivers the highest efficiency because of the well-developed simple circuit method. Accordingly, the Doherty PA market has experienced a rapid growth in recent years [11]. Among the various Doherty PAs, the three-stage Doherty PA has a superior efficiency characteristic because it has three maximum efficiency points along the output power level. To implement the three-stage Doherty PA, the size ratio between each PA has to be properly chosen. Furthermore, the saturated operation of the carrier PA with a constant output power is essential for the proper load modulation, and the gallium–nitride high electron-mobility transistor (GaN HEMT) device is difficult to use for the implementation because of the Shottky turn-on problem [12]–[14]. Therefore, the three-stage Doherty PA that utilizes a GaN HEMT device has to employ a complex input power management circuit along the power level [13], and most three-stage Doherty PAs have been designed using LDMOSFET devices [14], [16]. Moreover, it is hard to implement the three-stage Doherty PA, which can simultaneously provide a uniform gain and a proper uneven power combining [13]. Recently, a new three-stage Doherty architecture with no saturated operation of carrier PA has been reported by the NXP Corporation, Nijmegen, The Netherlands [16]. This architecture utilizes a different output combining circuit while delivering the three maximum efficiency points compared to the previously reported three-stage Doherty PA. Since the output power of the carrier PA is increased along with the input power with no hard saturated operation of the carrier PA, the new three-stage Doherty PA can be designed using the GaN HEMT power device. A flat gain response can also be achieved due to the load modulation characteristic of the carrier PA. However, it still has poor load modulation because of the low gate biases of the peaking PAs.

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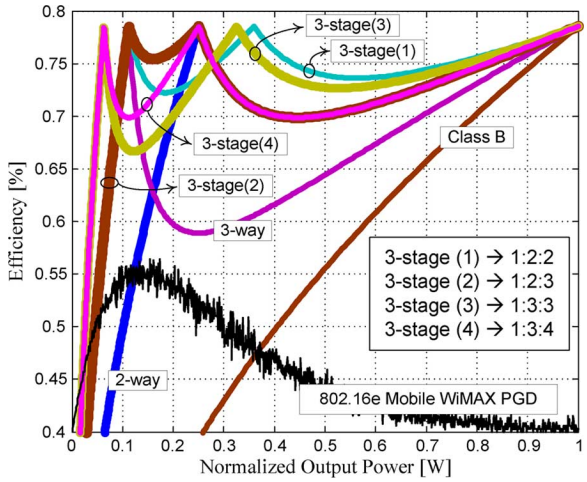


Fig. 1. Efficiency characteristics of various Doherty PAs versus the normalized output power.

For efficient operation at the backed-off output power region while maintaining peak power, we employed the envelope tracking (ET) technique to adaptively control the gate biases of the peaking PAs [14], which was demonstrated at the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium (IMS) [15]. In this paper, we will analyze the detailed operation principles of the new three-stage Doherty PA and suggest the optimum design method for the 802.16e mobile WiMAX application with the gate-bias adaptation technique including the linearization of the PA.

II. Comparison of N-Way Versus Previous Three-Stage Doherty PA

In Fig. 1, the efficiency curves versus the normalized output power of four types of three-stage Doherty PAs and two types of N-way Doherty PAs are illustrated. As reported in many papers [3], [17], the "N-way" Doherty PA has two maximum efficiency points at the backed-off output power and peak power levels, respectively. The backed-off level with the first maximum efficiency, $20 \cdot \log(1/N)$ [dB], is determined by selecting the size of the peaking PA. On the other hand, the three-stage Doherty PA has three maximum efficiency points along the output power level [12]. The back-off levels with the two maximum efficiencies are determined by the size ratio of the two peaking PAs compared to the carrier PA, which is derived in the reference paper [13]. k_1 and k_2 are the input power back-off points on the normalized input voltage magnitude. To evaluate the average efficiency of each Doherty PA, a 802.16e mobile WiMAX signal with a 8.5-dB PAPR was used. The average drain efficiency $(\mathrm{DE_{Avg}})$ can be calculated as follows [18]:

$$\mathrm{DE_{Avg}} = \frac{\int \mathrm{prob.}(V_{\mathrm{in}}) \cdot P_{\mathrm{out}}(V_{\mathrm{in}}) dV_{\mathrm{in}}}{\int \mathrm{prob.}(V_{\mathrm{in}}) \cdot P_{\mathrm{dc}}(V_{\mathrm{in}}) dV_{\mathrm{in}}}. \quad (1)$$

$\mathrm{prob.}(V_{\mathrm{in}})$ is the probability of occurrences of V_{in} for the modulated input signal. In this equation, the overall DE is determined by the ratio of the product of the probability distribution and the power generation terms $(P\mathrm{out})$ over that of the distribution and the dc power $(P\mathrm{dc})$. The numerator of the above function (probability × power) is called the power generation distribution (PGD) of the Doherty PA [6]. The distribution indicates the important power generation region of the Doherty operation, and the operation at that region determines the average efficiency. In Fig. 1, the PGD is also depicted, and the three-stage Doherty PA broadly maintains the high-efficiency characteristic at the important power generation region, whereas the N-way Doherty PAs do not. In Table I, the calculated back-off levels for the peak efficiency points and average efficiencies of each Doherty PA for the WiMAX signal are presented. The three-stage Doherty PA has an improved efficiency of about 10% compared to the N-way Doherty PA, showing that the three-stage Doherty PA is the most efficient architecture for amplification of a signal with a high PAPR. Fig. 2 shows the fundamental current profiles and the output combining circuit topology of the previously reported three-stage Doherty PA with a 1:2:2 size ratio between

TABLE I
Back-Off Level for Peak Efficiency Point and Average Efficiency of the "N-Way" and Three-Stage Doherty PA for the 802.16e Mobile WiMAX Signal With 8.5-dB PAPR

■ $N-way$	$Back-off$	DE_{Avg}
$2-way$	-6 dB	59 %
$3-way$	-9.5 dB	61.2 %
■ $3-stage$ $Cell\ Size\ Ratio$ $(Car.:Peak.1:Peak.2)$	$Back-off$	DE_{Avg}
1 : 2 : 2	-4.44/-9.5 dB	69.8 %
1 : 2 : 3	-6/-9.5 dB	69.4 %
1 : 3 : 3	-4.87/-12 dB	70.5 %
1 : 3 : 4	-6/-12 dB	71 %

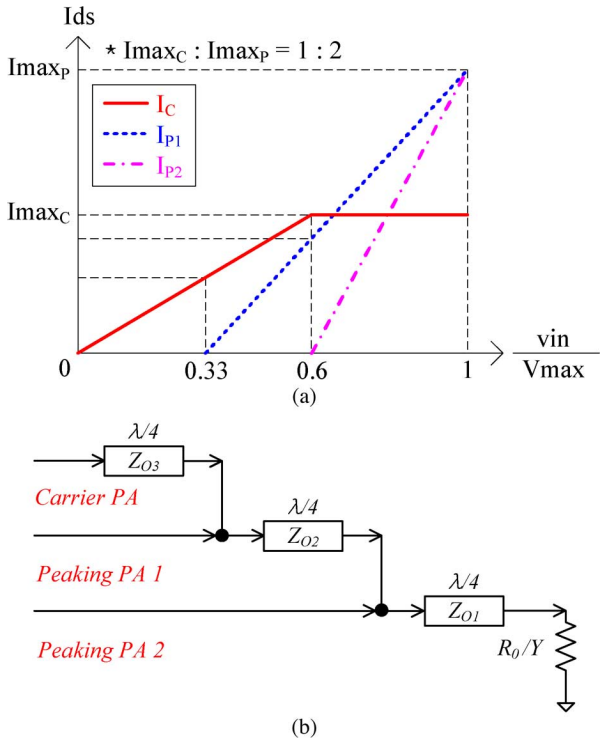


Fig. 2. Previous "1:2:2" three-stage Doherty PA. (a) Fundamental currents of each PA. (b) Output combining circuit.

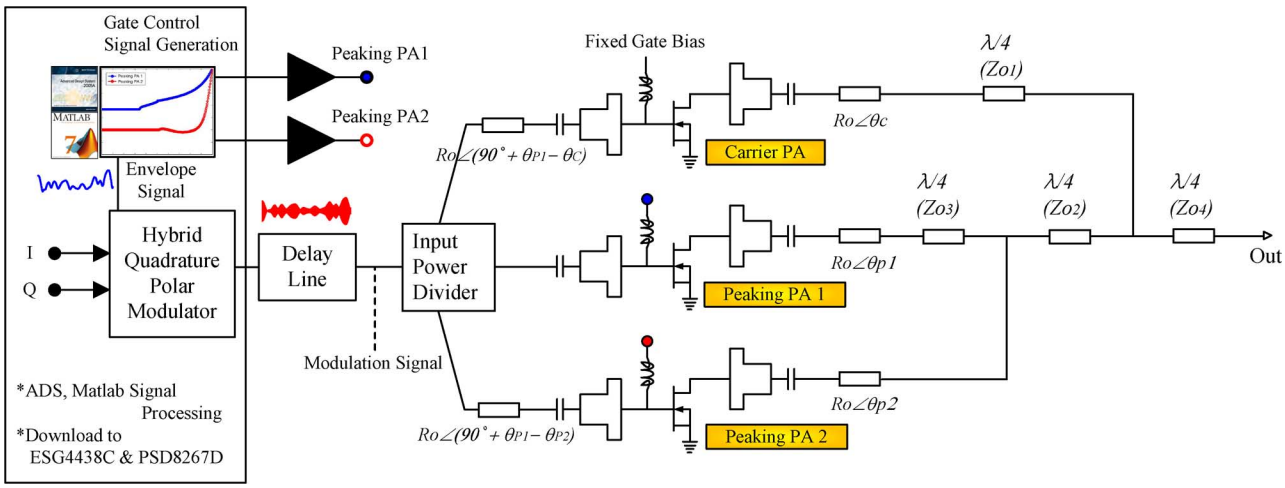


Fig. 3. Architecture of the proposed ET three-stage Doherty PA.

each PA [12], [13]. The topology is a parallel combination of one Doherty PA as a carrier PA with one additional peaking PA, and it is hard to implement the three-stage Doherty PA, which can provide a uniform gain and proper uneven power combining simultaneously. To maintain the flat gain profile versus the output power level, the high gain of the carrier PA due to the load modulation has to compensate for the input dividing loss. (In the case of the three-stage Doherty PA with a 1:2:2 size ratio, the load impedance of the carrier PA has to be modulated from $5 \cdot R_O$ to R_O to compensate the input dividing loss.) However, the three-stage Doherty PA cannot provide the proper load modulation for the carrier PA [13]. Accordingly, the gain at the low output power region where only the carrier PA is operating is lower than that of the Doherty PA at the peak output power. Moreover, as shown in Fig. 2(a), the carrier PA has to maintain the saturated state with the constant output power along $0.6 \sim 1$ of the normalized input power level for the proper load modulation. This operation can cause the Shottky turn-on problem for the GaN HEMT device. Since the GaN HEMT power device is the favored device due to its high efficiency and power density, this problem is a serious limitation for the previously reported three-stage Doherty PA architecture.

The NXP corporation has reported a new three-stage Doherty PA architecture [16], which is a parallel combination of one carrier PA and one Doherty PA used as a peaking PA. This architecture solves the problem of the saturated operation of the carrier PA. Accordingly, the GaN HEMT device can be used for the new three-stage Doherty PA. In addition, by using the uniform unit PA, a flat gain response becomes achievable because the high gain of the carrier PA is enough to compensate for the input dividing circuit through proper load modulation ($3 \cdot R_O$ to R_O). The load modulation of the new three-stage Doherty PA is analyzed in Section III. The remaining problem for the realization of the Doherty PA is the proper load modulation issue. The peaking PAs of the three-stage Doherty architecture are turned on one after another. Thus, the gate bias of the PA is much lower than that of the N-way Doherty architecture, and the load modulation at the peak power region becomes very poor. In this situation, we can design for two cases. The first case is that of a peak power and flat gain response (linear AM–AM) with a poor efficiency in the backed-off output power region. The other case involves a high efficiency in the backed-off output power level with insufficient peak power and gain flatness. However, neither of the options are optimum designs. To overcome this problem, we can employ the uneven input power drive technique [19], but it reduces the linear gain and is not enough to achieve high efficiency at the backed-off output power level and peak power at the same time. One other method is that a differently modulated signal is applied to each PA while the combined output can recover the original signal [13]. In this case, we need to regenerate the new input signal appropriate for the Doherty operation with three upconverters. The other alternative is a gate-bias adaptation of the peaking PAs [20], [21]. In this paper, we analyzed the operation principle of the optimized design using the gate-bias control of the peaking PA of the new three-stage Doherty PA for the efficiency improvement at the backed-off output power level and peak power at the same time[22]. The architecture of the proposed three-stage Doherty PA is shown in Fig. 3.

III. Analysis of the New Three-Stage Doherty PA

A. Load Modulation Behavior at the Backed-Off Output Power Level

In Fig. 4(a), the fundamental current profiles of the new three-stage Doherty PA are presented. The Doherty PA consists of symmetric unit cells, and all PAs are saturated at the maximum input power at the same time. To find the back-off levels with the maximum efficiency, the maximum output power and backed-off output power of the three-stage Doherty PA are derived as follows [13]:

$$\therefore\ P_{\mathrm{OUT,Max}} = \frac{3}{2} \cdot V_{\mathrm{DC}} \cdot I_{\max} \tag{2}$$

$$\therefore\ P_{\mathrm{OUT},k2} = \frac{1}{2} \cdot V_{\mathrm{DC}} \cdot I_{C,k2} \tag{3}$$

$$\therefore\ P_{\mathrm{OUT},k1} = \frac{1}{2} \cdot V_{\mathrm{DC}} \cdot (I_{C,k1} + I_{P1,k1}) \tag{4}$$

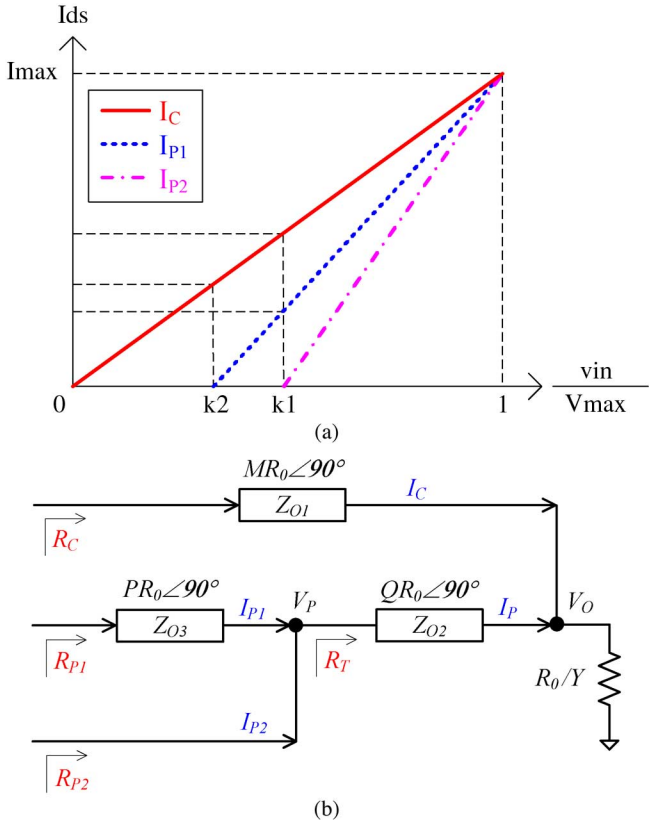


Fig. 4. (a) Fundamental currents of each PA. (b) Output combiner of the new three-stage Doherty PA.

where

$$I_{C,k1} = \frac{2}{3} \cdot k_1 \cdot \frac{P_{\mathrm{OUT,Max}}}{V_{\mathrm{DC}}}$$
$$I_{P1,k1} = \frac{2}{3} \cdot \frac{k_1 - k_2}{1 - k_2} \cdot \frac{P_{\mathrm{OUT,Max}}}{V_{\mathrm{DC}}}$$
$$I_{C,k2} = \frac{2}{3} \cdot k_2 \cdot \frac{P_{\mathrm{OUT,Max}}}{V_{\mathrm{DC}}}.$$

The backed-off output power can be written as

$$\therefore P_{\mathrm{OUT},k1} = k_1^2 \cdot P_{\mathrm{OUT,Max}} \tag{5}$$
$$\therefore P_{\mathrm{OUT},k2} = k_2^2 \cdot P_{\mathrm{OUT,Max}}. \tag{6}$$

Using (3)–(6), k_1 and k_2 are obtained as

$$\therefore k_1 = \frac{1}{3} \quad k_2 = \frac{1}{2} \text{ or } \frac{1}{3}. \tag{7}$$

The three-stage Doherty PA can have two or three maximum efficiency points depending on the biases of the peaking PAs. It is selected that the three-stage Doherty PA has the maximum efficiency at the -9.54- and -6-dB backed-off output power and maximum peak power using the different biases of peaking PAs.

In Fig. 4(b), the output combiner topology of the new three-stage Doherty PA is presented [13]. Using the active load–pull principle [10], the characteristic impedances of quarter-wave transformers in the circuit can be derived. The fundamental drain current ratios between the carrier and peaking PAs are defined as

TABLE II
CALCULATED δ_1 AND δ_2 VERSUS THE INPUT POWER LEVEL

v_{in}/V_{max}	0.33	0.5	1
δ_2	0	0	1
δ_1	0	0.5	2

$$\therefore \delta_2(v_{\mathrm{in}}) = \frac{I_{P2}(v_{\mathrm{in}})}{I_{P1}(v_{\mathrm{in}})} \tag{8}$$
$$\therefore \delta_1(v_{\mathrm{in}}) = \frac{I_{P1}(v_{\mathrm{in}}) + I_{P2}(v_{\mathrm{in}})}{I_C(v_{\mathrm{in}})} = \frac{I_{P1}(v_{\mathrm{in}})}{I_C(v_{\mathrm{in}})} \cdot [1 + \delta_2(v_{\mathrm{in}})]. \tag{9}$$

We assume that R_O is the final output load impedance, and the Y is the impedance transforming ratio of the three-stage Doherty PA. If the characteristic impedances of each quarter-wave transformer, Z_{O1}, Z_{O2}, and Z_{O3} are assigned as $M \cdot R_O$, $Q \cdot R_O$, and $P \cdot R_O$, respectively, the load impedances of each PA are derived as follows:

$$\therefore R_C(v_{\mathrm{in}}) = \frac{M^2 \cdot Y \cdot R_O}{1 + \delta_1(v_{\mathrm{in}})} \tag{10}$$
$$\therefore R_T(v_{\mathrm{in}}) = \frac{\delta_1(v_{\mathrm{in}})}{1 + \delta_1(v_{\mathrm{in}})} \cdot Q^2 \cdot Y \cdot R_0 \tag{11}$$
$$\therefore R_{P1}(v_{\mathrm{in}}) = \frac{[1 + \delta_1(v_{\mathrm{in}})] \cdot P^2 \cdot R_O}{\delta_1(v_{\mathrm{in}}) \cdot [1 + \delta_2(v_{\mathrm{in}})] \cdot Q^2 \cdot Y} \tag{12}$$
$$\therefore R_{P2}(v_{\mathrm{in}}) = \frac{\delta_1(v_{\mathrm{in}}) \cdot [1 + \delta_2(v_{\mathrm{in}})]}{\delta_2(v_{\mathrm{in}}) \cdot [1 + \delta_1(v_{\mathrm{in}})]} \cdot Q^2 \cdot Y \cdot R_O. \tag{13}$$

In Table II, δ_1 and δ_2 are calculated based on the fundamental current profiles shown in Fig. 4(a) using k_1 and k_2 of 0.5 and 0.33, respectively. Thus, the load impedance variations of each PA at the backed-off output power can be determined as follows:

$$\therefore R_C(v_{\mathrm{in}}) = \begin{cases} M^2 \cdot Y \cdot R_O, & v_{\mathrm{in}}/V_{\mathrm{max}} = 0.33 \\ \frac{2}{3} \cdot M^2 \cdot Y \cdot R_O, & v_{\mathrm{in}}/V_{\mathrm{max}} = 0.5 \\ \frac{1}{3} \cdot M^2 \cdot Y \cdot R_O, & v_{\mathrm{in}}/V_{\mathrm{max}} = 1 \end{cases} \tag{14}$$
$$\therefore R_{P1}(v_{\mathrm{in}}) = \begin{cases} \infty, & v_{\mathrm{in}}/V_{\mathrm{max}} = 0.33 \\ 3 \cdot P^2 \cdot R_O/[Q^2 \cdot Y], & v_{\mathrm{in}}/V_{\mathrm{max}} = 0.5 \\ 3 \cdot P^2 \cdot R_O/[4 \cdot Q^2 \cdot Y], & v_{\mathrm{in}}/V_{\mathrm{max}} = 1 \end{cases} \tag{15}$$
$$\therefore R_{P2}(v_{\mathrm{in}}) = \begin{cases} -, & v_{\mathrm{in}}/V_{\mathrm{max}} = 0.33 \\ \infty, & v_{\mathrm{in}}/V_{\mathrm{max}} = 0.5 \\ \frac{4}{3} \cdot Q^2 \cdot Y \cdot R_O, & v_{\mathrm{in}}/V_{\mathrm{max}} = 1. \end{cases} \tag{16}$$

If all of the PAs are matched to R_O at the 1 of $v_{\mathrm{in}}/V_{\mathrm{max}}$, three equations can be obtained from (14)–(16), and M, Q, and P are

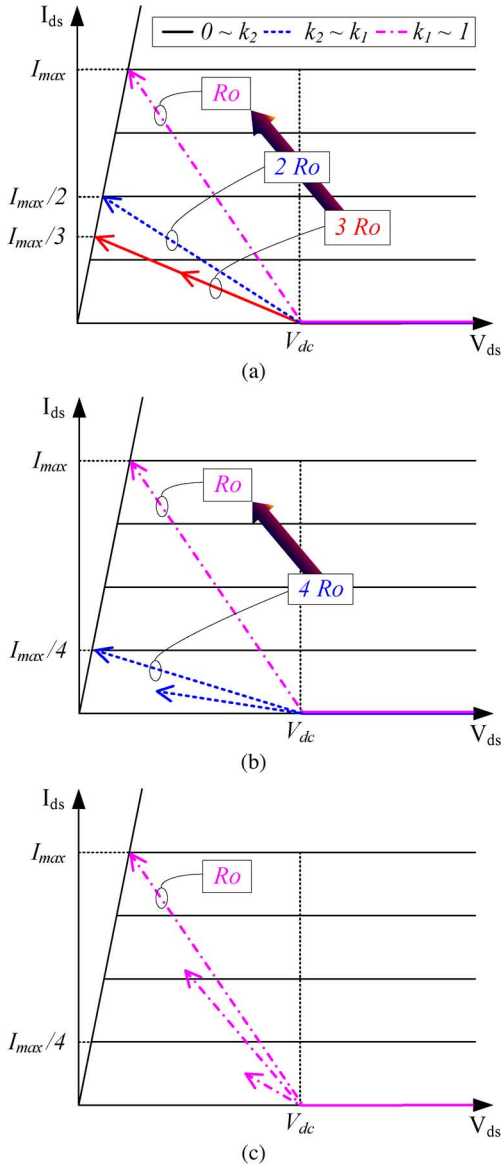


Fig. 5. Load-lines of the three-stage Doherty PA according to the input power levels. (a) Carrier PA. (b) Peaking PA 1. (c) Peaking PA 2.

calculated as a function of the Y parameter. Accordingly, each characteristic impedances can be summarized as follows:

$$\therefore\ Z_{O1} = M \cdot R_O = \sqrt{3/Y} \cdot R_O \tag{17}$$

$$\therefore\ Z_{O2} = Q \cdot R_O = \sqrt{3/(4 \cdot Y)} \cdot R_O \tag{18}$$

$$\therefore\ Z_{O3} = P \cdot R_O = R_O. \tag{19}$$

The load modulation ratios of the carrier PA are $3 \cdot R_O \sim n2 \cdot R_O \sim nR_O$, and the load modulation ratios of the peaking PA 1 and 2 are $\infty \sim 4 \cdot R_O \sim R_O$ and $- \sim \infty \sim_O$, respectively, with increasing input power. In Fig. 5, the load-lines of each PA are dynamically presented.

B. Conduction Angle of Each PA Versus Input Voltage Magnitude

To analyze the operation of the three-stage Doherty PA before and after the gate-bias adaptation, we conducted a MATLAB simulation. For the exact modeling of the peaking PA operation, we used the fundamental and dc current components derived from the conduction angle versus the input voltage magnitude.

The RF current waveform can be defined as [10], [14]

$$\therefore\ i_{\rm ds}(\theta, v_{\rm in}) = \begin{cases} I_q + I_{pk}(v_{\rm in}) \cdot \cos(\theta), \\ \quad -\alpha_{vin}/2 < \theta < \alpha_{vin}/2 \\ 0, \qquad -\pi < \theta < -\alpha_{vin}/2, \alpha_{vin}/2 < \theta < \pi. \end{cases} \tag{20}$$

I_q is a quiescent bias current, and $I_{pk}(v_{\rm in})$ is the magnitude of the drain current of a given PA. For simplicity, we assume that all of the PAs have a constant gm versus input voltage. The final conduction angle versus input voltage magnitude can be derived as [14], [23]

$$\therefore\ \alpha_{vin} = 2 \cdot \arccos\left[\frac{V_{\rm gsq}}{V_{\rm gsq} - (v_{\rm in}/V_{\rm MAX})}\right] \cdot \frac{180}{\pi}$$

where

$$\cos(\alpha_{vin}/2) = -\frac{I_q}{I_{pk}(v_{\rm in})}$$

$$I_{pk}(v_{\rm in}) = I{\rm in}(v_{\rm in}) - I_q. \tag{21}$$

$I{\rm in}(v_{\rm in})$ is an absolute amplitude of the drain current for the given input voltage, $v_{\rm in}$, and it is proportional to the input voltage. Therefore, the fundamental and dc currents of the carrier and two peaking PAs based on each conduction angle can be defined as follows:

$$\therefore\ I_C(v_{\rm in}) = \frac{I{\rm in}_C(v_{\rm in})}{2\pi} \cdot \frac{\alpha_{C,vin} - \sin(\alpha_{C,vin})}{1 - \cos(\alpha_{C,vin}/2)} = \frac{I{\rm in}_C(v_{\rm in})}{2\pi} \cdot W_C \tag{22}$$

$$\therefore\ I_{P1}(v_{\rm in}) = \frac{I{\rm in}_{P1}(v_{\rm in})}{2\pi} \cdot \frac{\alpha_{P1,vin} - \sin(\alpha_{P1,vin})}{1 - \cos(\alpha_{P1,vin}/2)} = \frac{I{\rm in}_{P1}(v_{\rm in})}{2\pi} \cdot W_{P1} \tag{23}$$

$$\therefore\ I_{P2}(v_{\rm in}) = \frac{I{\rm in}_{P2}(v_{\rm in})}{2\pi} \cdot \frac{\alpha_{P2,vin} - \sin(\alpha_{P2,vin})}{1 - \cos(\alpha_{P2,vin}/2)} = \frac{I{\rm in}_{P2}(v_{\rm in})}{2\pi} \cdot W_{P2} \tag{24}$$

and

$$\therefore\ I_{{\rm DC},C}(v_{\rm in}) = \frac{I{\rm in}_C(v_{\rm in})}{2\pi} \cdot \frac{2 \cdot sin(\alpha_{C,vin}/2) - \alpha_{C,vin} \cdot \cos(\alpha_{C,vin}/2)}{1 - \cos(\alpha_{C,vin}/2)} = \frac{I{\rm in}_C(v_{\rm in})}{2\pi} \cdot U_C \tag{25}$$

$$\therefore\ I_{{\rm DC},P1}(v_{\rm in}) = \frac{I{\rm in}_{P1}(v_{\rm in})}{2\pi} \cdot \frac{2 \cdot sin(\alpha_{P1,vin}/2) - \alpha_{P1,vin} \cdot \cos(\alpha_{P1,vin}/2)}{1 - \cos(\alpha_{P1,vin}/2)} = \frac{I{\rm in}_{P1}(v_{\rm in})}{2\pi} \cdot U_{P1} \tag{26}$$

$$\therefore\ I_{\mathrm{DC},P2}(v_{\mathrm{in}}) = \frac{I\mathrm{in}_{P2}(v_{\mathrm{in}})}{2\pi} \cdot \frac{2\cdot\sin(\alpha_{P2,vin}/2) - \alpha_{P2,vin}\cdot\cos(\alpha_{P2,vin}/2)}{1-\cos(\alpha_{P2,vin}/2)} = \frac{I\mathrm{in}_{P2}(v_{\mathrm{in}})}{2\pi}\cdot U_{P2} \tag{27}$$

where

$$\alpha_{C,vin} = 2\cdot\arccos\left[\frac{V_{\mathrm{gsq},C}}{V_{\mathrm{gsq},C} - (v_{\mathrm{in}}/V_{\mathrm{MAX}})}\right]$$
$$\alpha_{P1,vin} = 2\cdot\arccos\left[\frac{V_{\mathrm{gsq},P1}}{V_{\mathrm{gsq},P1} - (v_{\mathrm{in}}/V_{\mathrm{MAX}})}\right]$$
$$\alpha_{P2,vin} = 2\cdot\arccos\left[\frac{V_{\mathrm{gsq},P2}}{V_{\mathrm{gsq},P2} - (v_{\mathrm{in}}/V_{\mathrm{MAX}})}\right].$$

C. Efficiency of the Three-Stage Doherty PA

In the region of $0\sim0.33$ on the $v_{\mathrm{in}}/V_{\max}$ axis, only the carrier PA is operated, and the carrier and one peaking PA are operated in the region of $0.33\sim0.5$. All of the PAs are turned on in the region of $0.5\sim1$ on the axis.

The ideal current source expression of the three-stage Doherty PA in the region of $0\sim0.33$ is shown in Fig. 6(a). The load impedance at the carrier PA's current source can be written as

$$\therefore\ R_{C,\sim0.33}(v_{\mathrm{in}}) = \frac{Y\cdot Z_{01}^2}{R_O}. \tag{28}$$

The drain efficiency below the second back-off region can be calculated using the RF power and dc power as

$$\therefore\ \mathrm{DE}_{\sim0.33}(v_{\mathrm{in}}) = \frac{1}{4\pi\cdot R_O}\cdot\frac{I\mathrm{in}_C(v_{\mathrm{in}})}{I_{\max,C}}\cdot R_{C,\sim0.33}(v_{\mathrm{in}})\cdot\frac{W_C^2}{U_C} \tag{29}$$

where

$$P_{\mathrm{RF},\sim0.33}(v_{\mathrm{in}}) = 0.5\cdot I_C(v_{\mathrm{in}})^2\cdot R_{C,\sim0.33}(v_{\mathrm{in}})$$
$$P_{\mathrm{DC},\sim0.33}(v_{\mathrm{in}}) = I_{\mathrm{DC},C}(v_{\mathrm{in}})\cdot V_{\mathrm{DC}}.$$

In Fig. 6(b), which shows the region of $0.33\sim0.5$, the carrier PA and one peaking PA supply the fundamental currents to the load. The load impedances at the each current source can be calculated using the active load–pull principle [10]

$$\therefore\ R_{C,\sim0.5}(v_{\mathrm{in}}) = \frac{Y\cdot Z_{01}^2}{[1+\delta_1(v_{\mathrm{in}})]\cdot R_O} \tag{30}$$

$$\therefore\ R_{P1,\sim0.5}(v_{\mathrm{in}}) = \left[1+\frac{1}{\delta_1(v_{\mathrm{in}})}\right]\cdot\frac{R_O}{Y}\cdot\frac{Z_{O3}^2}{Z_{O2}^2}. \tag{31}$$

In the same way, the drain efficiency below the first back-off region can be calculated

$$\therefore\ \mathrm{DE}_{\sim0.5}(v_{\mathrm{in}}) = \frac{1}{4\pi\cdot R_O\cdot I_{\max,C}}\cdot\left[I\mathrm{in}_C(v_{\mathrm{in}})^2\cdot W_C^2\cdot R_{C,\sim0.5}(v_{\mathrm{in}}) + I\mathrm{in}_{P1}(v_{\mathrm{in}})^2\cdot W_{P1}^2\cdot R_{P1,\sim0.5}(v_{\mathrm{in}})\right] / \left[I\mathrm{in}_C(v_{\mathrm{in}})\cdot U_C + I\mathrm{in}_{P1}(v_{\mathrm{in}})\cdot U_{P1}\right] \tag{32}$$

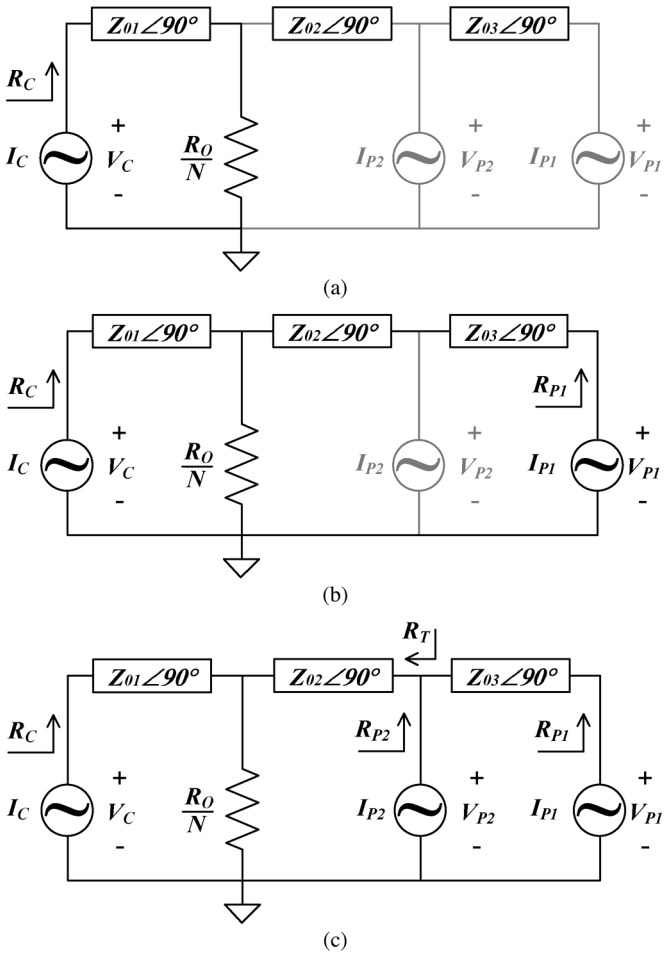


Fig. 6. Ideal current source expression of the three-stage Doherty PA. (a) Second back-off region. (b) First back-off region. (c) Full power condition (black: turned on state, gray: turned off state).

where

$$P_{\mathrm{RF},\sim0.5}(v_{\mathrm{in}}) = 0.5\cdot I_C(v_{\mathrm{in}})^2\cdot R_{C,\sim0.5}(v_{\mathrm{in}}) + 0.5\cdot I_{P1}(v_{\mathrm{in}})^2\cdot R_{P1,\sim0.5}(v_{\mathrm{in}})$$
$$P_{\mathrm{DC},\sim0.5}(v_{\mathrm{in}}) = (I_{\mathrm{DC},C}(v_{\mathrm{in}}) + I_{\mathrm{DC},P1}(v_{\mathrm{in}}))\cdot V_{\mathrm{DC}}.$$

In Fig. 6(c), which shows the region of $0.5\sim1$, all of the current sources of the PAs supply the fundamental current to the load. The load impedances at each node can also be calculated in the same way

$$\therefore\ R_T(v_{\mathrm{in}}) = \frac{\delta_1(v_{\mathrm{in}})\cdot Y\cdot Z_{O2}^2}{[1+\delta_1(v_{\mathrm{in}})]\cdot R_O} \tag{33}$$

$$\therefore\ R_{P2,\sim1}(v_{\mathrm{in}}) = \frac{[1+\delta_2(v_{\mathrm{in}})]\cdot\delta_1(v_{\mathrm{in}})}{\delta_2(v_{\mathrm{in}})\cdot[1+\delta_1(v_{\mathrm{in}})]}\cdot\frac{Y\cdot Z_{O2}^2}{R_O} \tag{34}$$

$$\therefore\ R_{P1,\sim1}(v_{\mathrm{in}}) = \frac{[1+\delta_1(v_{\mathrm{in}})]}{\delta_1(v_{\mathrm{in}})\cdot[1+\delta_2(v_{\mathrm{in}})]}\cdot\frac{R_O\cdot Z_{O3}^2}{Y\cdot Z_{O2}^2} \tag{35}$$

$$\therefore\ R_{C,\sim1}(v_{\mathrm{in}}) = \frac{Y\cdot Z_{01}^2}{[1+\delta_1(v_{\mathrm{in}})]\cdot R_O}. \tag{36}$$

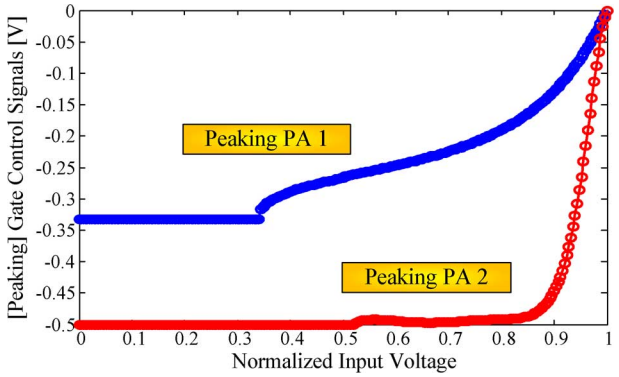


Fig. 7. Optimum gate-bias shapes for the peaking PAs versus the normalized input voltage.

The drain efficiency up to the full power state can be calculated using the RF power and dc power as

$$\begin{aligned}\therefore \mathrm{DE}_{\sim 1}(v_{\mathrm{in}}) = & \frac{1}{4\pi \cdot R_O \cdot I_{\max,C}} \\ & \cdot \left[I\mathrm{in}_C(v_{\mathrm{in}})^2 \cdot W_C^2 \cdot R_{C,\sim 1}(v_{\mathrm{in}}) \right. \\ & + I\mathrm{in}_{P1}(v_{\mathrm{in}})^2 \cdot W_{P1}^2 \cdot R_{P1,\sim 1}(v_{\mathrm{in}}) \\ & \left. + I\mathrm{in}_{P2}(v_{\mathrm{in}})^2 \cdot W_{P2}^2 \cdot R_{P2,\sim 1}(v_{\mathrm{in}}) \right] / \\ & \left[I\mathrm{in}_C(v_{\mathrm{in}}) \cdot U_C + I\mathrm{in}_{P1}(v_{\mathrm{in}}) \cdot U_{P1} \right. \\ & \left. + I\mathrm{in}_{P2}(v_{\mathrm{in}}) \cdot U_{P2} \right] \end{aligned} \tag{37}$$

where

$$\begin{aligned} P_{\mathrm{RF},\sim 1}(v_{\mathrm{in}}) = & 0.5 \cdot I_C(v_{\mathrm{in}})^2 \cdot R_{C,\sim 1}(v_{\mathrm{in}}) \\ & + 0.5 \cdot I_{P1}(v_{\mathrm{in}})^2 \cdot R_{P1,\sim 1}(v_{\mathrm{in}}) \\ & + 0.5 \cdot I_{P2}(v_{\mathrm{in}})^2 \cdot R_{P2,\sim 1}(v_{\mathrm{in}}), \\ P_{\mathrm{DC},\sim 1}(v_{\mathrm{in}}) = & \left(I_{\mathrm{DC},C}(v_{\mathrm{in}}) + I_{\mathrm{DC},P1}(v_{\mathrm{in}}) + I_{\mathrm{DC},P2}(v_{\mathrm{in}}) \right) \\ & \cdot V_{\mathrm{DC}}. \end{aligned}$$

D. MATLAB Simulation Results of the Three-Stage Doherty PA With and Without the Gate ET Operation

For the simulation, the conduction angle of the carrier PA at the full power state was set to 180° ($V_{\mathrm{gs}q,C} = 0$), and those of the peaking PAs were set to 151.05° ($V_{\mathrm{gs}q,P1} = -0.33$) and 141.06° ($V_{\mathrm{gs}q,P2} = -0.5$) to turn on the PAs above k_2 and k_1, respectively [14], to deliver the maximum efficiency of the carrier and peaking PA 1. The drain dc bias applied was 30 V. In Fig. 7, the optimum gate-bias shapes versus the normalized input voltage magnitude are illustrated, and the biases were increased from the class C mode to enhance the output power of each peaking PA as the input power level was increased. Fig. 8 illustrates the simulation results of the three-stage Doherty PA with and without the gate adaptation to the peaking PAs. Fig. 8(a) shows the simulated fundamental drain current increment of each PA [24]. Without the gate-bias adaptation, the fundamental drain currents of the peaking PA 1 and 2 did not reached 1 A (which is the maximum drain current of each PA) due to the low gate biases. Fig. 8(b) shows the fundamental drain voltage variation versus the normalized input voltage. As

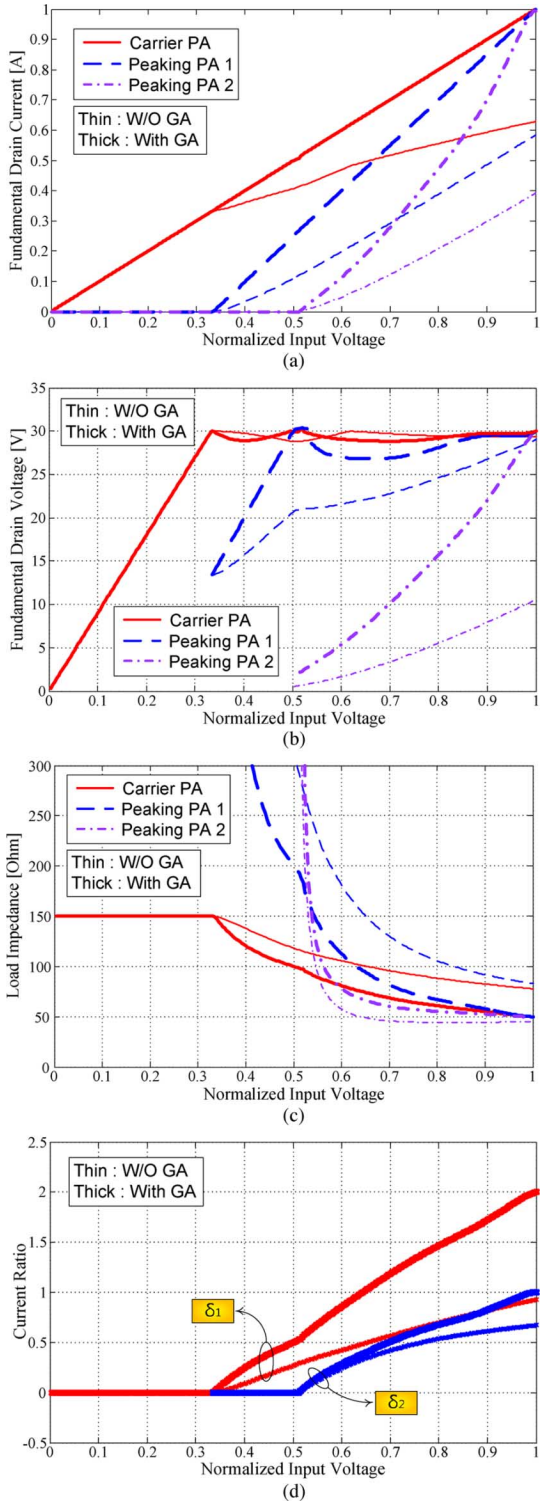


Fig. 8. Simulation results of the "1:1:1" three-stage Doherty PA with and without the gate-bias adaptation (GA). (a) Fundamental drain currents. (b) Fundamental drain voltages. (c) Fundamental load impedances at the each current source. (d) Calculated δ_1 and δ_2.

expected from Fig. 8(a), the drain voltage of the two peaking PAs do not reach 30 V. In particular, the fundamental current and voltage of the peaking PA 2 show significantly insufficient load modulation. The load impedance variation at each current source is presented in Fig. 8(c) and Table III. None of the PAs

TABLE III
LOAD IMPEDANCE VARIATIONS OF THE THREE-STAGE DOHERTY PA WITH AND WITHOUT THE GATE-BIAS ADAPTATION VERSUS THE INPUT POWER LEVEL

$[Before/After]$	$0 \sim 0.33$	$0.33 \sim 0.5$	$0.5 \sim 1$
$Carrier$	150/150 Ω	118.2/100 Ω	77.8/50 Ω
$Peaking\ 1$	∞	313.8/203 Ω	45/50 Ω
$Peaking\ 2$	∞	∞	94.5/50 Ω

reached the required load impedances after 0.33 of the normalized input power level. The fundamental drain current ratios, δ_1 and δ_2, had to be increased from 0 to 2 and from 0 to 1, respectively. The variations of δ_1 and δ_2 are shown in Fig. 8(d).

The optimum gate biases help the fundamental current expansion of each peaking PA and are generated by monitoring the fundamental drain voltage and load impedance of each peaking PA because these parameters determine the efficiency and output power (or gain flatness) characteristic versus input voltage level of the Doherty PA. In the region of $0.33 \sim 0.5$ on the normalized input voltage axis, only the gate bias of the peaking PA 1 is increased. As the gate bias is increased, the fundamental drain voltage of the PA reaches 30 V, and the load impedance converges to $4 \cdot R_O$ of the load impedance in Fig. 8(a) and (b). In the region of $0.5 \sim 1$, both of the gate biases of the peaking PAs have to be adapted. After applying the gate-bias adaptation, all of the fundamental drain currents of the PAs reach the maximum magnitude, and the fundamental drain voltage of the carrier PA and peaking PA 1 remain near 30 V. The load impedances of all PAs also converge the 50 Ω, and the proper load modulation behavior is clearly achieved within the overall input power level. δ_1 and δ_2 are also enhanced to 2 and 1, respectively.

In Fig. 9(a), the simulated load-lines of each PA are illustrated, with only the left-side at a $V_{\rm DC}$ of 30 V, for simplicity. As shown in the figure, without the gate control, the peaking PAs do not reach the knee region because the fundamental drain voltages of the two peaking PAs do not reach 30 V. This operation causes a serious efficiency degradation of the two peaking PAs, and the overall efficiency of the Doherty PA is decreased at the backed-off output power region, as shown in Fig. 9(b). Therefore, the optimum gate bias have to be properly shaped such that the fundamental drain voltage of the carrier PA and peaking PA 1 remain at 30-V magnitude. In this simulation, for simplicity, the gate bias of the peaking PA 1 is determined such that the fundamental drain current of the PA is linearly increased. The gate bias of the peaking PA 2 is then optimally shaped based on the above criteria for the maximum efficiency of the Doherty PA. The improper load modulation reduces the peak power by about 3.54 dB. The simulated gain flatness versus output power level is depicted in Fig. 9(c). The calculated gain flatness is improved from 3.8 to 1 dB after applying the gate-bias control technique, indicating the more linear AM–AM response of the proposed PA.

In Fig. 10, the calculated dc and RF powers of each PA and the overall three-stage Doherty PA are illustrated. By applying the gate-bias control technique, the RF power generation of the two peaking PAs is significantly enhanced, and the three-stage Doherty PA delivers the full power to the load. In Table IV, the

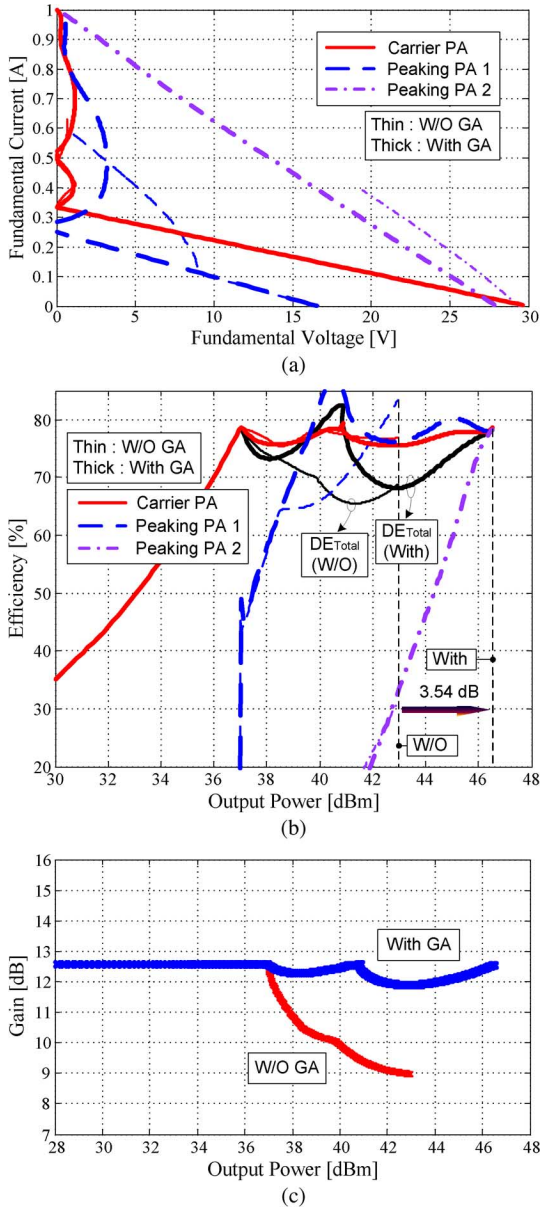


Fig. 9. Simulated: (a) fundamental load-line behavior, (b) efficiency characteristic, and (c) gain characteristic of the "1:1:1" three-stage Doherty PA with and without the gate-bias adaptation.

calculated performances of the three-stage Doherty PA with and without the gate-bias control technique are summarized for the WiMAX signal with 8.5-dB PAPR. The proposed Doherty PA shows enhanced efficiency together with an improved average output level. These simulation results clearly show the limitation on the load modulation behavior of the normal three-stage Doherty PA, and that this limitation can be removed by the gate-bias control technique.

E. Output Impedance Consideration of the Peaking PAs

A high output impedance of the peaking PA in the off state is essential; otherwise, the output power of the carrier PA can leak to the peaking PA, reducing the output power and efficiency [25]. For the new three-stage Doherty PA, the peaking PAs are connected to the output power combining node (V_o) through

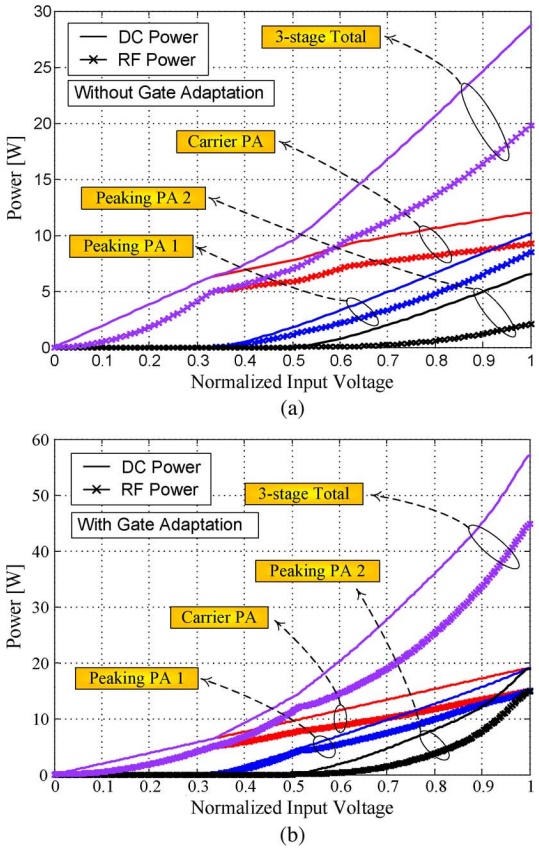


Fig. 10. Simulated dc and RF power of each PA: (a) without and (b) with the gate-bias adaptation.

TABLE IV
CALCULATED PERFORMANCE OF THE THREE-STAGE DOHERTY PA WITH AND WITHOUT THE GATE-BIAS ADAPTATION FOR THE 802.16e MOBILE WiMAX SIGNAL WITH 8.5-dB PAPR

Gate Control	$Pout_{Avg}$	DE_{Avg}	$Gain_{Avg}$	PAE_{Avg}
Before	36 dBm	66.1 %	11.2 dB	61.2 %
After	37.1 dBm	68.5 %	12.3 dB	64.5 %

the two quarter-wave transformers, as shown in Fig. 11(a). In fact, the final output impedance (R_{out}) at the output node is determined by $P \cdot R_O$ and $Q \cdot R_O$ as follows:

$$\therefore\ R_{\text{out}} = \left(\frac{Q}{P}\right)^2 \cdot R'_{\text{out}} = \frac{3}{4Y} \cdot R'_{\text{out}}. \tag{38}$$

Thus, as the parameter Y becomes smaller, the final output impedance (R_{out}) becomes higher, and the leakage through the peaking PA can be minimized. If the matching impedance of the peaking PA at the maximum output power is not matched to 50 Ω, but to $\sigma \cdot 50\ \Omega$, the final output impedance becomes:

$$\therefore\ R_{\text{out}} = \left(\frac{Q}{P}\right)^2 \cdot R'_{\text{out}} = \frac{3}{4\sigma \cdot Y} \cdot R'_{\text{out}}. \tag{39}$$

Consequently, the final output impedance (R_{out}) at the output node (V_o) is inversely proportional to the two parameters of Y and σ. However, if the matching impedance of the peaking PA is decreased, the output impedance of the peaking

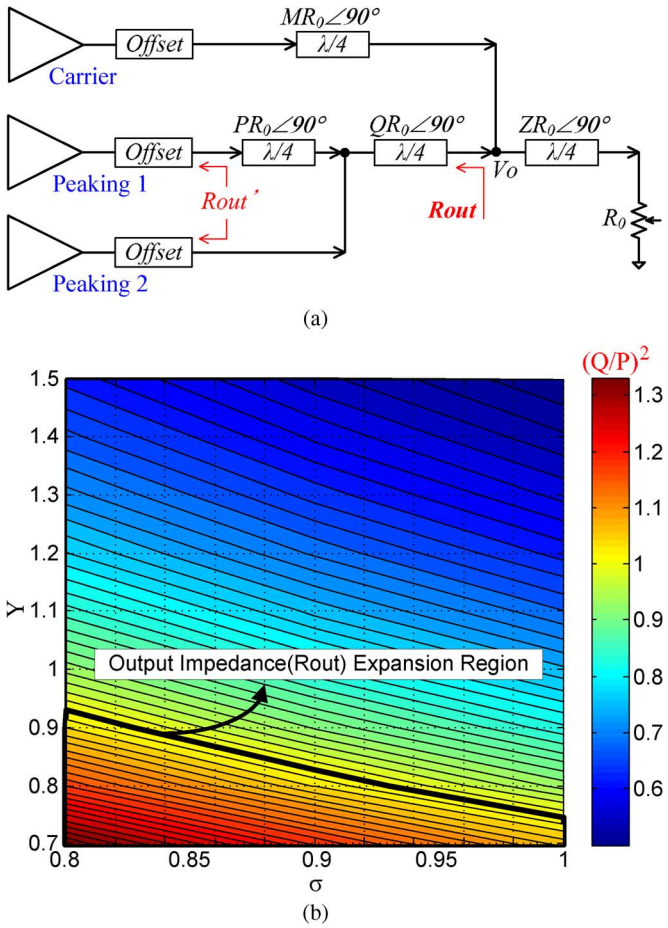


Fig. 11. (a) Output circuit topology of the new three-stage Doherty PA. (b) Output impedance (R_{out}) at the output combining node (Vo) versus Y and σ.

PA (R'_{out}) is also reduced because the characteristic impedance of the offset-line is also decreased. Therefore, a large reduction in σ is not recommended. In this analysis, we assume that the σ value ranges from 0.8 to 1 (40 Ω ∼ 50 Ω), which does not affect the output impedance of the peaking PA (R'_{out}). The simulated final output impedance (R_{out}) expansion from the R'_{out} is shown in Fig. 11(b). As shown in the figure, if all of the PAs are matched to 50 Ω, a Y parameter up to 0.75 causes the final output impedance (R_{out}) to decrease, and it can disturb the proper load modulation. On the other hand, the selection of a small Y value can cause the linewidth problem of the quarter-wave transformer (M) due to the high characteristic impedance. Therefore, the Y value has to be selected by considering the output impedance of the peaking PA and the linewidth of the quarter-wave transformer for a given substrate. In Table V, the implemented output combiner using TACONIC's TLY-5 $(\epsilon_r = 2.2)$ substrate is summarized.

IV. IMPLEMENTATION AND MEASURED RESULTS

As a unit cell of the Doherty PA, a class AB mode PA was designed at 2.655-GHz using Cree's CGH40045 GaN HEMT device [22]. The quiescent bias current of the carrier PA is 55 mA, and the PA delivers 64.6% of the drain efficiency at an output power of 46.4 dBm. Under the quiescent bias point at the

TABLE V
OUTPUT COMBINING CIRCUIT DESIGN OF THE THREE-STAGE DOHERTY PA USING THE TLY-5 SUBSTRATE

Y	σ	Z_{O1} (width)	Z_{O2} (width)	Z_{O3} (width)	Z_{O4} (width)
0.75	1	100 Ω (0.65 mm)	50 Ω (2.38 mm)	50 Ω (2.38 mm)	57.74 Ω (1.9 mm)

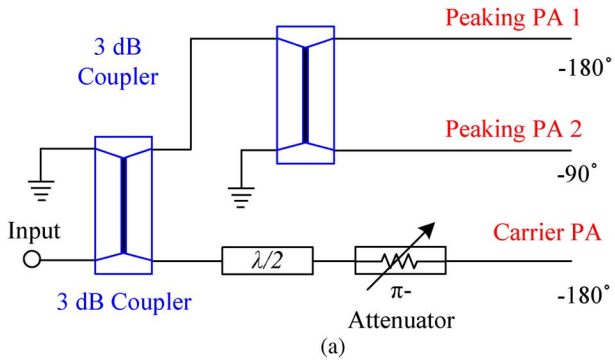
deep class C mode, the offset-line length of the implemented PA was determined to achieve the proper Doherty operation. The measured phase offset was 72°, and the transformed output impedance (R_{out}) was 1.4 kΩ.

A. Uneven Input Power Drive Method

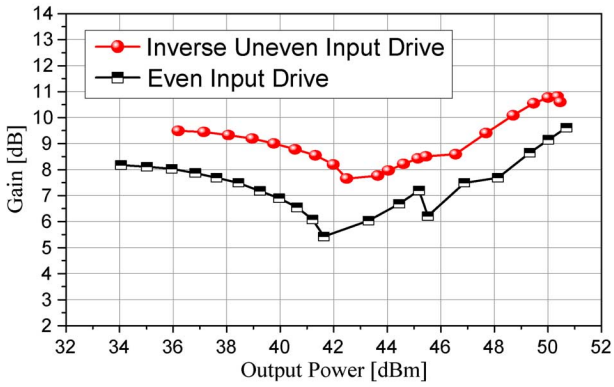
If the three-way input power dividing circuit, which has an equal dividing ratio, is used, the input power of each PA is 1/3 decreased about −4.77 dB than the total input power. Since the load of the carrier PA is initially $3{\cdot}50\ \Omega$ in the region of $0 \sim 0.33$, the overall gain of the three-stage Doherty PA can be maintained the same with the unit PA under a 50-Ω load impedance. However, the load of the carrier PA can be completely modulated and cause a serious gain degradation similarly to the three-way Doherty PA. To minimize the gain degradation, the input power dividing circuit has to be changed, more input power should be applied to the carrier PA than to the other PAs, and the carrier PA should reach its full power early under the $3 \cdot 50\ \Omega$ load condition. This input dividing method does not significantly affect the overall efficiency of the three-stage Doherty PA along the output power when the gate-bias adaptation is also used. In Fig. 12(a), the uneven input dividing circuit topology is shown. To adjust the input dividing ratio, a pi-attenuator was used. The attenuation level has to be selected by simultaneously monitoring the peak power of the three-stage Doherty PA and the gate current of the carrier PA, and the selected attenuation level was 1.7 dB. Here, we could employ an elaborate power divider without the lossy components. Fig. 12(b) shows the 1.5-dB gain improvement of the implemented three-stage Doherty PA with the input driving method.

B. Measured Results of the Continuous Wave (CW) Signal

Fig. 13 shows the measured optimum gate-bias control shapes versus input power level. A constant gate bias was applied to the carrier PA. The gate biases of the other PAs were initially maintained at deep class C modes for the turned-off operation. To minimize the gate voltage swing, which is relative to the size of the gate-bias modulator, the initial gate biases of the two peaking PAs were fixed to −6.7 and −9.5 V, respectively, along the output power level. Above each backed-off average output power level, the gate biases of the PAs were increased to the class AB mode to accelerate the load modulation. The measured results versus the output power level for a one-tone signal are summarized in Fig. 14. Fig. 14(a) shows the dc current profiles of each PA. By using the gate-bias adaptation, the peaking PA was properly turned on at the backed-off output power. Furthermore, the Shottky turn-on problem of the carrier PA was clearly eliminated. The measured efficiency performances are illustrated in Fig. 14(b). Above the second backed-off output



(a)



(b)

Fig. 12. (a) Uneven input power drive circuit. (b) Measured gain profiles of the proposed three-stage Doherty PA with even and uneven input power drive circuits for a one-tone signal.

power region, the proposed PA maintained an efficiency of 55% with ±1.6 dB of gain flatness. The gain of the implemented three-stage Doherty PA could be increased by optimizing the unit PA for the gain under the modulated load impedance. In this experiment, the carrier PA was optimized to obtain a high efficiency under a $3 \cdot 50\ \Omega$ load impedance.

C. Measured Results for the Modulation Signal

Using the gate-bias shaping functions shown in Fig. 13, the ET signals for each peaking PA were generated by the MATLAB simulator. Agilent's ESG4438C was used as a signal source and delivered the signals to the gate driver circuit, which was implemented as a noninverting type of gain amplifier using the TI's THS3001 OP-Amp. To investigate the efficiency of the proposed three-stage Doherty PA versus the average output power, an 802.16e Mobile WiMAX signal with a 7.8-dB PAPR and a 10-MHz signal bandwidth was used. Fig. 15(a) shows the measured efficiencies of the ET three-stage Doherty PA with and without the gate-bias adaptation. As expected from the MATLAB simulation, the efficiency and gain of the three-stage Doherty PA with gate-bias adaptation were significantly improved at the backed-off average output power level. The implemented three-stage Doherty PA with gate-bias adaptation delivered a 56.9% drain efficiency at an average output power of 42.58 dBm, which was a 7.9-dB backed-off output power from the peak power level. The MATLAB simulation in Table IV did not consider the knee voltage of the PA, output matching, and combining loss. Furthermore, the carrier PA in the simulation was assumed to be a class B mode PA, which has a maximum

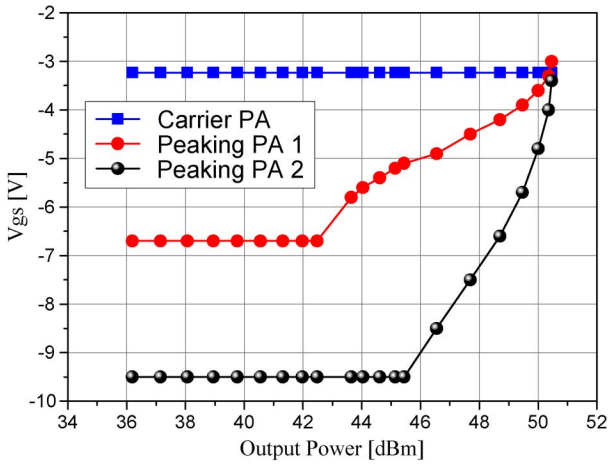


Fig. 13. Gate-bias shapes versus input voltages used in the experiment.

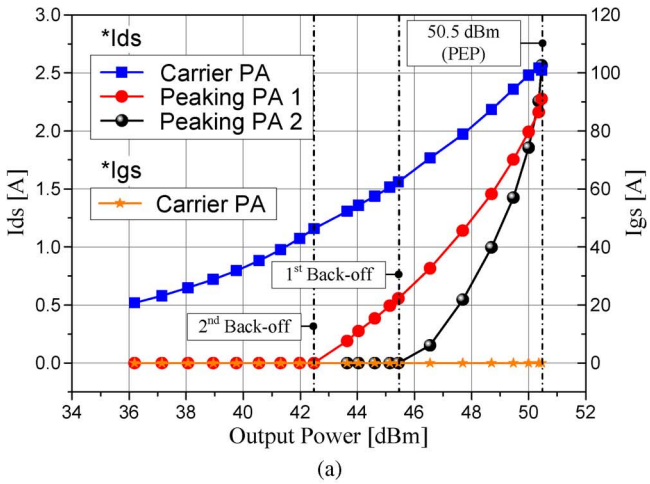


Fig. 14. Measured CW characteristics of three-stage Doherty PA. (a) DC current profiles. (b) DE, power-added efficiency (PAE), and gain performances of the proposed three-stage Doherty PA.

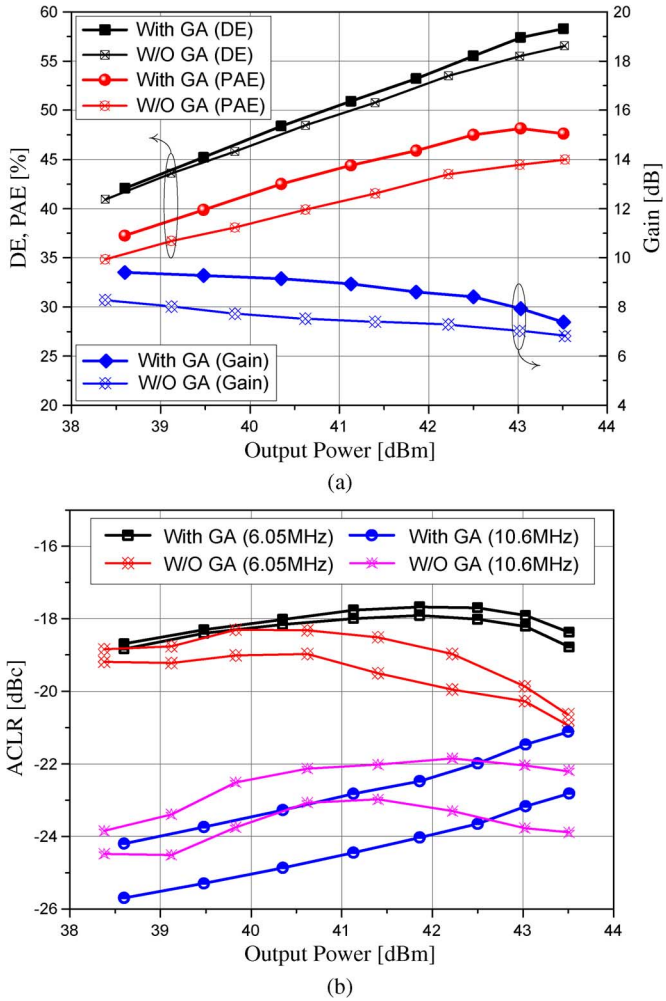


Fig. 15. Measured performances of a three-stage Doherty PA with and without the gate-bias adaptation. (a) DE, gain, and PAE characteristics. (b) Upper and lower ACLRs.

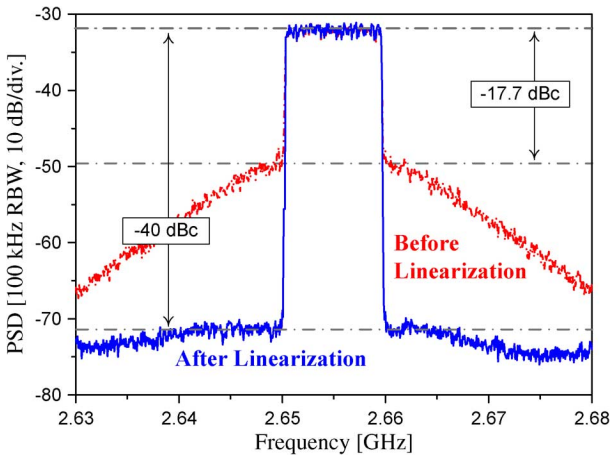


Fig. 16. Measured output spectra of the ET three-stage Doherty PA before and after the linearization.

efficiency of 78.5%. Thus, the simulated efficiency was higher than the measured efficiency. Fig. 15(b) presents the linearity of the proposed three-stage Doherty PA at 6.05- and 10.6-MHz offsets. Since the gate-bias control was optimized for the load modulation behavior to achieve maximum efficiency and peak power and not for the linearity, the adjacent channel leakage ratios (ACLRs) are not good. Accordingly, the DPD technique is essential for the linearity specification. The measured relative constellation error (RCE) was −17.06 dB before linearization. To linearize the three-stage Doherty PA, the digital feedback

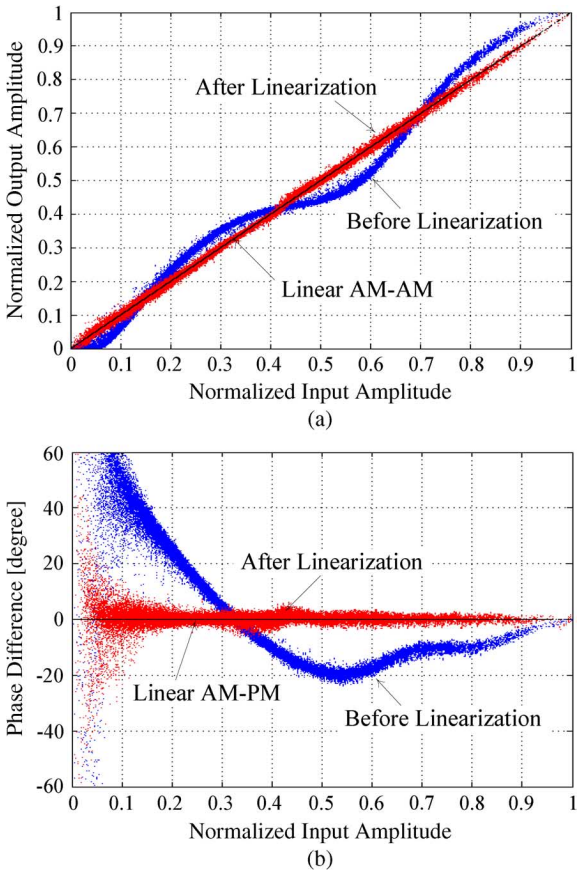


Fig. 17. Measured AM–AM and AM–PM characteristics of the three-stage Doherty PA before and after linearization. (a) AM–AM. (b) AM–PM.

TABLE VI
PERFORMANCE COMPARISON OF THE 3GPP WCDMA AND MOBILE WiMAX TRANSMITTER USING GaN TECHNOLOGY

–	*Kimball et al.* [7]	*Deguchi et. al.* [11]	*Pelk et. al.* [13]	*Our Work*
Topology	*ET*	*Doherty* $2-way$	*Doherty* $3-stage$	*Doherty* $3-stage$
Freq.	2.14 GHz	2.6 GHz	2.14 GHz	2.655 GHz
Signal	*WCDMA*	*WCDMA*	*WCDMA*	*WiMAX*
PAPR	7.67 dB	6.9 dB	11.5 dB	7.8 dB
$Back-off$	6 dB	7.3 dB	11.5 dB	8 dB
Pout	45.7 dBm	45.2 dBm	38.5 dBm	42.54 dBm
DE	53.4 %	55 %	55 %	55.4 %

predistortion (DFBPD) was applied to the RF input signal and the gate bias [1] to maximize the linearization. The measured output spectra before and after the linearization are presented in Fig. 16. By employing the DFBPD algorithm, the ACLR at the 6.05-MHz offset was linearized to −40 dBc. The measured AM–AM and AM–PM responses before and after the linearization are shown in Fig. 17, and a linear AM–AM and AM–PM response was successfully achieved. After the linearization, an efficiency of 55.45% was obtained at an average output power of 42.54 dBm, an 8-dB backed off output power from the peak power level, while maintaining a gain similar to that before linearization. The RCE was also enhanced to −33.15 dB,

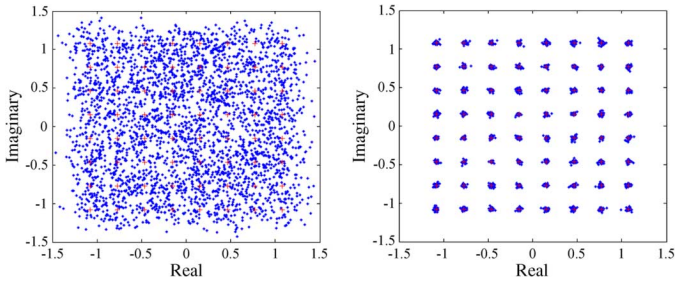


Fig. 18. Measured signal constellation diagrams of the ET three-stage Doherty PA, (*left*) before and (*right*) after linearization.

successfully satisfying the system specifications. The performances of the 3GPP WCDMA and mobile WiMAX transmitter using GaN technology are summarized in Table VI, and the efficiency of our work is the state-of-the-art performance for the WiMAX application at 2.655 GHz. The constellation diagrams before and after the linearization are also presented in Fig. 18. These experimental results clearly show that the proposed three-stage Doherty PA with the ET technique has a superior efficiency with a high peak power, and it is suitable for use as a linear transmitter.

V. CONCLUSIONS

In this paper, we have analyzed a new three-stage Doherty PA. It was verified through MATLAB simulation that the three-stage Doherty PA has the highest efficiency versus output power level among the various Doherty architectures, and its operation principles and optimum design method were clearly described. Furthermore, we have found that the three-stage Doherty PA has a serious improper load modulation problem, and by applying the gate-bias control technique, a proper load modulation can be achieved. The unit PA was designed using Cree's CGH40045 GaN HEMT device at 2.655 GHz. In the experiment, the gate bias was adapted to achieve the maximally efficient Doherty operation. To enhance the gain along the output power, the uneven input dividing circuit was employed. After linearization, the proposed three-stage Doherty PA had an excellent efficiency of 55.4% at an average output power of 42.54 dBm, an 8-dB backed-off from the peak output power level. The RCE was −37.23 dB, satisfying the system specification. These results clearly show that the ET three-stage Doherty PA is a very powerful architecture for achieving a high efficiency, and the proposed gate-bias control method employing the ET technique is essential for obtaining the proper load modulation behavior.

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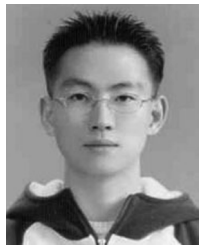

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