Design of Bandwidth-Enhanced Doherty Power Amplifiers for Handset Applications

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***Abstract*—A quarter-wavelength impedance transformer as well as a number of other factors limit the bandwidth (BW) of Doherty power amplifiers (PAs). We utilize the lower Q of a quarter-wavelength transformer and propose a phase compensation circuit and an additional offset line to be incorporated into the matching networks for an enhanced BW of the Doherty PA. The quarter-wavelength transformer and the final output circuit have the same Q. Input dividing networks are also analyzed for operation of broad BW. The Doherty PA for long term evolution (LTE) applications is integrated into a 1.4×1.4 mm^2 die using an InGaP/GaAs hetero-junction bipolar transistor (HBT) process. For an LTE signal with a 7.5-dB peak-to-average power ratio (PAPR) and a 10-MHz BW, the PA with a supply voltage of 4.5 V delivers a power-added efficiency (PAE) of 36.3% and an adjacent channel leakage ratio (ACLR) of -32 dBc with an average output power of 27.5 dBm at a frequency of 1.85 GHz. Across frequencies from 1.6–2.1 GHz, the PA performs with a PAE of more than 30%, a gain of more than 28 dB and an ACLR of less than -31 dBc at an average output power of 27.5 dBm while satisfying the standard spectrum mask. These figures verify that the proposed bandwidth enhancement techniques are effective for handset Doherty PAs.**

***Index Terms*—Broadband, doherty, efficient, handset, hetero-junction bipolar transistors (HBT), linear, long-term evolution (LTE), MMIC, power amplifier (PA).**

I. Introduction

MULTIBAND multimode radio frequency (RF) transceivers are demanded for cost and size reduction in wireless communication markets. However, it is still difficult to integrate power amplifiers (PAs) using CMOS processes into CMOS transceivers because of noise from local oscillation (LO) frequency pulling as well as the poor performance of CMOS PAs. Recently, phone manufacturers have started to integrate the multimode multiband PAs with front-ended blocks, i.e., filters and switches, rather than with RF transceivers [1]. Multimode operation of PAs can be achieved by employing supply modulators to control the rated output power and optimize linearity/efficiency. Multiband operation can be accomplished by utilizing broadband or dual-band techniques.

In addition, wireless telecommunication companies have started to utilize the fourth generation (4G) systems, such as long-term evolution (LTE) and worldwide interoperability for microwave access (WiMAX), because of their high data rates. However, the 4G applications have several challenging issues that must be addressed by RF transceiver designers, such as high data bandwidth (BW) and high peak-to-average-power ratio (PAPR). In particular, the high PAPR decreases the efficiency of PAs because PAs amplify a signal in back-off power regions. PAs inherently have lower efficiency in the low power region because of the fixed supply voltage and the optimized load impedance at the maximum power [2]–[4].

Envelope elimination and restoration (EER), envelope tracking (ET), linear amplification with nonlinear components (LINC), and Doherty techniques enhance efficiency for high PAPR applications as well as for the low power level of signals. The Doherty technique, invented in the 1930s [5], is one way to efficiently amplify high PAPR signals by modulating the load impedances for back-off power operation. The EER technique modulates the supply voltage according to the power level of a PA, which enhances efficiency. Studies have verified that the ET structure is a strong candidate for multimode multiband PAs [6], [7]. The Doherty PA with an ET structure further increases efficiency for high PAPR signals and low power level operations [8]. Thus, we focus on the BW-enhanced Doherty technique in this paper to reach an eventual goal of multimode multiband operation.

The design of the Doherty PAs in the real world should take into account the differences between real PAs and the ideal theory. A class-C-biased peaking amplifier, employed for turn-off in low power regions, inconsistently divides the input power between each path due to the variation of the amplifier's input capacitance. This results in nonlinear operation caused by a lower g_m. In addition, the amplifier's output capacitance causes imperfect load modulation and degrades efficiency and linearity. Those factors also degrade BW performance of the Doherty PAs.

M. Sarkeshi, *et al.* [9] proposed an adaptive quarter-wavelength transformer that used varactors depending on the frequency and increased the fractional BW to 20% (1.8–2 GHz). J. H. Qureshi *et al.* [10] noted that the output capacitance of transistors as the BW limiting factor and merged the capacitance into the capacitor of the quarter-wavelength transformer, leading to the fractional BW of 30%. K. Bathich *et al.* [11] showed that the quarter-wavelength transformer itself has a fractional BW of 35%. They used ladder-type multi-section

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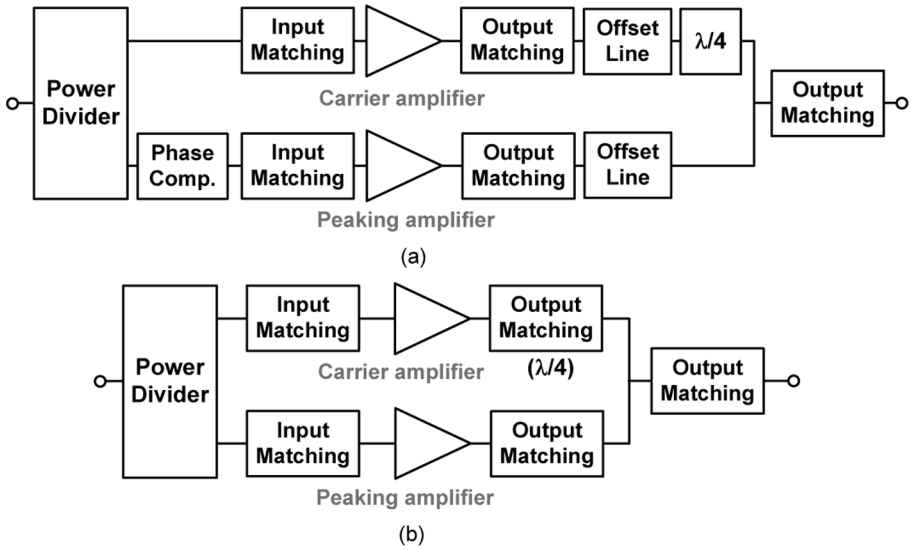

Fig. 1. (a) Structure of a conventional Doherty PA. (b) Structure of the proposed Doherty PA.

matching circuits to maintain the BW performance. The authors further improved the fractional BW of the Doherty PA to 42% using the quarter-wavelength line with a reduced impedance transformation ratio [12]. However, the techniques introduced above focus mainly on the output matching circuit, even though the inconsistent dividing of input power degrades the BW of the output matching circuits. It is also difficult to implement the varactor and the ladder-type multi-section network using a microstrip line for handset PAs in terms of size and loss.

The paper [13] proposed a direct input power divider that takes into account the input impedance variations and the output matching circuits using the same impedance transformation ratio, and it achieved a fractional BW of 20%, but only 8% without the use of a DPD technique. In [14], we found that an additional phase compensation network and an offset line, shown in Fig. 1(a), degrade the BW of the Doherty PA more than a quarter-wavelength transformer does, and we propose to merge the additional phase compensation network and the offset line to the broadband input and output matching circuits, respectively, as illustrated in Fig. 1(b).

In this extended paper, we further analyze the BW limiting factors in Section II. We compare the input dividing networks utilizing the direct dividing technique and the Wilkinson power divider for BW enhancement in Section III. In Section IV, the implementation of a broadband Doherty PA is explained, and more experimental results are illustrated. With the BW enhancement technique, the PA has a PAE of more than 30% across the fractional BW of 27% while satisfying the standard spectrum mask of the LTE signal.

II. BW Limiting Factors and BW Enhancement for Doherty PAs

The following BW limiting factors for Doherty operation are addressed in this section: quarter-wavelength transformers, different bias levels of two parallel amplifiers, phase compensation networks, offset lines, in/output matching circuits, and the cancellation of inter modulation distortions (IMDs) from two amplifiers for linear operation. BW enhancement techniques that address these BW limiting factors are also explained.

A. Doherty Configuration and Quarter-Wavelength Transformer

As shown in Fig. 1(a), a Doherty configuration consists of two parallel amplifiers that are connected by a power divider for the input and a quarter-wavelength transformer for the output. At the output combining junction, the load for each path is determined by the ratio of the currents. The load (R_{oc}) at the path of the carrier (main) amplifier is the same as that at the junction $(R_o/2)$ until the peaking (auxiliary) amplifier turns on. The load (R_{op}) on the path of the peaking amplifier decreases from infinity to R_o since the peaking amplifier generates a current, while R_{oc} increases from $R_o/2$ to R_o at the maximum output power. It is assumed that the currents of the carrier and the peaking amplifiers are the same at the maximum output power. Load modulation is achieved by the ratio of the currents. However, the optimum load for the carrier amplifier at 6-dB back-off power is not $R_o/2$ but $2R_o$ when R_o is the optimum load at the maximum power. Thus, the quarter-wavelength transformer with the characteristic impedance of R_o is placed on the carrier path as an impedance inverter. The optimum loads $2R_o$ and R_o result in the peak efficiency at the 6-dB back-off and the maximum power, respectively. The impedance relationship of the quarter-wavelength transformer is

$$Z_o^2 = R_{\mathrm{opt},c} \cdot R_{oc} \tag{1}$$

where Z_o is the characteristic impedance of the transformer.

To figure out the BW characteristics of quarter-wavelength transformers, we need to explore the BW of the low-pass filter

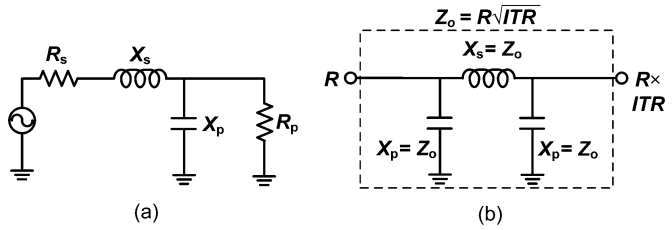

Fig. 2. (a) Low-pass filter. (b) Lumped quarter-wavelength transformer. The dotted box can be a quarter-wavelength transmission line with the characteristic impedance of Z_o. ITR: impedance transformation ratio.

illustrated in Fig. 2(a). A loaded Q_L and a circuit node Q_n for the low-pass filter are defined by

$$Q_n = \frac{R_p}{X_p} = \frac{X_s}{R_s} = \sqrt{\frac{R_p}{R_s} - 1}$$
$$Q_L = \frac{Q_n}{2} = \frac{f_o}{\mathrm{BW}} \tag{2}$$

where R_s and R_p are the series and the parallel resistances, respectively, and X_s and X_p are the series and the parallel reactances, respectively. BW is inversely proportional to Q_n, and the smaller impedance transformation ratio results in a greater BW.

The quarter-wavelength transformer shown in Fig. 2(b) can be separated into two low-pass filters. The higher Q of the low-pass filters is expressed as

$$Q_n = \frac{R_p}{X_p} = \frac{R \cdot \mathrm{ITR}}{R\sqrt{\mathrm{ITR}}} = \sqrt{\mathrm{ITR}} \tag{3}$$

where ITR is the impedance transformation ratio of the transformer. Thus, the Q of the quarter-wavelength transformer is $\sqrt{\mathrm{ITR}}$, the same as the worst BW for the two low-pass filters.

Fig. 3(a) illustrates the impedance transformation and the Q for lumped and transmission line transformers. An ITR of 4 indicates the load modulation in the 6 dB back-off power condition for the conventional Doherty PA, and an ITR of 1 indicates the impedance transformation in the maximum power condition. An ITR of 2 gives the same impedance transformation for the back-off and maximum power conditions. For more than 6 dB back-of power, the load impedance of $2R$ is obtained from R by the characteristic impedance $\sqrt{2}R$ of the transformer at the output combining junction of the carrier and the peaking amplifiers. The load impedances of R for the carrier and the peaking amplifiers in the maximum power condition is obtained from $2R$ at the output combining junction.

Fig. 3(b) shows the simulated BW characteristics. The transmission line transformer with an ITR of 4 has a 35% fractional bandwidth at a VSWR of 1.5 [11], i.e., 650-MHz BW at a center frequency of 1.85 GHz (TL $\mathrm{ITR} = 4$). Transmission line transformers always have a wider BW than lumped-type transformers. The lower ITR results in a wider BW. The maximum achievable BW is reached with an ITR of 2, which delivers the lowest ITR for both the back-off and the maximum power conditions.

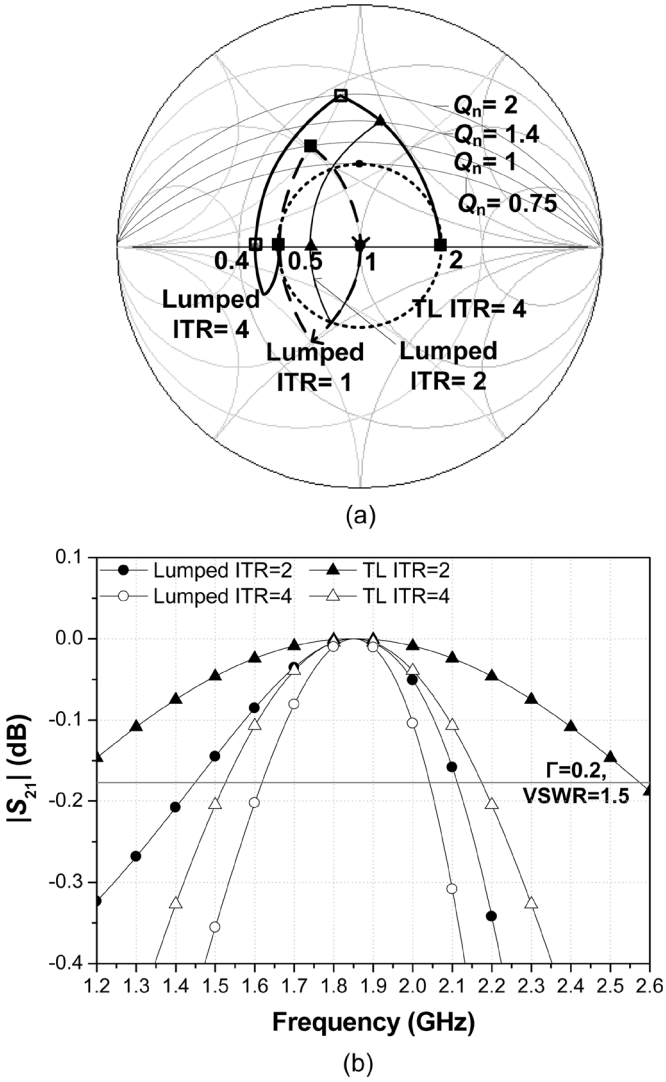

Fig. 3. (a) Impedance transformation of quarter-wavelength transformers. Impedances on the Smith chart are normalized. (b) BW of lumped and transmission line (TL) quarter-wavelength transformers.

Even though the impedance transformer with an ITR of 2 delivers the maximally achievable BW, the final output circuit, located after the junction of the carrier and the peaking amplifiers, requires more matching elements to maintain the Q of the quarter-wavelength transformer. In this design, therefore, a proper Q is determined by considering the loss and the BW from the overall matching circuits. This will be explained in Section II.D.

B. Class-C-Biased Peaking Amplifier

The Doherty PA requires a class-C-biased peaking amplifier that turns off in low power regions, while the carrier amplifier is biased at a class-AB level for linear operation. However, the class-C bias for the peaking amplifier causes non-ideal operation of the Doherty PA. The gain with the class-C bias expands as the input power increases, and the input capacitance grows significantly because of the turn-on process of the transistor. The input impedance of the peaking amplifier varies with the input power level, disturbing the consistent division of power

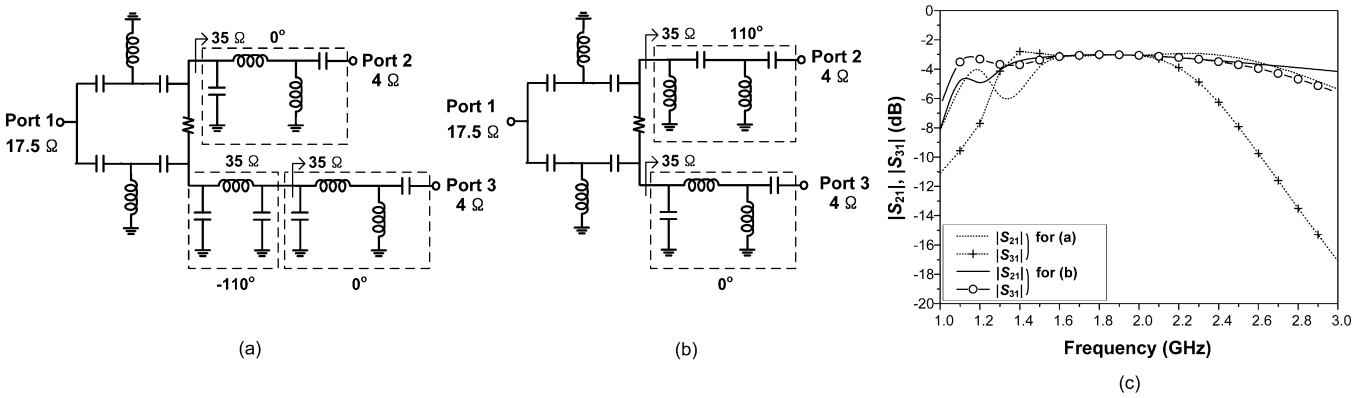

Fig. 4. (a) Doherty input network with an additional phase compensation circuit. (b) Doherty input network with a merged phase compensation circuit. (c) BW of Doherty input networks.

between the carrier and peaking amplifiers. The inconsistent input impedance weakens the broadband operation of Doherty PAs.

Broadband input matching circuits that absorb the average input-capacitance of amplifiers are required for consistent division of power and input matching across a broad BW. In addition, the significant variation of the input impedance with input power levels of the peaking path should be carefully considered, and an appropriate dividing network should be connected to the input. This issue is discussed in more detail in Section III.

Another problem of the Doherty PA is the gain difference between the carrier and peaking amplifiers. Theoretically, at the maximum output power, the fundamental voltages and currents of the two amplifiers are the same so that the carrier and peaking amplifiers have the same load impedance and generate the same power. However, with the gain difference, the current and the voltage of the peaking amplifier are lower than those of the carrier amplifier. This difference results in a higher load for the carrier and a lower load impedance for the peaking amplifier than what is desired. Consequently, the proper Doherty operation cannot be achieved, which degrades the power, efficiency, and linearity.

Therefore, more power needs to be driven to the peaking amplifier at the maximum output power for proper operation and load modulation. This uneven power drive is further explored with different types of input dividing networks in Section III.

C. Phase Compensation Network

A phase compensation network is required at the input of Doherty PA to eliminate the phase difference caused by various elements, such as the quarter-wavelength transformer and the differently-biased transistors.

Fig. 4(a) shows a conventional input network with an additional phase compensation circuit. For BW evaluation, it is assumed that the input power is driven equally to each path and the resistance value for the each path is 4 Ω. The input capacitance of the transistors are absorbed into the broadband matching circuits. A lumped Wilkinson power divider is used, and its input impedance of 17.5 Ω is the load impedance of a pre-stage amplifier. The phase delay of -110° compensates for the quarter-wavelength transformer and the delay from the differently-biased amplifiers.

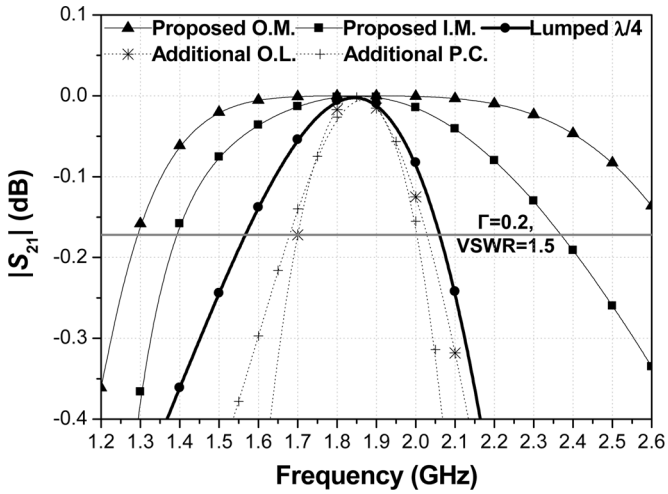

Fig. 5. Proposed BW enhancement by merging the phase compensation network and the offset line into the input and the output matching circuits (I.M. and O.M.), respectively. The conventional (additional) offset line (O.L.) and phase compensation (P.C.) circuits have even narrower BW than the lumped quarter-wavelength transformer (ITR = 3.1).

Fig. 4(b) is the proposed input matching network with a merged phase compensation circuit. The input matching circuits play the role of phase compensator. A two-section high-pass filter (HPF) with the same impedance transformation ratio is placed on the carrier amplifier path to compensate for the phase and to match the input impedances across a broad BW. The peaking amplifier employs a band-pass filter with zero delay.

The BW characteristics of the two input networks are plotted in Fig. 4(c). The input network with the additional phase circuit (Fig. 4(a)) has a narrower BW than the circuit with a merged phase circuit (Fig. 4(b)). This BW plot is compared with the lumped quarter-wavelength transformer in Fig. 5. The BW of the additional phase compensation circuit is even narrower than that of the lumped transformer, limiting the broadband operation of the Doherty PA. The proposed input network eliminates the BW limit caused by the additional phase compensation circuit.

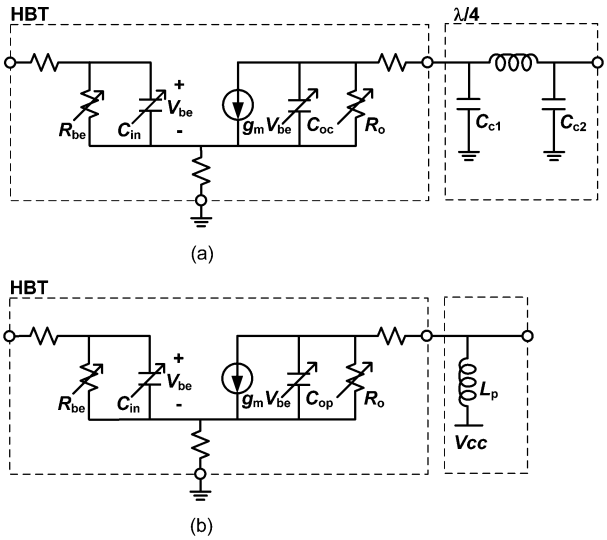

Fig. 6. Manipulation of the output capacitances without additional offset lines. (a) For the carrier amplifier. (b) For the peaking amplifier.

D. Offset Line and Output Matching

The additional offset line in the conventional Doherty PA degrades the BW since it has narrower BW than the lumped quarter-wavelength transformer as shown in Fig. 5 (Additional O.L.). The offset line is conventionally employed to compensate for the output capacitance of the transistors and to modulate the output load impedances of both amplifiers to keep them close to ideal values.

Fig. 6 illustrates how to manipulate the output capacitances of the transistors without using offset lines. The average output capacitance $(\overline{C_{oc}})$ of the carrier amplifier is merged into the quarter-wavelength transformer [Fig. 6(a)]. Thus, the capacitor of the quarter-wavelength transformer is obtained by

$$C_{c1} = C_{c2} - \overline{C_{oc}}. \tag{4}$$

Therefore, the load modulation circuit is directly attached to the current source of the transistor since the series resistance at the collector terminal is negligible. The average output capacitance $(\overline{C_{op}})$ of the peaking amplifier is resonated out by the inductance of the bias line [Fig. 6(b)]. The inductance is given by

$$L_p = \frac{1}{(2\pi f)^2 \cdot \overline{C_{op}}}. \tag{5}$$

Fig. 7 shows BW characteristics for possible Doherty output configurations using lumped elements. Fig. 7(a) employs the proposed offset line technique, but the final output matching circuit has high Q because the impedance is transformed from 4 Ω to 50 Ω. Multiple stages for the final matching circuit can increase the BW, but loss from the lumped elements also increases, which degrades efficiency.

Fig. 7(b) increases the impedance at the combining junction by adding the output matching circuit to the peaking amplifier so that each output circuit has the same Q. In this case, the additional offset line is required due to the matching circuit in the peaking path.

Fig. 7(c) shows the proposed offset line implementation. The two-section output matching circuit has a phase of zero degrees to ensure a high impedance seen through the peaking path at the combining junction. The Q's of the carrier and the final output circuits are given by

$$\begin{aligned} Q_1 &= \sqrt{\mathrm{ITR}_1} \\ Q_3 &= \sqrt{\mathrm{ITR}_3 - 1} \\ Q_1 &= Q_3 \end{aligned} \tag{6}$$

where ITR_1 indicates the ITR of the quarter-wavelength transformer, and ITR_3 indicates the ITR of the final output matching circuit. Q_2 for the peaking output circuit is lower than Q_1 and Q_3. From the (6), Q_1 is calculated to be 1.76 and ITR_1 is 3.1.

Fig. 7(d) and (e) show the impedances for the carrier amplifier in the 6 dB back-off power region. The proposed output configuration has the widest BW because it maintains the most constant real and imaginary impedances. Fig. 7(f) and (g) depict the impedances for the carrier and the peaking amplifiers when the same power is delivered to each amplifier in a maximum output power condition. The circuit shown in Fig. 7(b) maintains more constant impedances than the circuit in Fig. 7(a) thanks to the low Q matching circuits. However, the additional offset line disturbs to keep the constant impedance, especially the imaginary part for the peaking amplifier, which results in lower BW than the circuit shown in Fig. 7(c). In a maximum output power condition, the proposed output configuration also achieves the constant impedance across the widest BW.

The enhanced BW is shown and compared with the BW of the lumped quarter-wavelength transformer in Fig. 5. The proposed circuit implementation eliminates the BW limit caused by the additional offset line.

E. IMD Cancellation

Researchers have been searching for a digital pre-distortion technique with low power consumption and a short processing time [17], but this is still a problem for commercial handset power amplifiers. Thus, the Doherty PAs need to be both linear and efficient. The Doherty PA achieves allowable linearity by canceling the inter-modulation distortions (IMDs) between the two differently-biased amplifiers. For the cancellation across a broad BW, we should maintain both the same magnitude and the out-of-phase relationship of IMDs between the carrier and the peaking PAs, which can be achieved by maintaining the consistent load impedance across the BW. The BW improvement techniques, using the same Q, and merging the phase compensation network and the offset line into the matching circuits, reduce the variation of the IMDs and the phase difference across the broad BW.

Fig. 8 shows the simulated total phase difference of the fundamental power between the carrier and the peaking amplifiers with the combination of the input and the output circuits, that are respectively shown in Figs. 4 and 7. The additional phase compensation circuit from Fig. 4(a) and the additional offset

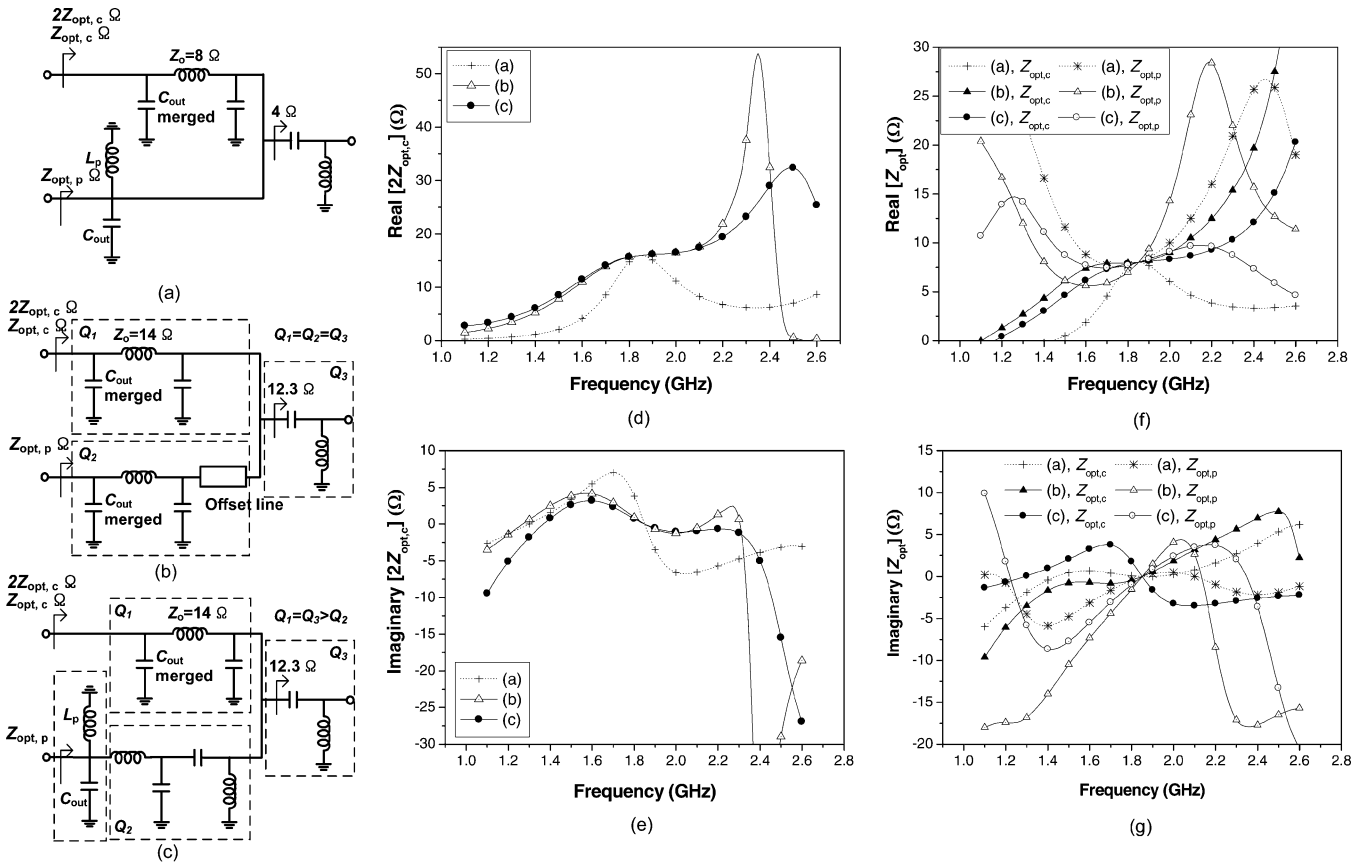

Fig. 7. Doherty output networks to deliver 8 Ω for both $Z_{\mathrm{opt},c}$ and $Z_{\mathrm{opt},p}$ at a center frequency of 1.85 GHz. (a) Different Q output matching circuit. (b) Additional offset line and the same Q output matching circuit. (c) Proposed offset line and the same Q of the quarter-wavelength transformer and the final output matching circuit. (d) Real part of $2Z_{\mathrm{opt},c}$ for the carrier amplifier when the peaking amplifier is turned off. (e) Imaginary part of $2Z_{\mathrm{opt},c}$. (f) Real part of the output impedances of $Z_{\mathrm{opt},c}$ and $Z_{\mathrm{opt},p}$ when the same power is delivered to each amplifier. (g) Imaginary part of $Z_{\mathrm{opt},c}$ and $Z_{\mathrm{opt},p}$.

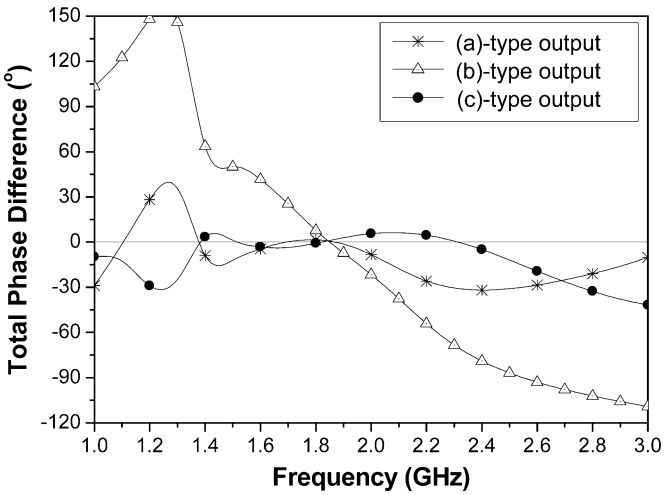

Fig. 8. Simulated total phase difference of the carrier and the peaking paths with the following combinations: Figs. 4(a)–7(a), Fig. 4(a)–7(b), and Fig. 4(b)–7(c).

line from Fig. 7(b) cause a significant phase difference that varies with the frequency. The combination of Figs. 4(b) and 7(c) maintains the phase difference within 10 degrees across the widest BW, which helps to cancel the IMDs as well as combining the fundamental output powers.

III. Input Dividing Networks for BW Enhanced Doherty PA

As explained in Section II.B, the uneven power drive, or more power to the peaking path, is necessary for the class-C biased peaking amplifier in the Doherty PA architecture. In this section, we introduce two input dividing networks and explain how they can achieve the uneven drive. The advantages and the disadvantages of each input dividing network are also discussed.

A Wilkinson power divider consists of two quarter-wavelength microstrip lines for two output ports and a resistor at the two output ports for isolation. The Wilkinson power divider is utilized in most of the Doherty designs to achieve power division and isolation. The power division ratio is determined by the input reflection coefficient of each amplifier, and is given by

$$P_{\mathrm{in},c} : P_{\mathrm{in},p} = \frac{1}{2}P_{\mathrm{in}}\left(1 - \left|\frac{Z_{\mathrm{in},c} - Z_o}{Z_{\mathrm{in},c} + Z_o}\right|^2\right) : \frac{1}{2}P_{\mathrm{in}}\left(1 - \left|\frac{Z_{\mathrm{in},p} - Z_o}{Z_{\mathrm{in},p} + Z_o}\right|^2\right) \quad (7)$$

where $P_{\mathrm{in},c}$ and $P_{\mathrm{in},p}$ are the drive power to the carrier and the peaking amplifiers, respectively. $Z_{\mathrm{in},c}$ and $Z_{\mathrm{in},p}$ are the input impedances of the carrier and the peaking amplifiers. Z_o is the

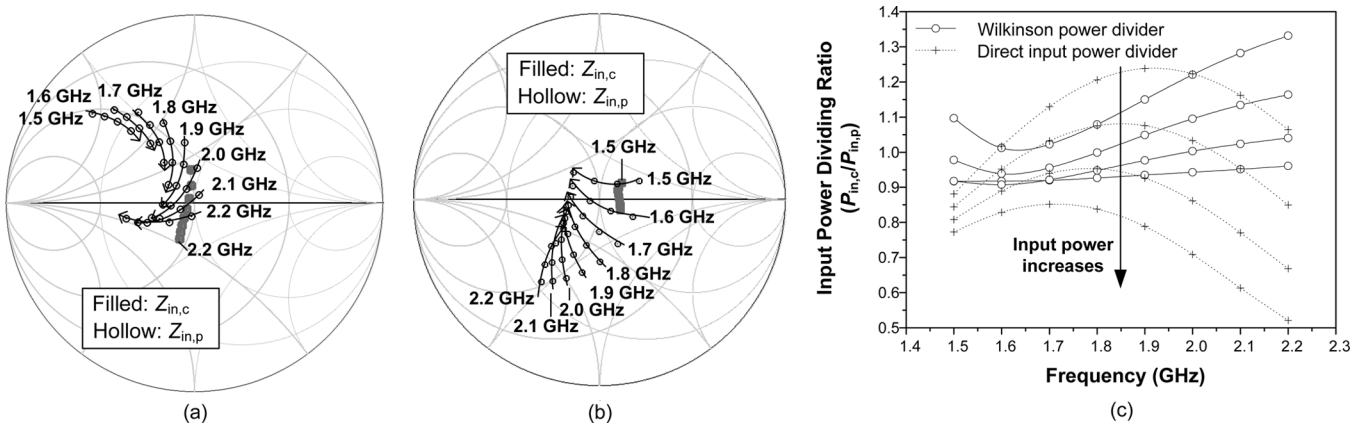

Fig. 9. (a) Input impedance traces with the direct input power divider according to the frequency and the input power. (b) Input impedance traces with the Wilkinson power divider. (c) Input power dividing ratio of the carrier to the peaking path.

output port impedance of the Wilkinson divider, and $P_{\rm in}$ is the input power at the input port of the Wilkinson divider.

Because of the large size of the Wilkinson power divider, the input paths of the carrier and the peaking amplifiers are connected directly for handset applications [16]. The power division is determined by the input impedance ratio of both amplifiers, and is given by

$$P_{{\rm in},c} : P_{{\rm in},p} = \frac{1}{2}{\rm Re}\left[\frac{|V_{\rm in}|^2}{Z^*_{{\rm in},c}}\right] : \frac{1}{2}{\rm Re}\left[\frac{|V_{\rm in}|^2}{Z^*_{{\rm in},p}}\right] \qquad (8)$$

where $V_{\rm in}$ is the voltage at the junction of the carrier and the peaking paths. The divided power ratio is proportional to the inverse ratio of the resistances, that is, the ratio of the conductances.

The purpose of the uneven drive is to help achieve the load modulation and the desired output power close to the ideal Doherty operation by compensating for the lower gain of the class-C-biased peaking amplifier. This uneven drive can be achieved by placing an attenuator on the path of the carrier amplifier [18]. However, this approach results in not only low gain but also low efficiency at low power because the peaking amplifier turns on early due to the increased power driven to the peaking path, which draws more dc currents.

Therefore, it is desirable to drive more power to the carrier at low power and more power to the peaking path at high power. More power to the carrier prevents the peaking amplifier from turning on early and improves the gain and efficiency at low power. In addition, more power to the peaking path leads to proper load modulation, desired power generation, and good linearity by IMDs cancellation. This can be accomplished by utilizing the impedance variation, caused by the class-C bias, of the peaking amplifier according to the input power level.

When using the Wilkinson power divider, the input impedance of the carrier amplifier $(Z_{{\rm in},c})$ is mismatched, and the input impedance of the peaking amplifier $(Z_{{\rm in},p})$ is matched to the port impedance at the maximum output power so that more power is driven to the peaking path. As the input power decreases, the impedance variation of the peaking amplifier causes greater mismatch with the port impedance, thereby driving more power to the carrier. Here, the reflection coefficients affect the division ratio.

For the direct power division, the conductance value of $Z_{{\rm in},c}$ is larger than that of $Z_{{\rm in},p}$ for more power to the carrier amplifier in the maximum output power condition. As the input power decreases, the conductance value of $Z_{{\rm in},p}$ becomes larger than that of $Z_{{\rm in},c}$ for more power to the peaking amplifier. Because the ratio of the conductances determines the power ratio of each path, the uneven drive is more dynamic to the power level variation but is also more vulnerable to the frequency changes compared to the Wilkinson power divider.

The input impedance traces according to the frequency and the input power with the direct input power divider and with the Wilkinson power divider are shown in Fig. 9(a) and (b). The arrows indicate the increase of the power level. $Z_{{\rm in},p}$ in Fig. 9(a) varies according to the power and follows the conductance circle. $Z_{{\rm in},p}$ in Fig. 9(b) changes from a high to a low reflection coefficient.

Fig. 9(c) shows the proportion of the input power that is sent to the carrier path versus the peaking path according to frequencies. More input power is driven to the carrier at low power and to the peaking paths at high power for both cases. In the case using the Wilkinson power divider (Fig. 9(c)), the input power division is more consistent in the high power region according to the frequency sweep so that it can take advantage of better IMD cancellation for linear operation and better load modulation for the Doherty operation. Even though the direct power divider has a narrower BW performance, it drives more dynamic uneven input power to the carrier path in the low power condition and to the peaking path in the high power region near the center frequency of 1.85 GHz, which possibly lead to higher efficiency at low power while maintaining linear operation at high power across a narrow BW.

Therefore, the input dividing networks need to be utilized considering the trade-offs among BW, size, gain, and efficiency performances. To maximize the BW performance, the Wilkinson power divider is employed in this work, even though it reduces the overall gain and the efficiency at a back-off power level.

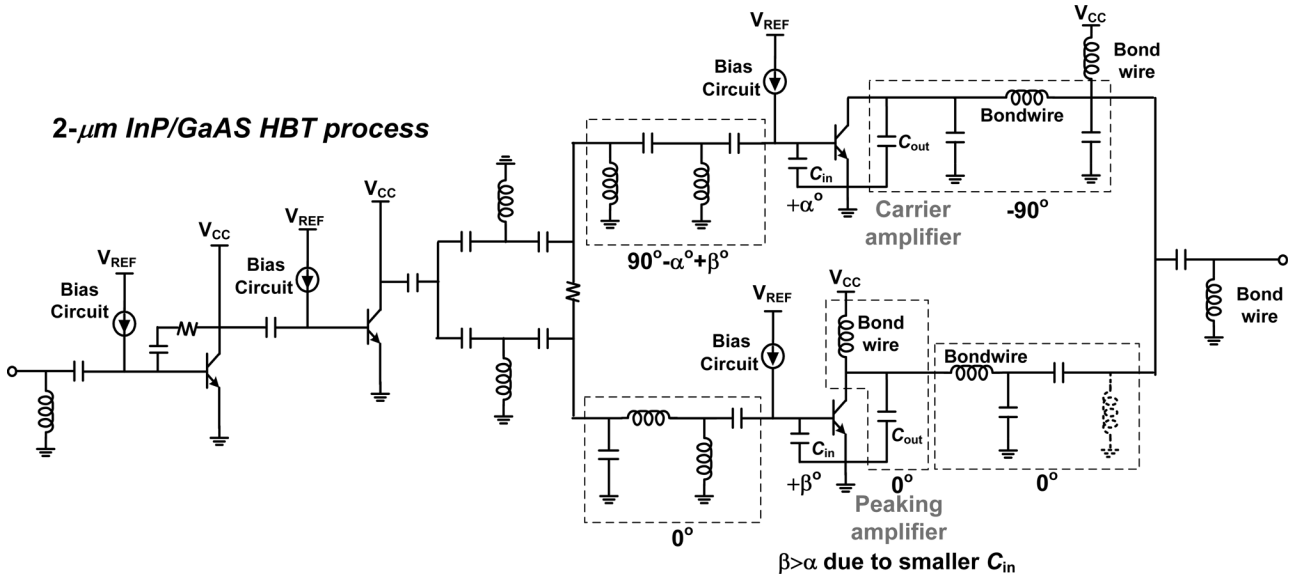

Fig. 10. Schematic of the integrated broadband Doherty PA.

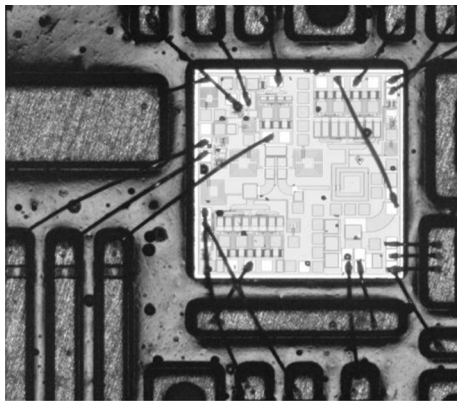

Fig. 11. A photograph of a chip. The chip size is 1.4×1.4 mm^2.

IV. Implementation and Measurement Results

The Doherty PA is implemented using an InGaP/GaAs 2-μm HBT process, and the overall circuit schematic of the PA is shown in Fig. 10. The PA is integrated into a chip with 1.4 mm $\times$ 1.4 mm as shown in Fig. 11. The inductors, which have large losses, are implemented off the chip using bondwires and slab inductors on a printed circuit board.

The transistor size of the carrier and the peaking amplifiers is the same to ensure high efficiency at 6-dB back-off output power for a 7.5-dB PAPR LTE signal, but the input matching of the carrier amplifier has a mismatch of about 1-dB to achieve the uneven drive for proper IMDs cancellation. The input impedance of the peaking amplifier is mismatched in the low power region, and it becomes matched at the maximum output power using the variation of the input capacitance. Thus, more input power is driven to the carrier and the peaking amplifiers at low and high power, respectively.

The broadband two-section matching circuits are employed for the input of the carrier and the peaking amplifiers, and the intrinsic capacitances of the amplifiers is merged into the matching circuits. An additional phase compensation network degrades the BW performance as shown in Section II, so it is eliminated. Instead, the input networks, including the matching circuits and the capacitances of the transistors, generate a phase difference of 90 degrees. The input matching circuit of the carrier amplifier compensates for the phase difference of both transistors because the smaller input capacitances of the peaking amplifier result in a larger phase degree. It is worthwhile to note that the phase difference of the differently-biased transistors causes a longer phase compensation network than 90 degree as shown in [15].

The output matching circuit after the combining point and the output matching circuits of the carrier amplifier are designed using the same Q considering a wide BW and low loss from the components. The additional offset line in the peaking path used in the conventional design is eliminated, which results in a wider BW. Instead, the shunt DC feed bond wire inductance resonates the output capacitance of the peaking amplifier, and the output matching of the peaking amplifier has a two-section circuit with a phase delay of zero degrees to maintain the broad BW and the high output impedance seen into the peaking path at the output junction.

The three-stage PA is designed for a gain of more than 28 dB. The first stage has a feedback path with a series resistor and capacitor for broadband operation. The lumped Wilkinson power divider is integrated into a die to ensure consistent power division across a wide BW, and is located at the output of the second stage, i.e., the input of the Doherty configuration. The lumped Wilkinson power divider is realized using lumped quarter-wavelength transformers with shunt inductors to minimize insertion loss and size. The Wilkinson power divider is better than the direct power divider in terms of the BW even though it reduces the overall gain and the efficiency at a back-off power level, because each path is isolated and the power division is only dependent on the reflection coefficients.

The PA is designed and measured with a supply voltage of 4.5 V, which is suitable for ET operation of the Doherty PA using a boosted supply modulator. The boosted supply modulator has advantages, such as maintaining the maximum performance at a wanted output power regardless of battery discharge and delivering higher efficiency due to small portions of the knee voltage

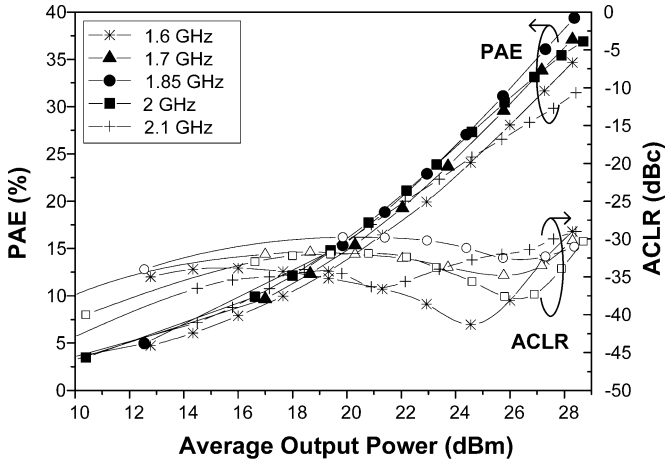

Fig. 12. Measured PAE and ACLR across 1.6–2.1 GHz with a 10-MHz BW 16-QAM 7.5 dB PAPR LTE signal according to the input power sweep.

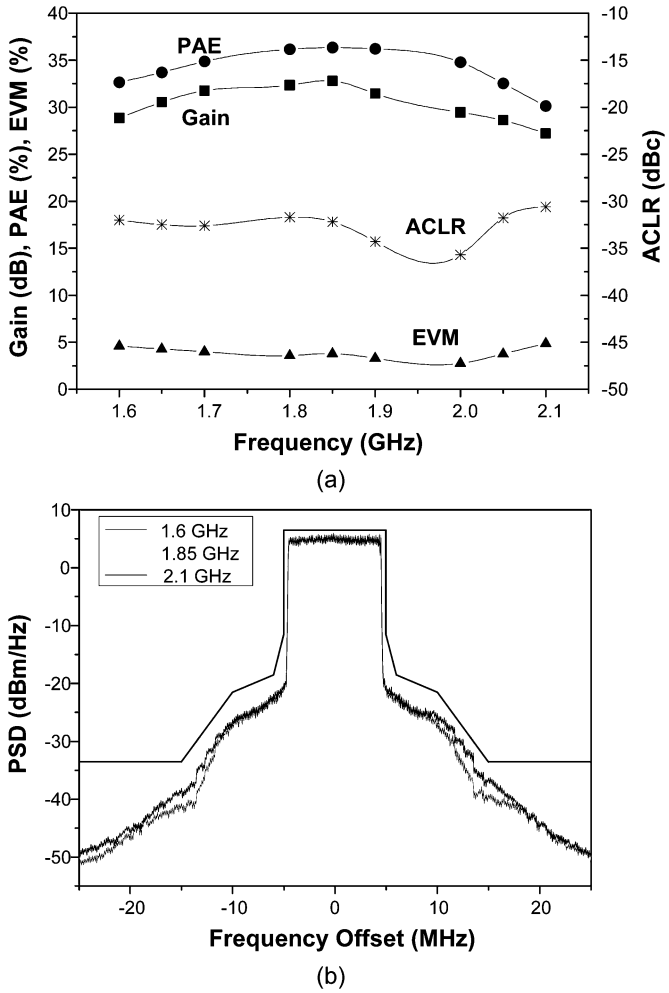

Fig. 13. (a) Measured performance of the proposed PA across 1.6–2.1 GHz at an average output power of 27.5 dBm with the LTE signal. (b) Measured spectra with the standard spectrum mask of the LTE application.

and broad bandwidth due to the low output capacitance of PAs with higher supply voltages [7].

Fig. 12 shows the measured PAE and ACLR performance across 1.6–2.1 GHz with the 10-MHz BW 16-QAM 7.5 dB PAPR LTE signal according to the input power sweep.

Fig. 13(a) shows the measured performance across 1.6–2.1 GHz with the LTE signal. The PA with a supply voltage of 4.5 V delivers a PAE of 36.3%, an EVM of 3.8% and an ACLR of -32 dBc with an average output power of 27.5 dBm at a frequency of 1.85 GHz. The ACLR performance is measured for the 9-MHz resolution BW at the center and the 10-MHz offset frequency. The PA delivers more than 30% PAE below -31-dBc ACLR and 4.8% EVM at an average output power of 27.5 dBm across 1.6–2.1 GHz. Fig. 13(b) shows the measured spectra that meet the standard spectrum mask of the LTE application.

V. Conclusion

In this paper, we have aimed to eliminate a number of factors that limit BW. We utilize the lower Q of the quarter-wavelength transformer and propose the phase compensation circuit and the additional offset line to enhance the overall BW of the Doherty PA. The output matching circuit having the same Q and the broadband input matching circuit also increases the BW. The Wilkinson power divider is selected and integrated into a chip to enhance the bandwidth of Doherty operation. For an LTE signal with a 7.5-dB PAPR and a 10-MHz BW, the PA with a supply voltage of 4.5 V delivers a PAE of 36.3% and an ACLR of -32 dBc at an average output power of 27.5 dBm and a frequency of 1.85 GHz. Across the 1.6–2.1 GHz range, the PA performs with a PAE of over 30%, a gain of over 28 dB and an ACLR of below -31 dBc at an average output power of 27.5 dBm while satisfying the standard spectrum mask. These results verify that the proposed bandwidth enhancement techniques are effective when incorporated into the design of broadband handset Doherty PAs.

Acknowledgment

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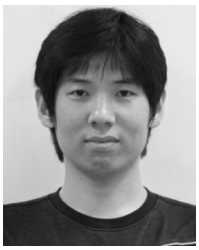

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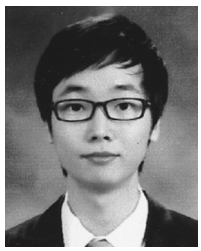

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