Optimization for Envelope Shaped Operation of Envelope Tracking Power Amplifier

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***Abstract*—This paper describes the analysis of an optimized envelope shaping function for the envelope tracking power amplifier (ET PA) and its implementation. The proposed shaping function, which is sweet spot tracking with crest factor reduction, improves the efficiency and output power of the power amplifier (PA), as well as its linearity. For an accurate simulation of the supply modulator, an equivalent model of the PA under the envelope shaping is suggested. To achieve high efficiency and wide bandwidth, the CMOS supply modulator has a hybrid structure of a switching amplifier and a linear amplifier. The fabricated ET PA delivers higher efficiency and better linearity than standalone PA for the wideband code division multiple access and long-term evolution signals.**

***Index Terms*—Crest factor reduction (CFR), envelope tracking (ET), polar transmitter, power amplifier (PA), sweet spot.**

I. Introduction

THE MOBILE handsets for current communication systems need to handle signals with wide channel bandwidth and high peak-to-average power ratio (PAPR). To provide the high data rate services, a conventional PA with a fixed supply voltage [see Fig. 1(a)] should be operated at the back-off power region. This operation linearly amplifies the high PAPR signal, but its efficiency is much lower than its peak value, as shown in Fig. 2. To improve the low efficiency at the back-off power region, many efficiency enhancement techniques at the low power are studied [1]–[19].

The envelope tracking power amplifier (ET PA) is one of the most popular efficiency enhancement techniques. To reduce dc power consumption, it modulates the supply voltage of the PA according to the output power level [see Fig. 1(b)]. As shown in Fig. 2, efficiency of the PA is increased significantly by the ET technique. Since the overall efficiency of the ET PA is proportional to the efficiency of the supply modulator and the linearity of the PA is strongly affected by the linearity of the supply modulator, optimized design of the supply modulator is very important. There are two types of modulators; a linear amplifier and a switching amplifier. In [1], [2], a low dropout (LDO) is used as the supply modulator. Although the LDO provides a large bandwidth, its efficiency is poor. In [3]–[5], a switching amplifier is used and the efficiency is much higher than the LDO. However, this structure requires a high-order passive filter and its bandwidth is too narrow to be used for wide bandwidth signals. To achieve an operation with the wide bandwidth and high efficiency, a hybrid switching amplifier that has a combined structure of the switching amplifier and the linear amplifier is used in [6]–[14].

In [12]–[17], several envelope shaping methods are suggested to improve efficiency and linearity of the ET PA. In this paper,

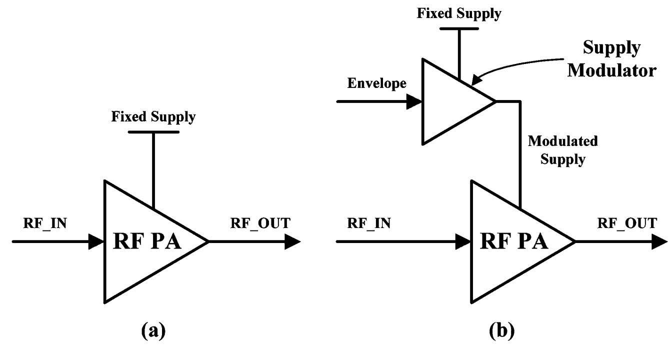

Fig. 1. (a) Conventional PA with fixed supply voltage. (b) ET PA with modulated supply voltage.

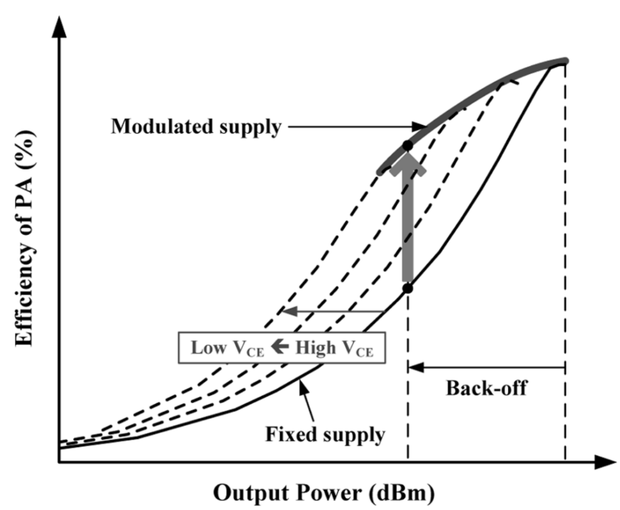

Fig. 2. Efficiency curves for conventional PA and ET PA.

Manuscript received November 06, 2010; revised March 22, 2011; accepted March 30, 2011. Date of publication May 05, 2011; date of current version July 13, 2011. This work was supported by the World Class University (WCU) Program through the National Research Foundation of Korea funded by the Ministry of Education, Science and Technology (R31-2010-000-10100-0), The Ministry of Knowledge Economy (MKE), Korea, under the Information Technology Research Center (ITRC) Support Program supervised by the National Information Technology Industry Promotion Agency (NIPA) [NIPA-2011-(C1090-1111-0011)], and the 2010 Brain Korea 21 Project.

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Digital Object Identifier 10.1109/TMTT.2011.2140124

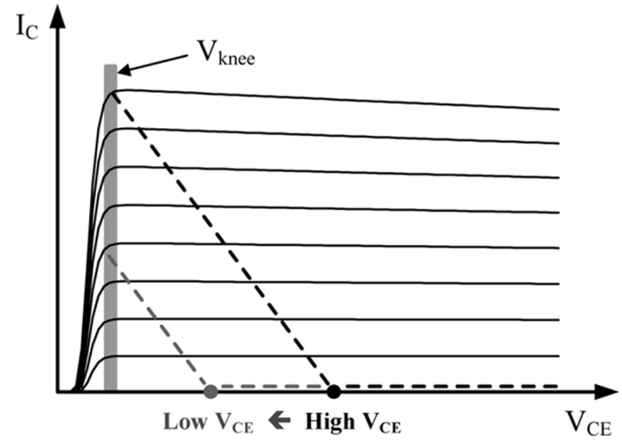


Fig. 3. Load lines of class-B biased GaAs HBT PA.

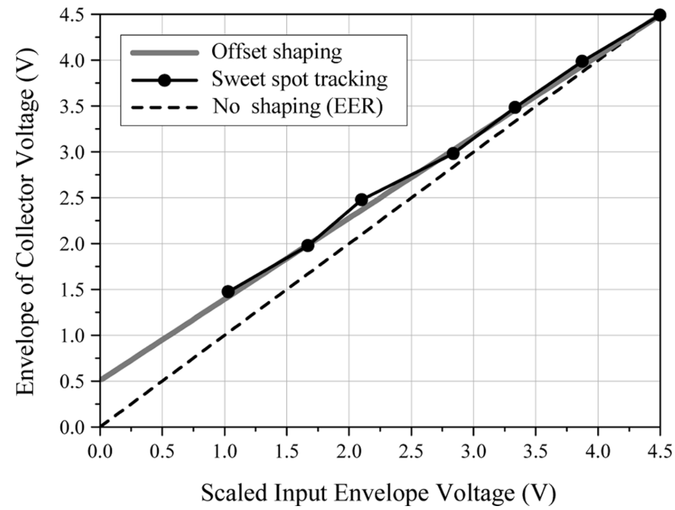


Fig. 4. Envelope shaping functions.

we propose a new envelope shaping method for higher efficiency, output power, and linearity, following the sweet spot tracking. The tracking method is analyzed and the performance of the ET PA is investigated. It is shown that the sweet spot tracking provides the best performance from the ET PA. For the optimum design of the supply modulator, an accurate model of the PA is necessary. In the previously published papers, the PA is usually modeled as a constant resistor. However, this model is inaccurate for estimating the efficiency and causes a stability problem for the supply modulator. We propose an equivalent model of the PA that considers different shaping characteristics of the voltage and current envelopes and other parasitic components such as the PA's output capacitance and a connection line between the PA and the supply modulator.

In Section II, analysis of the envelope shaping function for the optimized operation is presented. In Section III, the equivalent model of the PA is described. The design of the wideband high efficiency supply modulator is explained in Section IV. The measurement results for the wideband code division multiple access (WCDMA) and long-term evolution (LTE) signals are provided in Section V.

II. Optimum Envelope Shaping Function

To find the optimized envelope shaping function, the ET characteristic of the PA is analyzed. Fig. 3 shows the load lines of a class-B biased GaAs HBT PA, which are similar to a deep class-AB operation in the implementation. As the collector voltage decreases, the load line moves to the left with the same slope, and its voltage and current swings are reduced. Regardless of the collector voltage, the knee voltage $(V_{\rm knee})$ is almost constant for the HBT. For simple analysis, we can assume $V_{\rm knee}$ is a constant value, which is about 0.45 V with the maximum collector voltage $(V_{\rm CE.MAX})$ of 4.5 V.

A. Output Power Generation

When the envelope shaping is not adopted, the collector voltage of the PA is a scaled input envelope voltage $(V_{\rm in.env.scaled})$, which is proportional to the square root of the input power $(P_{\rm IN})$. In this case, the output voltage swing is reduced by $V_{\rm knee}$, and the output power is also decreased, accordingly. The power reduction at a low output power region is a large portion, generating a significant AM–AM distortion. To compensate this power reduction due to the $V_{\rm knee}$, a simple shaping function ($V_{\rm knee}$ offset shaping) is adopted and shown in Fig. 4. The shaped envelope of the collector voltage $(V_{\rm CE})$ can be expressed as

$$V_{\rm CE} = k \times V_{\rm in.env.scaled} + V_{\rm knee} \tag{1}$$

$$k = \frac{V_{\rm CE.MAX} - V_{\rm knee}}{V_{\rm CE.MAX}} \tag{2}$$

where k is a scaling factor for the same peak voltage. By using the $V_{\rm knee}$ offset shaping function, the output power $(P_{\rm OUT})$ of the PA is exactly proportional to the $P_{\rm IN}$

$$\begin{aligned} P_{\rm OUT} &= \frac{(V_{\rm CE} - V_{\rm knee})^2}{2 \times R_{\rm LOAD}} \\ &= \frac{k^2 \times V_{\rm in.env.scale}^2}{2 \times R_{\rm LOAD}} \propto P_{\rm IN} \end{aligned} \tag{3}$$

where $R_{\rm LOAD}$ is a load impedance of the PA, similar to that of the class-B PA. In this shaped operation, linearity is maintained and the drain efficiency is kept high.

B. Sweet Spot Tracking and Linearity Consideration

In the ET PA, linearity of the PA is dependent on the supply voltage, and Fig. 5 shows the typical third-order intermodulation distortion (IMD3) curves versus the supply voltage. As the supply voltage decreases, the minimum point of the IMD3, which is called the sweet spot, moves to lower power. The sweet spots are local minimums of IMDs and are due to the internal cancellation of the harmonic components [20]–[22]. By adjusting the supply voltage to follow the sweet spot points at each power level, the linearity of the PA can be maintained high, which, in this paper, is called a sweet spot tracking technique. The sweet spot tracking curve is derived from the PA simulation and is depicted in Fig. 4. It has a matched curve of the $V_{\rm knee}$ offset shaping proposed in [12], but its offset voltage is 0.5 V, which is a little higher than $V_{\rm knee}$ of 0.45 V, and k is about 0.89. Since the trend of the envelope shaping for the

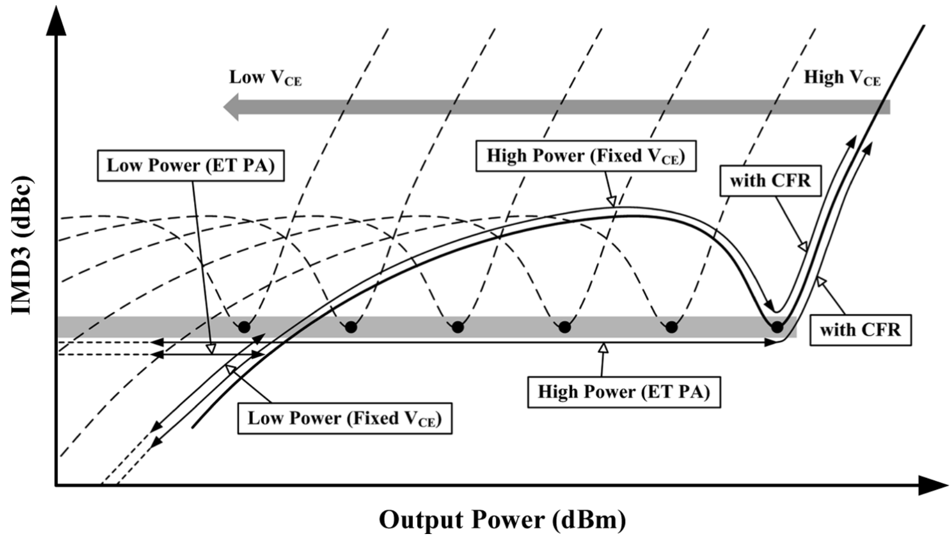


Fig. 5. IMD3 curves according to the collector voltage.

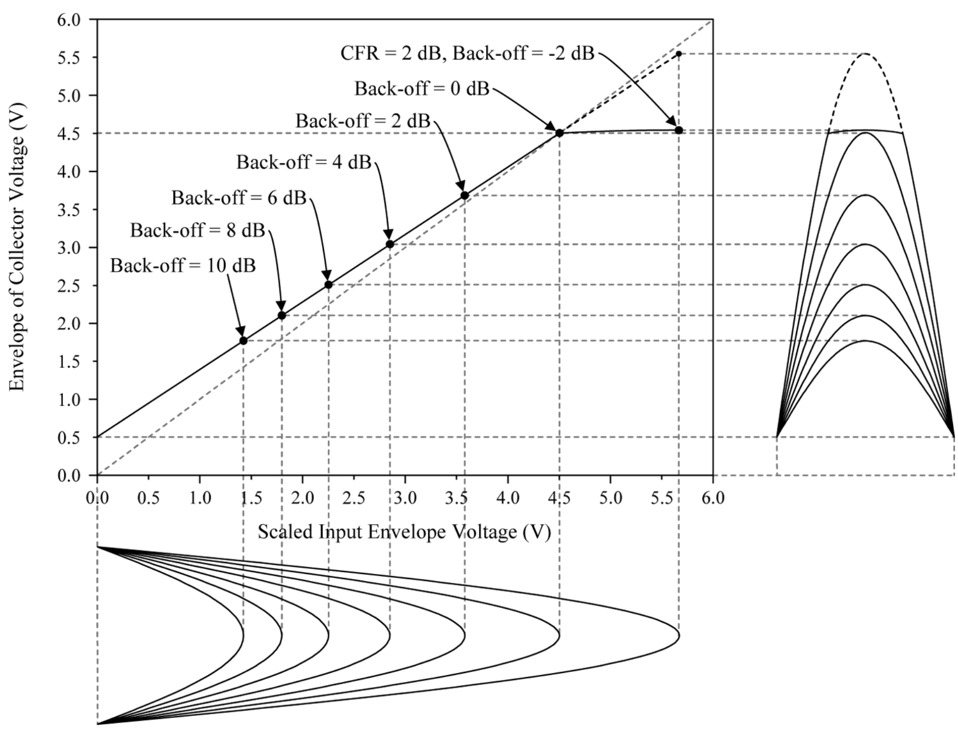


Fig. 6. Envelope shaping function for CFR and power control.

sweet spot tracking is very similar to the $V_{\rm knee}$ offset shaping, the optimum design of the tracking can be achieved by (1).

As shown in Fig. 5, the IMD3 of the ET PA with the sweet spot tracking is almost constant regardless of the output power level. On the other hand, the IMD3 of the conventional PA with a fixed supply voltage is changed according to the output power. In conclusion, the linearity of the ET PA is better than the conventional PA at the high power region. On the other hand, the linearity of the ET PA is worse than conventional PA at the low power region, but it still satisfies the system requirement with good overall linearity. Therefore, the PA can be driven to higher power, improving the power performance.

The envelope shaping has additional advantages. At a low supply voltage, PA has severe nonlinear characteristics, such as AM–AM and AM–PM distortions because of the $V_{\rm knee}$ effect with a nonlinear capacitance [19]. These nonlinear distortions are reduced by this envelope shaping. By adopting the offset shaping function with the sweet spot tracking, the ET PA can deliver the high efficiency and good linearity at the same time.

C. Crest Factor Reduction (CFR) and Power Control

CFR is a technique to reduce the PAPR, leading to efficiency enhancement of the PA [23], [24]. In the polar domain, it clips the signal with a magnitude larger than a certain threshold

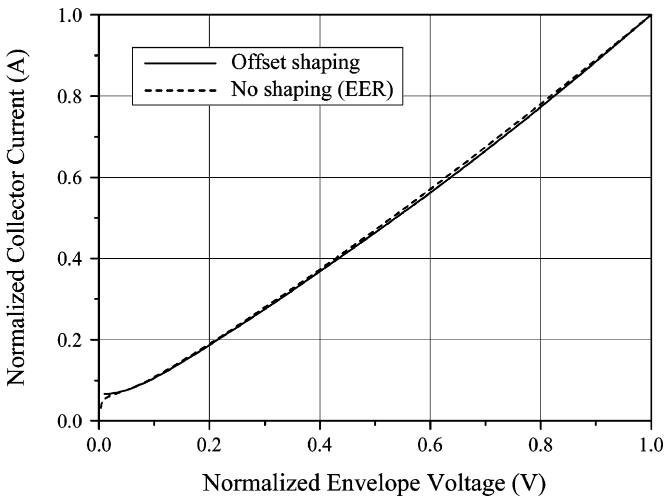


Fig. 7. Simulated collector current of class-AB biased PA with and without envelope shaping.

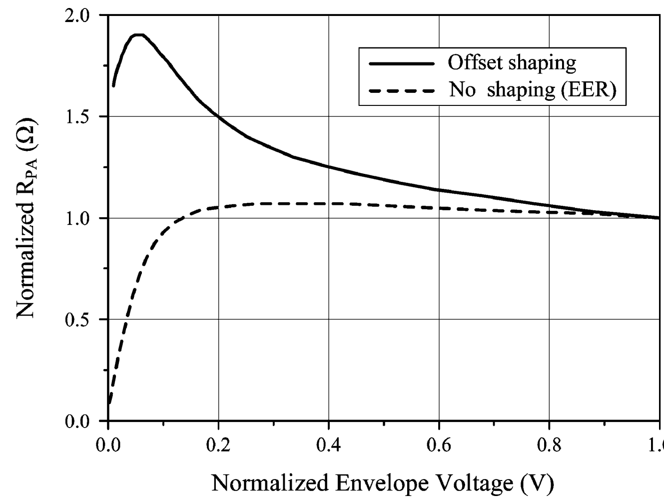


Fig. 8. Simulated equivalent load resistance of the PA with and without envelope shaping.

value while maintaining the phase information. The clipped signal has lower PAPR with little distortion. Generally, CFR is realized by digital signal processing (DSP). For a simple implementation without DSP, it can be realized by an output power compression through a higher input power driving. As shown in Fig. 6, the maximum voltage of the V_{CE} is determined by the output voltage limitation of the supply modulator. However, the input is still increased, automatically generating the proper CFR. In this way, the output power and efficiency of the PA are increased with little linearity degradation. For the back-off output power region, they trace the same envelope shaping function with smaller magnitude and maintain the sweet spot tracking.

III. Modeling of PA

In this section, we model the PA suitable to design the supply modulator and analyze operation of the ET PA under the proposed envelope shaping. Although V_{CE} of the PA is shaped, the collector current of the class-B biased PA is not shaped. The magnitude of the current is proportional to the square root of the output power. On the other hand, V_{CE} is not proportional to the square root of the output power, as presented by (1). For implementation, a class-AB biased PA is used because it shows better linearity than class B with high efficiency, and its current is very similar to the class-B case. As shown in Fig. 7, the change of the collector current by the envelope shaping is very small and can be ignored. Since the voltage and current shapings are different, the PA cannot be modeled as a constant resistor. Using the voltage shaping (Fig. 4) and the current shaping (Fig. 7), the equivalent load resistance (R_{PA}) representing the PA is calculated and depicted in Fig. 8. If the shaping is not adopted, R_{PA} changes little, except at the very low voltage region. For the offset shaping with the sweet spot tracking, R_{PA} increases up to 1.8 times from the R_{PA} at the peak output power, and this value is determined by the offset voltage and bias current of the PA.

The PA, which is a load for the supply modulator, can be modeled as Fig. 9. The variable R_{PA} can be replaced by

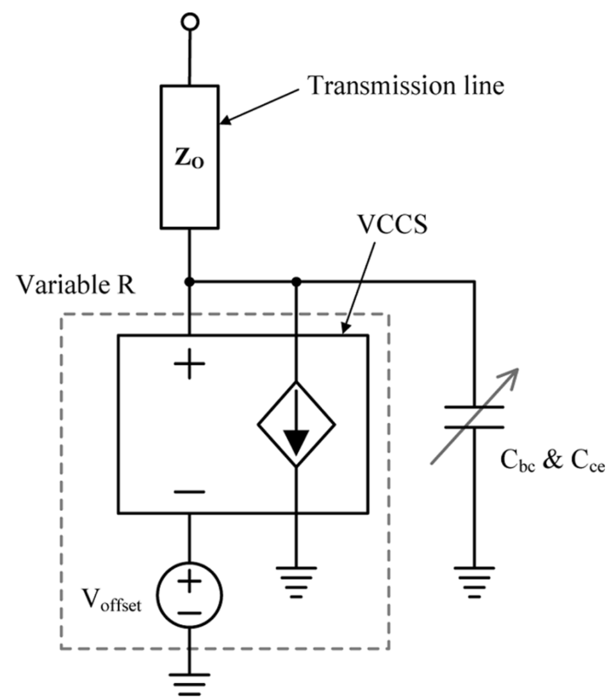


Fig. 9. Equivalent model of the PA for the envelope shaping.

a voltage-controlled current source (VCCS) with an offset voltage. A variable capacitor is added to represent the output capacitance of the HBT. For simple analysis, this variable capacitor can be regarded as a constant capacitor because the capacitance value changes a little in the offset shaping. The transmission line stands for the connection line between the PA and the supply modulator.

This PA model offers more accurate and realistic results for the simulation of the supply modulator than a constant resistor model. At the low supply voltage, the increased R_{PA} enhances the loop gain of the linear amplifier, and the increased nonlinear capacitance leads to a phase lagging. Besides, the transmission line also affects the phase response. By these effects, the phase margin (PM) of the linear amplifier is decreased and

TABLE I
MODULATED SIGNALS'S PAPR AND EFFICIENCY OF THE SUPPLY MODULATOR ACCORDING TO THE PA MODEL. ($V_{\mathrm{CE.MAX}} = 4.5$ V, $V_{\mathrm{offset}} = 0.5$ V)

		WCDMA		LTE	
		PAPR (dB)	Efficiency (%)	PAPR (dB)	Efficiency (%)
Input Envelope		3.28	-	7.44	-
Output Envelope	Constant Resistor Model	2.87	86.4	6.25	76.2
	Proposed PA Model based on class-B PA	3.12	85.6	7.21	73.3

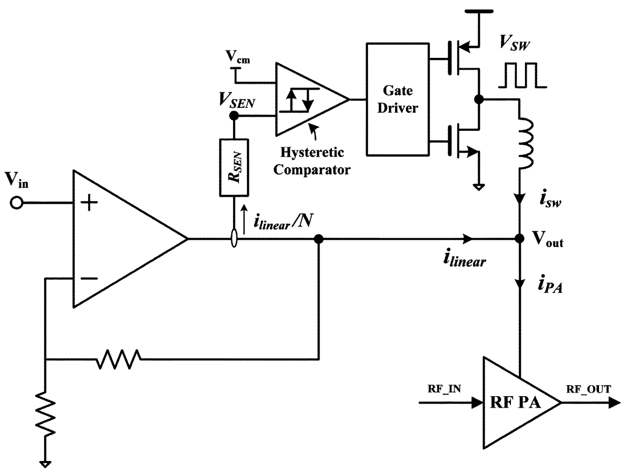


Fig. 10. Schematic of hybrid switching supply modulator.

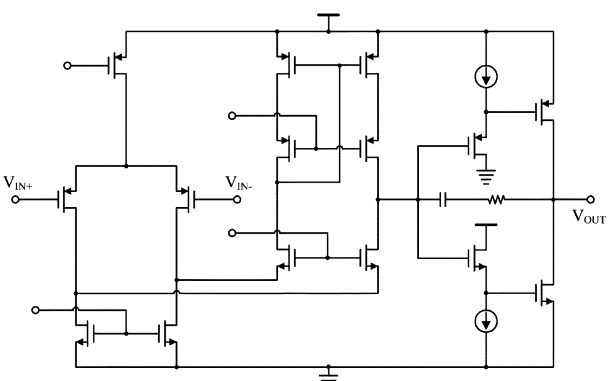


Fig. 11. Schematic of linear amplifier.

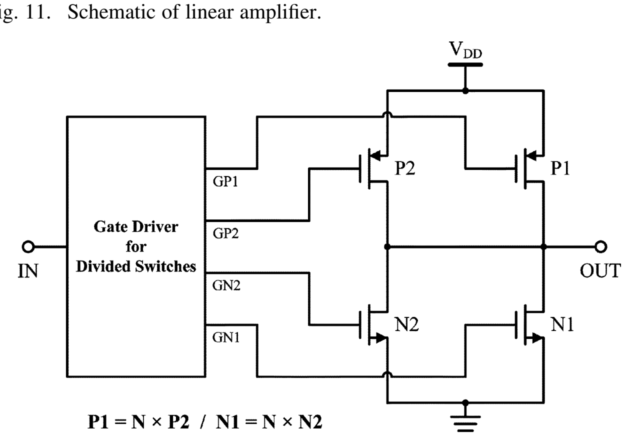


Fig. 12. Schematic of switching amplifier.

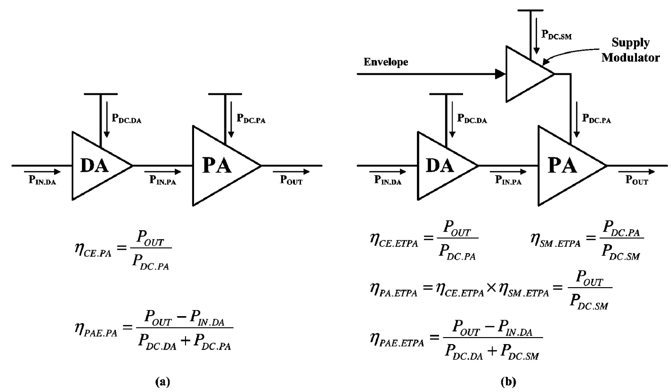


Fig. 13. Schematics and efficiency equations for: (a) standalone PA and (b) ET PA.

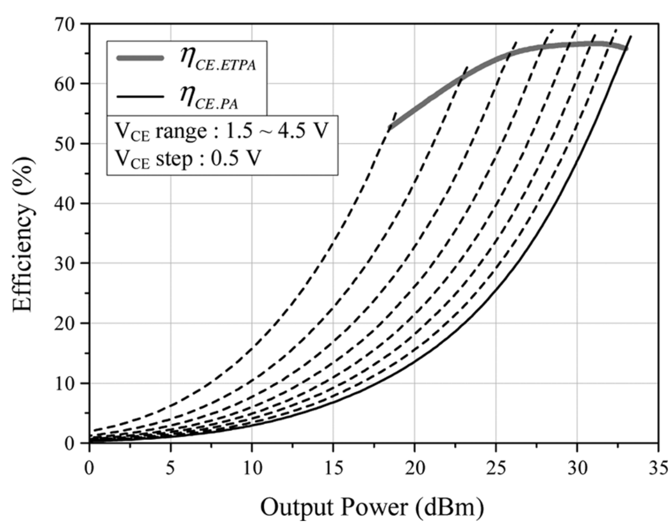


Fig. 14. Measured collector efficiency curves of ET PA and standalone PA.

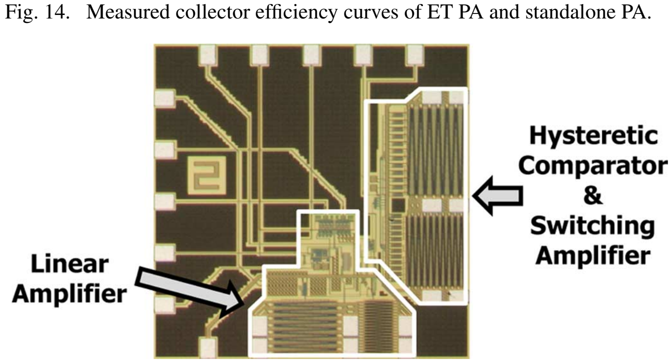


Fig. 15. Fabricated chip photograph of the supply modulator.

its stability is degraded. Since the operating frequencies of the PA and the supply modulator are quite different, the simultaneous simulation of these two circuits provides problems, such as convergence errors and extremely long simulation time. For the efficiency estimation of the supply modulator, this simple PA model could be used. As shown in Table I, the efficiency

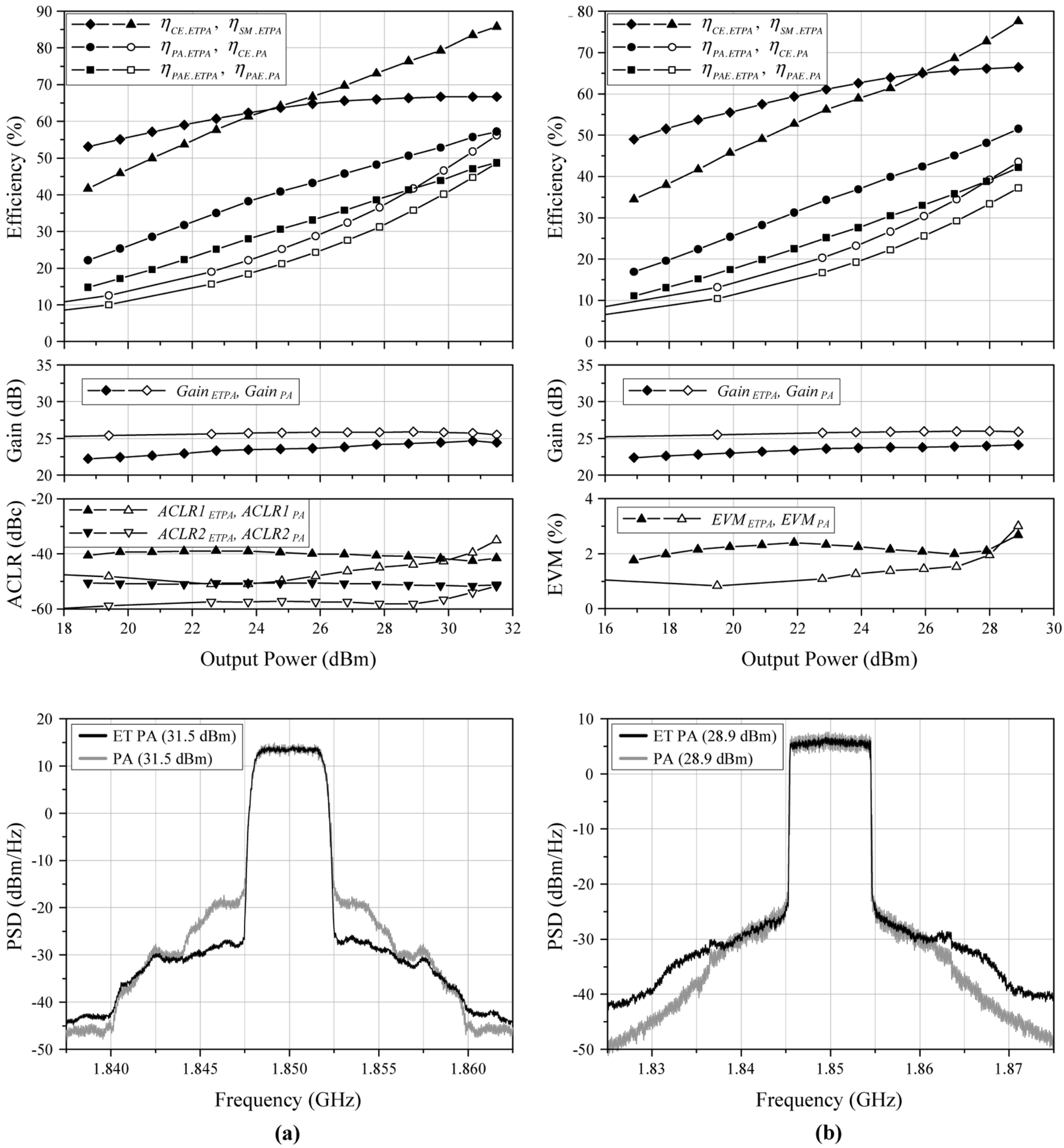


Fig. 16. Measured performances of ET PA and standalone PA for: (a) WCDMA and (b) LTE.

calculated from the constant resistor model delivers an overestimated value because the collector current is shaped according to $V_{\rm CE}$ and the PAPR is decreased too much. The proposed PA model, which considers the change of the $R_{\rm PA}$, offers more accurate efficiency estimation, close to the real operation.

IV. Design of Supply Modulator

The hybrid switching supply modulator consists of a wideband linear amplifier and a high-efficiency low-speed switching amplifier, as shown in Fig. 10. Usually the switching amplifier supplies the low-frequency component of the envelope signal with high efficiency and the linear amplifier provides the other high-frequency component with high speed. Since most of the power of the envelope signal is located at the low frequency, this structure is suitable for the high-efficiency and wideband operation.

The wideband linear amplifier operates as a voltage-controlled voltage source (VCVS). It means the output voltage of the linear amplifier is the same as its input voltage due to its high gain, wide bandwidth, and negative feedback loop. As shown in Fig. 11, we use a folded-cascode OTA as a gain stage to achieve a large bandwidth and a high dc gain. For a large

TABLE II
PERFORMANCE SUMMARY OF ET PA AND STANDALONE PA FOR WCDMA AND LTE SIGNALS AT THE PEAK AND BACK-OFF P_{OUT}

Signal	**WCDMA**				**LTE**			
	3.84 MHz / 3.28 dB / QPSK				**10 MHz / 7.44 dB / 16QAM**			
Type of PA	ET PA		Stand-alone PA		ET PA		Stand-alone PA	
P_{OUT} (dBm)	31.5	22.75	31.5	22.6	28.9	22.9	28.9	22.78
$\eta_{PAE.ETPA}$ or $\eta_{PAE.PA}$ (%)	48.8	25.2	48.6	15.7	42.2	25.2	37.2	16.7
$\eta_{PA.ETPA}$ or $\eta_{CE.PA}$ (%)	57.2	35.0	56.2	19.0	51.5	34.3	43.5	20.3
Estimated $\eta_{CE.ETPA}$ (%)	66.7	60.7	-	-	66.4	61.1	-	-
Estimated $\eta_{SM.ETPA}$ (%)	85.8	57.7	-	-	77.5	56.1	-	-
ACLR1 / ACLR2 (dBc)	–41.6/–51.2	–38.9/–50.9	–35.1/–51.7	–51.0/–57.4	-	-	-	-
EVM (%)	-	-	-	-	2.69	2.34	3.01	1.09

current driving capability and a rail-to-rail operation, the output buffer has a common source configuration, and it is biased as a class-AB for linearity and efficiency.

The switching amplifier operates as a dependent current source. It senses the direction of the linear amplifier's current flow and controls the power switches using a hysteretic comparator. Generally, the average switching frequency is dependent on the hysteresis width, inductor value, and some other parameters for a narrowband signal. For a wideband signal, the average switching frequency is mainly determined by its bandwidth. The sizes of the power switches are determined by considering the conduction loss and switching loss at the specific load resistance, switching frequency, and duty ratio. For the protection, high efficiency, and low switching noise of the switches, antishoot-through circuit, and divided switches with current control technique are employed (Fig. 12) [25]. A gate driver for the divided switches turns on/off the four switches with a little delay. It can be designed easily using four MUXs and inverter chains [13].

V. MEASUREMENT RESULTS

For comparison, a standalone PA and an ET PA are implemented, as shown in Fig. 13. The designed class-AB PA is fabricated using an InGaP/GaAs 2-μm HBT process [26]. Its operating frequency is 1.85 GHz and it has a two-stage configuration for high gain. As shown in Fig. 14, collector efficiency of the standalone PA ($\eta_{\mathrm{CE.PA}}$) and collector efficiency of the ET PA ($\eta_{\mathrm{CE.ETPA}}$) are similar at the peak output power of 33 dBm. As the output power is decreased, $\eta_{\mathrm{CE.PA}}$ is decreased significantly, while $\eta_{\mathrm{CE.ETPA}}$ is maintained high. For example, $\eta_{\mathrm{CE.PA}}$ is 20.0% and $\eta_{\mathrm{CE.ETPA}}$ is 61.5% at output power of 23 dBm. The designed supply modulator is fabricated using a 0.18-μm CMOS process and it uses thick oxide I/O devices for a high-voltage operation. A chip photograph is shown in Fig. 15 and its size is 1.4 mm $\times$ 1.4 mm. The supply voltage for the supply modulator is 5 V and the output voltage range is from 0.5 to 4.5 V. The linear amplifier has over 50-MHz bandwidth and over 50-dB dc gain. The average switching frequency of the switching amplifier is varied from 2 to 6 MHz according to the bandwidth of the input signal.

Fig. 16 shows the measured performances of the ET PA and the standalone PA. For the WCDMA signal [see Fig. 16(a)], the ET PA/standalone PA have the efficiencies of 48.8/48.6% at the output power of 31.5 dBm. ACLR1, ACLR2 and spectra of the ET PA are better than the standalone PA at the peak output power. For the LTE signal [see Fig. 16(b)], the ET PA/standalone PA have the efficiencies of 42.2/37.2% at the output power of 28.9 dBm. Although the out-of-band spectra of the ET PA is worse than the standalone PA, the ET PA's error vector magnitude (EVM) performance is better than the standalone PA. For the WCDMA/LTE signals, CFRs of 0.75/2 dB (voltage clippings of 0.36/1.04 V) are employed to the ET PA and the values are experimentally determined. By the envelope tracking technique, the peak efficiency is increased by 5% for the LTE signal, while the peak efficiency is similar for the WCDMA signal because of its low PAPR. As the output power is decreased, the efficiency of the ET PA is enhanced significantly. The envelope tracking technique is meaningful for a large PAPR signal or back-off power region. Table II summarizes overall performances of the two PAs at the peak output power and back-off output power, about 23 dBm.

VI. CONCLUSION

A wideband ET PA has been implemented using a 0.18-μm CMOS supply modulator and 1.85-GHz class-AB HBT PA. It delivers high efficiency and good linearity due to the proposed optimum envelope shaping. The optimum shaping function follows the sweet spot tracking, which has an offset voltage of 0.5 V, slightly larger than V_{knee} of 0.45 V. The linearity, output power capability, and efficiency are all improved by the tracking. A proposed PA model for the tracking is composed of a variable resistor, variable capacitor and transmission line. It offers more accurate simulation results than a simple constant resistor model. For the WCDMA/LTE signals, the fabricated ET PA shows the efficiencies of 48.8/42.2% at the peak output power of 31.5/28.9 dBm, respectively.

REFERENCES

[1] P. Reynaert and M. S. J. Steyaert, "A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2598–2608, Dec. 2005.

[2] J. S. Walling, S. S. Taylor, and D. J. Allstot, "A class-G supply modulator and class-E PA in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2339–2347, Sep. 2009.

[3] G. Hanington, P. Chen, P. M. Asbeck, and L. E. Larson, "High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 8, pp. 1471–1476, Aug. 1999.

[4] B. Sahu and G. A. Rincón-Mora, "A high-efficiency linear RF power amplifier with a power-tracking dynamically adaptive buck-boost supply," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 1, pp. 112–120, Jan. 2004.

[5] V. Pinon, F. Hasbani, A. Giry, D. Pache, and C. Garnier, "A single-chip WCDMA envelope reconstruction LDMOS PA with 130 MHz switched-mode power supply," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2008, pp. 564–565.

[6] J. Kitchen, W. Chu, I. Deligoz, S. Kiaei, and B. Bakkaloglu, "Combined linear and Δ-modulated switched-mode PA supply modulator for polar transmitters," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2007, pp. 82–83.

[7] F. Wang, A. H. Yang, D. F. Kimball, L. E. Larson, and P. M. Asbeck, "Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 4, pp. 1244–1255, Apr. 2005.

[8] F. Wang, D. F. Kimball, D. Y. Lie, P. M. Asbeck, and L. E. Larson, "A monolithic high-efficiency 2.4-GHz 20-dBm SiGe BiCMOS envelope-tracking OFDM power amplifier," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1271–1281, Jun. 2007.

[9] T. Kwak, M. Lee, and G. Cho, "A 2 W CMOS hybrid switching amplitude modulator for EDGE polar transmitters," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2666–2676, Dec. 2007.

[10] W. Chu, B. Bakkaloglu, and S. Kiaei, "A 10 MHz-bandwidth 2 mV-ripple PA-supply regulator for CDMA transmitters," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2008, pp. 448–449.

[11] J. Choi, D. Kim, D. Kang, J. Park, B. Jin, and B. Kim, "Envelope tracking power amplifier robust to battery depletion," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Anaheim, CA, May 2010, pp. 1074–1077.

[12] J. Choi, D. Kim, D. Kang, and B. Kim, "A polar transmitter with CMOS programmable hysteretic-controlled hybrid switching supply modulator for multistandard applications," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 7, pp. 1675–1686, Jul. 2009.

[13] D. Kim, J. Choi, D. Kang, and B. Kim, "High efficiency and wide-band envelope tracking power amplifier with sweet spot tracking," in *IEEE Radio Freq. Integr. Circuits Symp.*, Anaheim, CA, May 2010, pp. 255–258.

[14] I. Kim, J. Kim, J. Moon, and B. Kim, "Optimized envelope shaping for hybrid EER transmitter of mobile WiMAX," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 5, pp. 335–337, May 2009.

[15] J. Hoversten and Z. Popović, "Envelope tracking transmitter system analysis method," in *IEEE Radio Wireless Symp.*, New Orleans, LA, Jan. 2010, pp. 180–183.

[16] J. Jeong, D. F. Kimball, M. Kwak, C. Hsia, P. Draxler, and P. M. Asbeck, "Wideband envelope tracking power amplifier with reduced bandwidth power supply waveform," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Boston, MA, Jun. 2009, pp. 1381–1384.

[17] J. Jeong, D. F. Kimball, M. Kwak, P. Draxler, and P. M. Asbeck, "Envelope tracking power amplifiers with reduced peak-to-average power ratio RF input signals," in *IEEE Radio Wireless Symp.*, New Orleans, LA, Jan. 2010, pp. 112–115.

[18] F. H. Raab, "Intermodulation distortion in Kahn-technique transmitters," *IEEE Trans. Microw. Theory Tech.*, vol. 44, no. 12, pp. 2273–2278, Dec. 1996.

[19] J. C. Pedro, J. A. Garcia, and P. M. Cabral, "Nonlinear distortion analysis of polar transmitters," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 12, pp. 2757–2765, Dec. 2007.

[20] N. B. Carvalho and J. C. Pedro, "Large- and small-signal IMD behavior of microwave power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 12, pp. 2364–2374, Dec. 1999.

[21] C. Fager, J. C. Pedro, N. B. Carvalho, H. Zirath, F. Fortes, and M. J. Rosário, "A comprehensive analysis of IMD behavior in RF CMOS power amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 24–34, Jan. 2004.

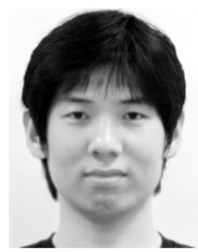
[22] E. Malaver, J. A. García, A. Tazón, and A. Mediavilla, "Characterizing the linearity sweet-spot evolution in FET devices," in *Proc. 11th GaAs Symp.*, Munich, Germany, Oct. 2003, pp. 361–364.

[23] R. Sperlich, Y. Park, G. Copeland, and J. S. Kenney, "Power amplifier linearization with digital pre-distortion and crest factor reduction," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Fort Worth, TX, Jun. 2004, pp. 669–672.

[24] O. Degani, F. Cossoy, S. Shahaf, E. Cohen, V. Kravtsov, O. Sendik, D. Chowdhury, C. D. Hull, and S. Ravid, "A 90-nm CMOS power amplifier for 802.16e (WiMAX) applications," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 5, pp. 1431–1437, May 2010.

[25] S. Sakiyama, J. Kajiwara, M. Kinoshita, K. Satomi, K. Ohtani, and A. Matsuzawa, "An on-chip high-efficiency and low-noise DC/DC converter using divided switches with current control technique," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 1999, pp. 156–157.

[26] D. Kang, D. Yu, K. Min, K. Han, J. Choi, D. Kim, B. Jin, M. Jun, and B. Kim, "A highly efficient and linear class-AB/F power amplifier for multimode operation," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 1, pp. 77–87, Jan. 2008.



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