A New Power Management IC Architecture for Envelope Tracking Power Amplifier

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Abstract—A new supply modulator architecture for robust performance against the battery voltage variation is presented. The resulting modulator is an optimized power management integrated circuit (PMIC) for an envelope tracking (ET) power amplifier (PA). The basic topology of the PMIC is based on a hybrid switching amplifier combining a wideband class-AB buffered linear amplifier and a highly efficient switching-mode buck converter in a master–slave configuration. The additional boost converter regulates the supply voltage of the linear amplifier, while the supply of the buck converter is directly coupled to the battery. The proposed supply modulator achieves max/min efficiencies of 76.8/69.3% over the entire battery voltage range. The ET PA is operated at 4.5 V, providing higher output power, efficiency, and gain than at nominal 3.5-V design. The robust performance of the proposed PMIC is demonstrated.

Index Terms—CMOS analog integrated circuits, DC–DC power conversion, envelope tracking (ET), power amplifiers (PAs), 3GPP LTE, transmitters, wireless communication.

I. INTRODUCTION

A S VARIOUS functions of the multiple portable devices are merged into a single handset, longtime usage of the battery is getting very important. The power amplifier (PA) is the most power-consuming component in the handset so there have been many efforts to improve efficiency of the PA [1]–[16]. In a handset, the PA is directly coupled to the battery and delivers the required RF output power to the antenna, as shown in Fig. 1(a). Although the previous research has resulted in excellent efficiency of the PA, most of them are optimized for the operation at the minimum battery voltage level. Fig. 2 shows the voltage characteristic of an Li-Ion battery. When it is fully charged, the battery voltage is nearly 4.2 V, but as it is discharged, the voltage drops to 3.5 V and the voltage drops very fast thereafter. Since the PA
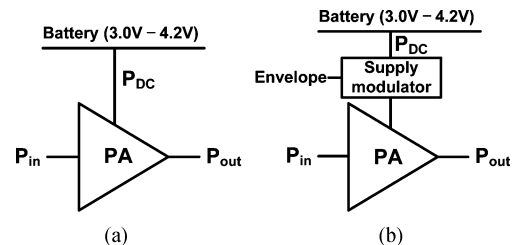

Fig. 1. Block diagram of the: (a) general PA and (b) ET PA.

should transmit the required output power ($P_{\text{out,min}}$) at any circumstance, it should be designed for the worst case, the minimum battery level ($V_{DD,\text{min}}$) of 3.5 V. For higher levels, it transmits the output power higher than the minimum requirement.

In the envelope tracking (ET) PA, the supply modulator, directly coupled to the battery, regulates output power of the PA, as shown in Fig. 1(b). Therefore, the modulator should be designed and optimized at $V_{DD,\text{min}}$. For the operating battery voltage higher than $V_{DD,\text{min}}$, the supply modulator still presents the same output voltage to the PA. This can be an inherent advantage of ET PA to transmit the constant output power regardless of the operating battery voltage. However, the supply voltage to the PA cannot be higher than the battery voltage, and the supply modulator cannot maintain the high efficiency over the entire battery voltage range. In [1] and [2], the low dropout (LDO) regulator is employed as a supply modulator. It operates over a wide bandwidth (BW), but efficiency of the LDO is not high for a high peak-to-average ratio (PAPR) signal. In the LDO, the feedback loop consisting of the pMOS and the operational transconductance amplifier (OTA) keeps the output voltage constant whatever the battery voltage is. As there is a dropout voltage across the PMOS, the maximum output voltage of the LDO is limited to 3 V by the $V_{DD,\text{min}}$. For the battery voltage higher than $V_{DD,\text{min}}$, the dropout voltage across the pMOS transistor is then increased to constantly keep the output voltage and load current. As a result, the efficiency of the LDO is degraded since it is inversely proportional to V_{DD}. The switching mode power supply, such as buck or boost converters, can present high efficiency over the wide battery voltage range, but their switching frequencies are limited by the switching loss so that wide BW capability cannot be fulfilled [3]–[6].

In this paper, we present a new supply modulator architecture enabling a high efficiency over the entire battery voltage range [7], resulting in the optimized power management integrated circuit (PMIC) for an ET PA. By boosting up the battery voltage to 5 V and employing the hybrid switching architecture, the high efficiency over the entire battery voltage range
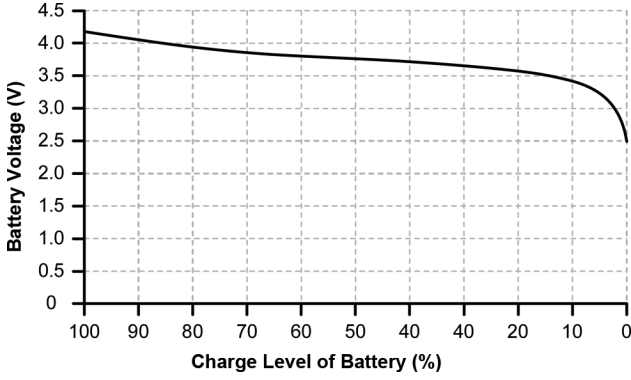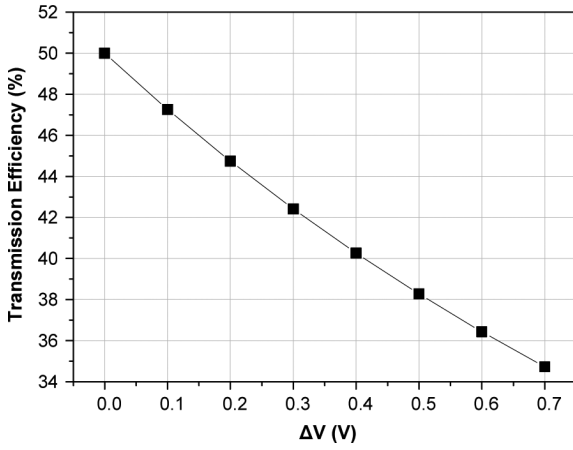
Fig. 2. Discharge curve of Li-Ion battery [17].

Fig. 3. *Real* transmission efficiency of the PA according to the operating battery voltage level, where ΔV is the difference between the operating battery voltage (V_{DD}) and the minimum battery voltage $(V_{DD,\min})$.

is achieved. The fabricated ET PA with the proposed supply modulator presents the max/min power-added efficiencies of 32.3/29.1% for the 10-MHz BW 3GPP LTE standard (at LTE band VII, 2.5–2.57 GHz) along the battery voltage range from 4.2 to 3 V. Section II covers the design of the supply at the practical situation with the battery. Section III presents the concept and circuit implementation of the proposed PMIC architecture. The measurement results are presented in Section IV.

II. Effect of Battery Voltage Variation by Discharging

A. Impact on PA Efficiency

When the load resistance of a PA is fixed, the output power (P_{out}) is proportional to a square of the supply voltage of the PA (V_{DD}) or the battery voltage. It can be expressed as follows:

$$P_{\text{out}} \propto V_{DD}^2 \tag{1}$$
$$P_{\text{out}} = k \cdot V_{DD}^2. \tag{2}$$

The required output power at $V_{DD,\min}$ can then be expressed as follows:

$$P_{\text{out,min}} = k \cdot V_{DD,\min}^2 \tag{3}$$

and the output power of the PA at the battery voltage (V_{DD}) higher than the minimum battery voltage $(V_{DD,\min})$ can be expressed as follows:

$$\begin{aligned} P_{\text{out}} &= k \cdot (\Delta V + V_{DD,\min})^2 \\ &= k \cdot V_{DD,\min}^2 + 2k \cdot \Delta V \cdot V_{DD,\min} + k \cdot \Delta V^2 \\ &= P_{\text{out,min}} + k \cdot \Delta V (2V_{DD,\min} + \Delta V) \end{aligned} \tag{4}$$

where ΔV is the difference between the operating battery voltage and the minimum battery voltage. That is, as the PA is designed for the minimum battery voltage level, while the battery voltage is always higher than the minimum level, there is an unnecessary power generation from the PA. As a result, the *real* transmission efficiency, which can be defined as a ratio of the required output power $(P_{\text{out,min}})$ to the dc power consumption $(P_{\text{out}}/\eta_{\text{PA}})$, is reduced over most of the battery voltage range. For example, when $P_{\text{out,min}}$ is 2 W and $V_{DD,\min}$ is 3.5 V, then k is about 0.163. Assuming the average operating battery voltage is around 3.85 V, the average ΔV is around 0.35 V. The average output power level is as follows:

$$P_{\text{out,avg}} = P_{\text{out,min}} + k \cdot \Delta V_{\text{avg}} (2V_{DD,\min} + \Delta V_{\text{avg}}). \tag{5}$$

If the efficiency of the PA (η_{PA}) is 50%, the dc power consumption at $V_{DD,\min}$ is 4 W. However, at the average battery voltage, the output power level is 2.42 W and the dc power consumption is 4.84 W with the assumption of the same efficiency of 50%. Considering the required output power level of the PA is 2 W, regardless of the battery voltage, the *real* transmission efficiency of the PA is not 50% (2.42/4.84), but 41.3% (2/4.84). The efficiency for the various operating battery voltage levels are shown in Fig. 3. The efficiency of the PA optimized for 2-W generation at the 3.5-V battery drops to 34.7% for the maximally charged battery of 4.2 V.

B. Efficiency Degradation of Supply Modulator

To overcome low efficiency of an LDO over the battery voltage variation and limited BW of a switching converter, [8] introduces the ET LDO whose supply is modulated by a buck converter. Efficiency of the LDO is improved by the high-efficiency step-down buck converter, but two regulators (LDO and buck converter) cause a significant voltage drop from the battery, limiting the high output power generation. Moreover, it is still hard to achieve a wide BW and high efficiency together due to the limited BW of the buck converter tracking the envelope signal.

In [9]–[15], the hybrid switching structure is introduced to achieve a wide BW and high efficiency simultaneously. The simple architecture of the hybrid switching supply modulator is shown in Fig. 4. It is composed of a wideband class-AB buffered linear amplifier and a highly efficient step-down buck switching converter. For the input signals with narrow BW and low PAPR, the switching converter provides most of the current to the load and the linear amplifier compensates the ripple current generated by the switching converter so that the overall efficiency of the hybrid switching supply modulator is close to the efficiency of the switching converter. There is little contribution to
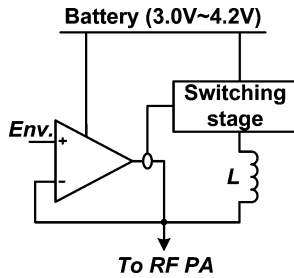
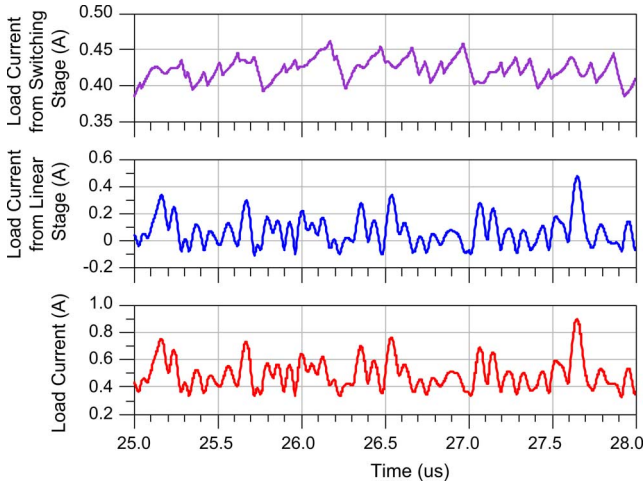Fig. 4. Basic architecture of the hybrid switching supply modulator.

Fig. 5. Simulated current waveforms of the hybrid switching amplifier.
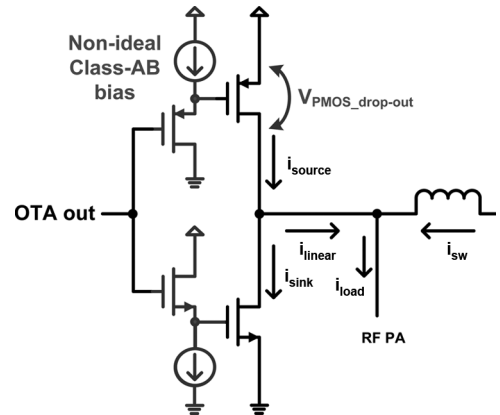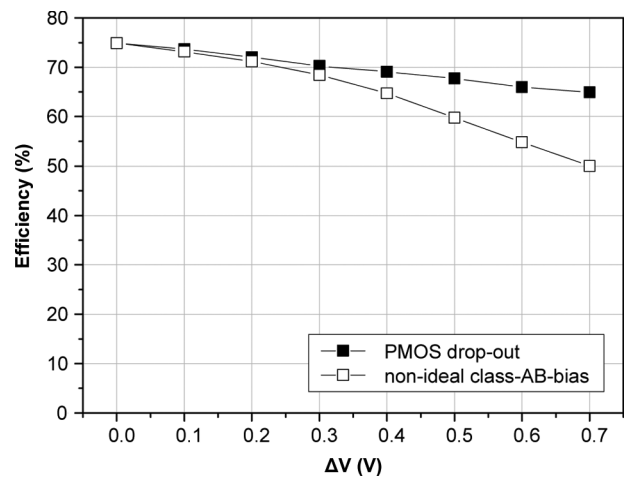

Fig. 6. Schematic of the class-AB output stage.

Fig. 7. Simulated efficiency degradation of the supply modulator according to the battery voltage variation.

the overall efficiency by the linear amplifier. However, for input signals with wide BW and high PAPR, the switching converter does not follow the high slew-rate input signal so that it supplies the average current to the load, while the linear amplifier sources and sinks the current according to the required load current, as shown in Fig. 5. When the switching converter does not provide sufficient current to the load, the linear amplifier assists to source the current to the load through the pMOS transistor of the output stage buffer in Fig. 6. When the battery voltage is higher than the minimum battery voltage, the drop-out voltage across the pMOS transistor, $V_{DD} - V_{\text{load}}$, is increased, which results in the efficiency degradation of the linear stage. Since the current provided by the linear amplifier is not negligible in the case, the overall efficiency degradation of the supply modulator by the battery voltage variation becomes considerable.

In the battery depletion condition, in addition, to keep the class-AB bias of the output stage in the linear amplifier, an adaptive biasing scheme such as the tunable quiescent current limiting circuit is required. Otherwise, the shoot-through current is changed by the incorrect bias condition. When it is smaller than the appropriate level, the linearity is degraded. On the other hand, when it is too excessive, the efficiency is significantly reduced. As a result, the unstable battery condition significantly degrades efficiency of the modulator.

Fig. 7 illustrates the efficiency degradation of the modulator resulting from the above factors. In this simulation, the supply modulator is designed for 3.5-V supply voltage and the maximum load voltage is 3 V. The supply voltage is then increased with the battery voltage offset to observe the efficiency degradation. At the minimum battery voltage, the simulated efficiency

of the modulator is 74.9%, and it is reduced to 50.0% at the maximum battery voltage of 4.2 V.

III. DESIGN OF NEW SUPPLY MODULATOR

A. Design Concept

To achieve high efficiency over the entire battery voltage levels, an additional regulator is inserted between the battery and the supply modulator, as shown in Fig. 8. It supplies a constant voltage to the linear amplifier and the problems mentioned in Section II are solved. Among various types of regulators, the boost converter is the right choice for its high efficiency and voltage step-up characteristics. If the step-down converter (such as buck converter) is employed, there will be too much voltage drop from the battery to the supply of PA, while there is no voltage drop by the regulator in the step-up topology. Moreover, if we can increase the supply voltage to 5 V, considering the 0.5-V drop across the supply modulator, the PA now operates with 4.5-V supply voltage. In this case, to meet the 2-W output power level of the modern wireless communication standards, the maximum current of the power cell is 1 A, which is 1.5 times smaller than the conventional ET PA directly coupled to the 3.5-V battery. It results in smaller die size and routing loss, which means lower cost and higher efficiency.

Due to the boost converter, the linear amplifier now has an additional source of the switching noise. The output ripple
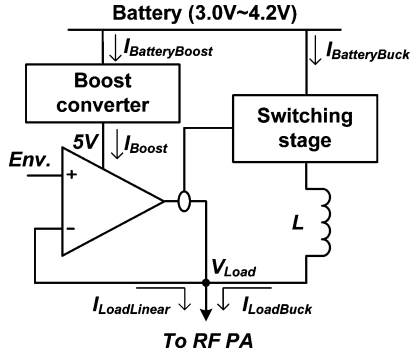
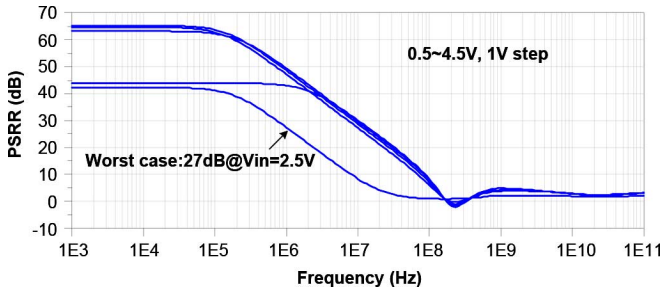Fig. 8.   Proposed supply modulator architecture.

Fig. 9.   PSRR of the linear amplifier in HSA with the input dc voltage from 0.5 to 4.5 V.

voltage of the boost converter can be delivered to the modulator's output, and finally to the output of the PA. To present high purity signal to the antenna, distortion of the PA should be less than −50 dBc. Considering the 29-dBm average output power of the modulator, the ripple power should be less than −21 dBm, which is about 8 μW. Since the load PA impedance of the modulator is about 5 Ω, the ripple voltage needs to be smaller than 6.3 mV. It determines the required power supply rejection ratio (PSRR) for the linear amplifier, and the output ripple voltage $V_{\mathrm{OutRipple}}$ can be expressed as

$$V_{\mathrm{OutRipple}} = \frac{V_{\mathrm{BoostRipple}}}{\mathrm{PSRR}}. \tag{6}$$

Since output ripple voltage of the designed boost converter is less than 20 mV and its switching frequency is about 680 kHz in the simulation, the required PSRR has to be larger than 20 dB for the ripple voltage under 2 mV. In Fig. 9, the simulated PSRR of the linear amplifier for the various input voltage is presented. In this simulation, the buck converter is replaced with a constant current source. Here, the x-axis is the frequency of the input signal. It shows the PSRR is larger than 40 dB for all input voltage levels, except for the input dc voltage of 2.5 V, where the PSRR is about 27 dB at 1 MHz. As well described in the previous publication on the hybrid switching supply modulator, the switching ripple of the buck converter is also compensated by the linear amplifier due to its low output impedance. The average switching frequency of the buck converter in the designed supply modulator is about 5 MHz, which can be slightly changed by the operating battery voltage level.

As shown in Fig. 8, we have adopted the boost converter only to the linear amplifier of the modulator, while the buck converter is directly coupled to the fluctuating battery. The linear amplifier
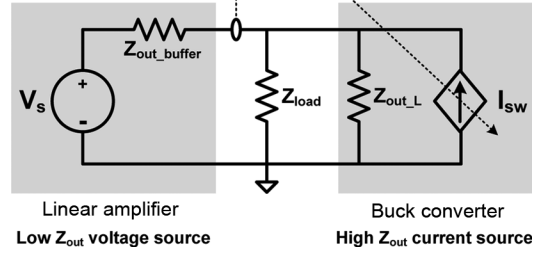

Fig. 10.   Conceptual operation of the hybrid switching structure.

is now operating with the boosted supply voltage and stably regulates the load (the PA). In this architecture, the efficiency degradation by the additional regulator is not significant since the current of the linear amplifier is a small portion of the overall load current. The efficiency of the proposed boosting supply modulator is calculated as follows:

$$\eta_{\mathrm{Boost}} = \frac{5V \cdot I_{\mathrm{Boost}}}{V_{\mathrm{Battery}} \cdot I_{\mathrm{BatteryBoost}}} \tag{7}$$

$$\eta_{\mathrm{Linear}} = \frac{V_{\mathrm{Load}} \cdot I_{\mathrm{LoadLinear}}}{5V \cdot I_{\mathrm{Boost}}} \tag{8}$$

$$\eta_{\mathrm{Buck}} = \frac{V_{\mathrm{Load}} \cdot I_{\mathrm{LoadBuck}}}{V_{\mathrm{Battery}} \cdot I_{\mathrm{BatteryBuck}}} \tag{9}$$

$$\eta_{\mathrm{Overall}} = \frac{V_{\mathrm{Load}} \cdot (I_{\mathrm{LoadLinear}} + I_{\mathrm{LoadBuck}})}{V_{\mathrm{Battery}} \cdot (I_{\mathrm{BatteryBoost}} + I_{\mathrm{BatteryBuck}})} \tag{10}$$

$$= (1 - \alpha) \cdot \eta_{\mathrm{Boost}} \cdot \eta_{\mathrm{Linear}} + \alpha \cdot \eta_{\mathrm{Buck}} \tag{11}$$

where α is defined as the ratio of the dc current consumption from the buck converter ($I_{\mathrm{BatteryBuck}}$) to the total dc current consumption from the battery ($I_{\mathrm{BatteryBoost}} + I_{\mathrm{BatteryBuck}}$). Assuming that α, η_{Linear}, η_{Boost}, and η_{Buck} are 0.7, 50%, 90%, and 90%, respectively, the efficiency of the proposed supply modulator is 76.5%, while those of modulators in Fig. 4 is 78%.

In this hybrid architecture, the buck converter operates as a high output impedance current source, while the linear amplifier works as a low output impedance voltage source, as described in Fig. 10. Thus, there is ideally no reverse current flowing through the buck converter. However, in practice, it happens if some conditions are not satisfied. Assuming $V_{\mathrm{Load}} = V_{\mathrm{DC}} + V_{\mathrm{AC}} \cdot \sin(2\pi f_s t)$, V_{DC} should be lower than V_{Battery}, and $Z_{\mathrm{out\_L}}(= j2\pi f_s L)$ has to be much higher than Z_{Load} since the current from the linear amplifier sees the Z_{Load} and $Z_{\mathrm{out\_L}}$ in parallel. For the modern wireless communication systems, the above conditions are easily satisfied. V_{DC} is lower than V_{Battery} due to high PAPR and $Z_{\mathrm{out\_L}}$ is higher than Z_{Load} due to wide BW. There is no reverse current flowing from the output of the linear amplifier to the output of the buck converter even at the output voltage instantaneously higher than the supply voltage of the buck converter. Therefore, the supply voltage of the buck converter can be lower than that of the linear amplifier for those signals.

B. Circuit Implementation

The designed boost-mode hybrid switching supply modulator is composed of a battery-to-5-V boost converter, a linear amplifier, and a buck converter, as shown in Fig. 11. The boost converter employs the thick-oxide 0.35-μm CMOS devices for
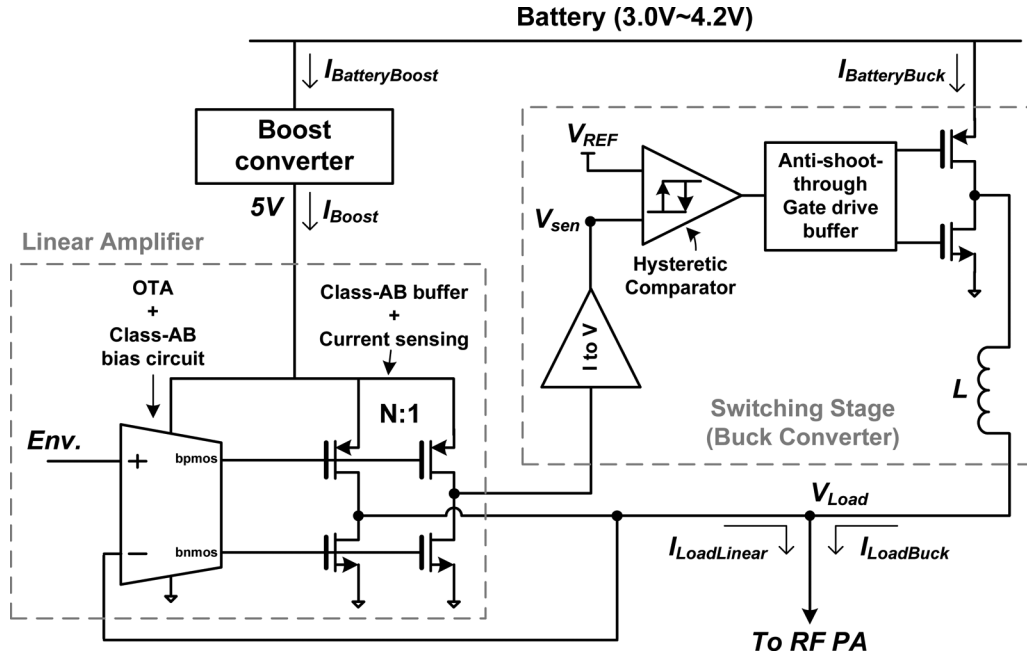
Fig. 11.   Schematic of designed boost-mode hybrid switching supply modulator.

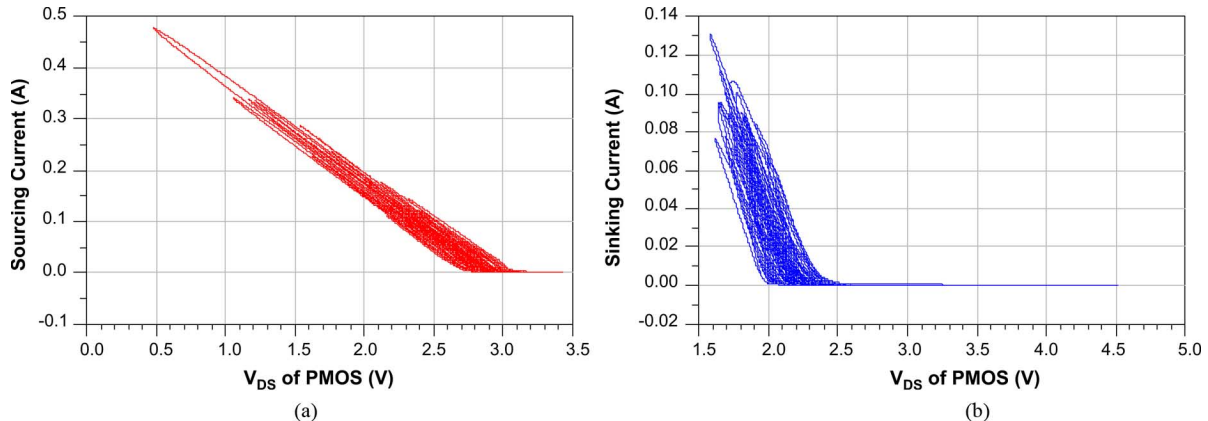
Fig. 12.   Simulated I–V curve of nMOS and pMOS transistors in the class-AB output stage of the 5-V boosted linear amplifier.

switches, which are stacked to prohibit breakdown of the transistors [18]. The current-mode boost converter based on [19] is designed to cover the battery variation range from 2.8 to 4.2 V. The linear amplifier consists of the folded-cascode two-stage operational trans-conductance amplifier (OTA) and the class-AB output stage.

Since the envelope shaping technique for the linear operation of the ET PA with the offset voltage of 1.5 V is applied [14], the pMOS transistor of the output buffer operates in the safe region, as shown in Fig. 12. For the nMOS transistor, the $V_{\rm DS}$ is instantaneously larger than 3.5 V, but the current through the nMOS is nearly zero. In this region, the switching buck converter does not provide the sufficient current to the load so that the linear amplifier sources the insufficient current to the load. That is, the nMOS is turned off and it is allowed to be 4.5 V instantaneously during the very short time for the wide BW of the modern wireless communication signals. (Of course, it will be better to use the higher voltage process for the reliability issue, if it is available. For the information on the real measured breakdown voltage of the sub-micrometer CMOS process, refer to [20].)

The buck converter provides most of the current to the load, and its switching state is determined by the programmable hysteretic comparator, which is able to control the switching frequency for multimode operation [14]. The divided switches with current control technique for low switching noise and antishoot-through current is also used for the buck converter [21].

IV.   MEASUREMENT RESULTS

Over the operating BW from 2.5 to 2.7 GHz, a class-AB PA, which is fabricated using an InGaP/GaAs 2-μm HBT process [22], with 4.5-V supply voltage provides more than 32-dBm output power with the maximum power-added efficiency (PAE) of 58.5%. Chip size of the designed supply modulator, including all pads, is 2.6 mm × 1.7 mm. The die photograph is presented in Fig. 13. It drives the load impedance of 4.7 Ω with the maximum output voltage of 4.5 V. The measured efficiency of the supply modulator with the 3.3-V battery voltage is 75.4% for the shaped 3GPP LTE envelope signal. Combining the class-AB PA and the supply modulator, the PAE of 31.6% with the battery voltage of 3.3 V is achieved with the gain of 24.8 dB at the
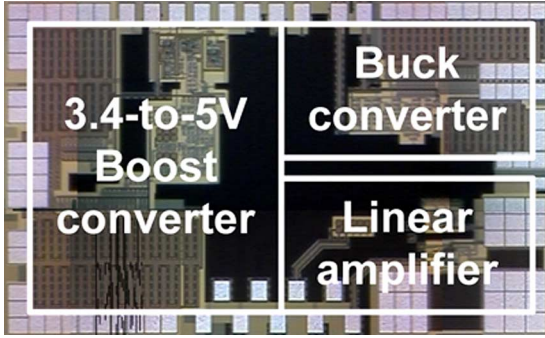
Fig. 13. Microphotograph of the fabricated boost-mode hybrid switching supply modulator.
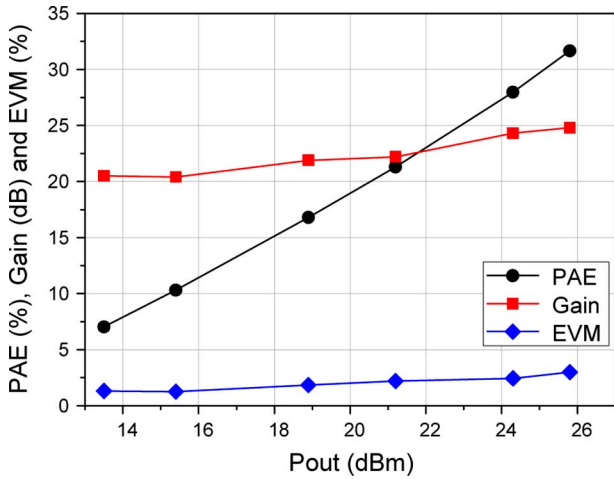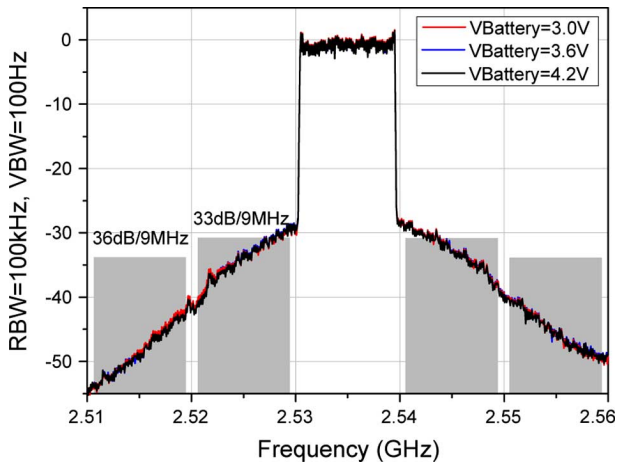

Fig. 16. Measured efficiencies of the 5-V boosting ET PA for LTE.

Fig. 14. Measured PAE, gain, and EVM of the ET PA for LTE.

Fig. 15. Measured spectra of the ET PA output for LTE.

efficiency over the entire battery voltage levels. The maximum efficiency of the modulator is 76.8% at the battery voltage of 3.6 V. It is because the optimum battery voltage for the boost converter and the buck converter is different. For the boost converter, the efficiency is reduced for the low battery voltage. For the buck converter, however, there is an optimum battery voltage (here designed to 3.5 V) as the amount of the current from the buck converter slightly depends on the battery voltage. For the operating battery voltage higher than the optimum level, there is an excessive current to the load and it is sunk to the class-AB output stage of the linear amplifier, which induces the efficiency degradation of the overall supply modulator. At the 25.8-dBm output power, the implemented ET PA delivers the minimum efficiency of 29.1% at the 4.2-V battery, while it shows maximally 32.3% at the 3.6-V battery.

V. CONCLUSIONS

The boost-mode hybrid switching supply modulator has been proposed and designed for the practical operation environment where the modulator is directly coupled to the battery. It provides the high efficiency over the entire battery voltage levels, while the efficiency of the conventional modulator focused on the design at the minimum battery voltage can be very poor at a high-voltage region. It enables the high-voltage operation of the RF PA resulting in the reduced chip size for 2-W peak-envelope output power and the high efficiency by the reduced current and routing loss. Therefore, the supply modulator is the optimized PMIC for PAs. The fabricated chip is composed of the battery-to-5-V boost converter, the linear class-AB amplifier and the highly efficient buck converter. The supply voltage of the linear amplifier is boosted to 5 V, and it enables the RF PA operating with the maximum 4.5-V supply voltage regardless of the battery depletion. For the 10-MHz BW 3GPP LTE envelope signal, it provides the maximum output voltage of 4.5 V to the 4.7-Ω resistive load with 76.8% efficiency. With the 2.535-GHz class-AB PA, it has an overall PAE of 32.3% at the output power of 25.8 dBm. Due to the additional boost converter coupled to the linear amplifier, the proposed supply modulator presents the robust performance over the battery voltage variation while the efficiency degradation is minimized.

output power of 25.8 dBm. The average PAE and the gain according to the output power level are presented in Fig. 14. Due to the envelope shaping technique, the ET PA satisfies the 3GPP LTE spectrum emission mask specifications [23], as shown in Fig. 15. The robust operation of the boosting supply modulator against the battery voltage variation enables the stable spectral performance of the ET PA, as well as the output power. The PAE variation according to the battery voltage is measured and illustrated in Fig. 16. There is no significant degradation of the
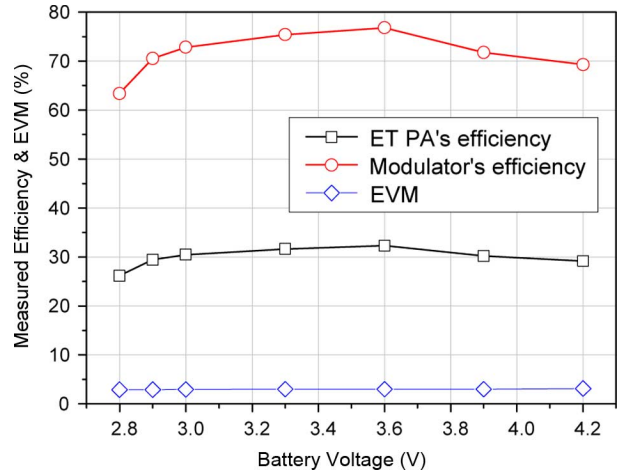
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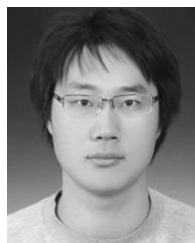
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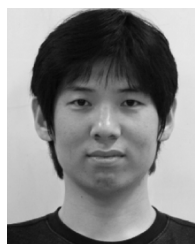
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