A Wideband Digital RF Receiver Front-End Employing a New Discrete-Time Filter for m-WiMAX

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***Abstract*—A wideband digital RF receiver front-end employing a discrete-time (DT) filter is presented for application to m-WiMAX (WiBro). By employing a sampling mixer and a DT filter, the receiver operates in the charge domain. In addition to the flexibility of the DT filter, the new non-decimation finite impulse response (NDF) filter can be cascaded to a conventional finite impulse response (FIR) filter without the decimation effect. Thus, we can easily increase the order of the $sinc^n$ function-type filtering response and the signal processing bandwidth. The FIR filter is also modified to reduce the noise and the number of required clock signal. Because of the new filter configuration, clock signals can be shared by the FIR filter and NDF filter and the clock generator circuit can be simplified. The designed receiver front-end is implemented using an IBM 0.13-μm RF CMOS process. The fabricated chip satisfies the m-WiMAX specification of an 8.75 MHz channel bandwidth and the total system current dissipation is 26.63 mA from a 1.5-V supply voltage.**

***Index Terms*—Digital RF, discrete-time filter, non-decimation FIR filter, radio frequency (RF), receiver front-end, wideband.**

I. Introduction

As WIRELESS communication technology advances, new wireless communication standards require not only higher mobility for the user's convenience but also larger channel bandwidth to handle multi-media contents that has a large amount of data. Moreover, multi-mode/multi-band technology, which makes it possible to process various wireless communication standards using only one device, has been widely researched to achieve higher chip area efficiency and fabrication cost saving [1]–[5]. Because of this demand, a transceiver system for software-defined radio (SDR) or the reconfigurable RF concept is being actively developed now. Because the channel lengths of devices have been scaled down as the CMOS process technology advances, device speeds have become faster and the resolution in the time domain has become better than that in the voltage domain. The digital RF concept, which involves processing the signal in the discrete-time and the charge domain, has become a useful technique in the development of SDR or reconfigurable RF [6]–[14]. A sampling receiver uses the digital RF concept, employing a sampling mixer and a charge-domain filter, to realize signal frequency conversion and selection. The filtering response can be flexibly adjusted using the control of clock signals to prevent aliasing due to the analog-to-digital converter (ADC) sampling operation.

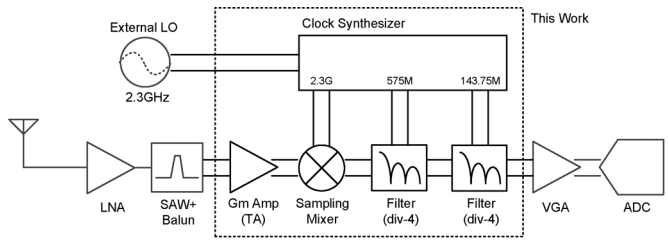

Fig. 1. Digital RF receiver front-end system architecture.

The DT filter, which employs a switched-capacitor circuit has a $sinc$ function filtering response with a limited bandwidth and its applications are limited to narrowband wireless communication standards [6], [7]. To overcome the bandwidth problem, we have proposed a non-decimation finite impulse response (NDF) filter. The NDF filter has the moving average characteristic, but without the decimation effect. This characteristic enables the NDF filter to be cascaded with another DT filter and allows us to increase the order of the $sinc$ function-type filtering response. The clock generator is an important block in the digital RF receiver front-end. To generate the complicated clock signals required for the DT filter, a complex and large-sized clock generator is needed. The finite impulse response (FIR) filter configuration has been modified to reduce the number of required clock signal and to improve the noise performance of the filter chain. The NDF filter has also been designed to share the same

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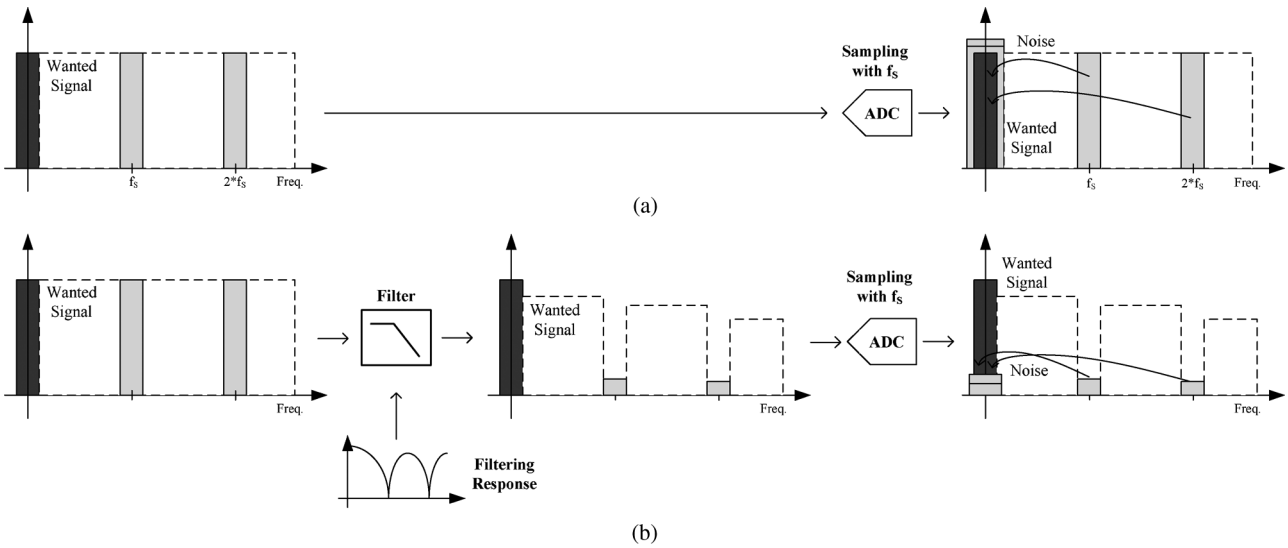

Fig. 2. SNR degradation due to aliasing by ADC sampling (a) without filter and (b) with discrete-time filter.

clock signal with the FIR filter. Through this optimization, the clock generator can be simplified, reducing the chip area and the noise figure [15].

In this paper, we present a digital RF receiver system with a wideband signal processing capability employing the simplified clock and NDF filter. The designed receiver front-end is targeted for the m-WiMAX (WiBro) standard with an 8.75 MHz channel bandwidth. This paper is organized as follows: the system architecture and specifications of the DT filter are described in Section II and the details of the circuit implementation are presented in Section III. Section IV presents the experimental results obtained from the designed digital RF receiver front-end fabricated using the 0.13-μm RF CMOS process.

II. System Architecture and Specification of the Discrete-Time Filter

The proposed digital RF receiver front-end system architecture for m-WiMAX is shown in Fig. 1. The carrier frequency of m-WiMAX is 2.3 GHz and the chosen ADC sampling rate is 143.75 MHz. The required decimation ratio of the two-stage DT filter chain is 16 (4×4) and each DT filter has a decimation ratio of 4.

The signal received by an antenna is amplified by a low-noise amplifier (LNA). The amplified signal is fed to a SAW filter and a balun, to suppress the interferer components and to get a differential signal, respectively. In the transconductance amplifier (TA) stage, the signal is converted from a voltage form to a current form. The converted current signal is sampled and down-converted to the baseband by the following passive sampling mixer.

After the RF front-end stage, the down-converted signal is sampled and converted to a digital signal by the ADC. Because of this sampling operation of the ADC, not only the wanted signal but also large interferers at the harmonic frequencies of the ADC sampling rate are folded into the baseband. The folded interferer components become noise and degrade the signal-to-noise ratio (SNR) of the receiver. A graphical description of this aliasing problem is shown in Fig. 2. Without the filter, the large interferer is directly folded into the baseband with the wanted signal, and it degrades the SNR significantly. Therefore, we need a baseband antialiasing filter in front of the ADC to suppress the harmonics. One kind of baseband antialiasing filter is the DT filter. The filtering response of the DT filter can be easily adjusted by controlling the local oscillator (LO) clock signal, the number of taps, or the sampling capacitance ratio. This flexibility makes the DT filter a favorable filter solution for the SDR or reconfigurable RF receiver system.

Since the carrier channel of m-WiMAX is located at 2.3 GHz, the clock signal frequency used in the sampling mixer of the direct conversion receiver architecture is also 2.3 GHz. The first DT filter uses a 575 MHz (2.3 GHz ÷ 4) clock signal, and the second filter uses a 143.75 MHz (575 MHz ÷ 4) clock signal. By employing these clock signals in the DT filters, the baseband filter chain has null points with large attenuation level at all the harmonics of the ADC sampling rate. The total filtering response of the DT filter chain using this clock configuration is shown in Fig. 3. The null points located at the harmonics of the ADC sampling rate and the interferers are attenuated.

The sensitivity of $64QAM(3/4)$ in the m-WiMAX system is -72 dBm [16] and the SNR for a bit-error ratio (BER) of 10^{-6} is 20 dB. Using an implementation margin (IM) for the SNR of 5 dB and a maximum interferer power $(P_{Int,MAX})$ of -30 dBm, the required attenuation level at the harmonics of the ADC sampling rate can be calculated using following equation (its graphical explanation is shown in Fig. 4)

$$\begin{aligned} AttnenuationLevel &= P_{int} - AcceptableNoiseLevel \\ &= P_{int} - (P_{S,min} - (SNR + IM)) \\ &= -30 - (-72 - (20 + 5)) \\ &= 67 \text{ dB}. \end{aligned} \tag{1}$$

As a result, the required attenuation level for the channel bandwidth of 8.75 MHz at each null point should be over 67 dB.

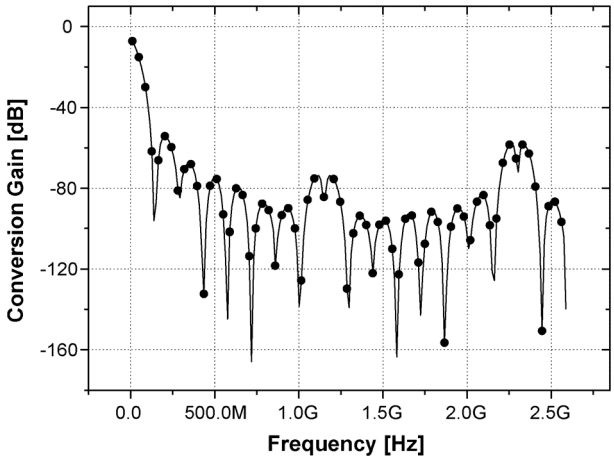

Fig. 3. Filtering response of the total discrete-time filter chain.

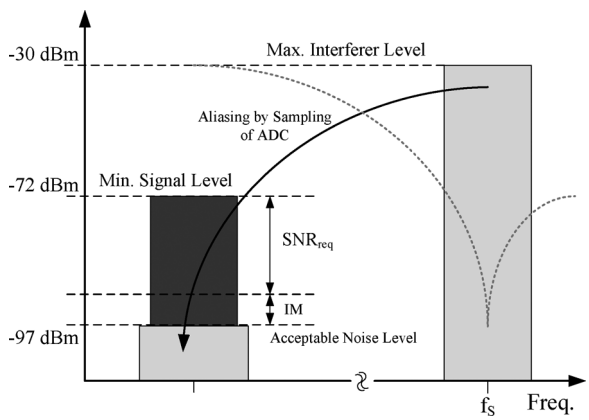

Fig. 4. Calculation of the required attenuation level.

However, the FIR filter, which is based on the basic DT filter, has the filtering response of a $sinc$ function with limited bandwidth. To increase the bandwidth, the DT filter needs to be cascaded in order to have a higher order $sinc$ function filtering response. The $sinc^2$ function filtering response is sufficient to handle the m-WiMAX wideband signal. However, because of the decimation, the FIR filter cannot be cascaded. Therefore, we have developed the new NDF filter to increase the order of the $sinc$ function filtering response through cascading. A detailed description of the NDF filter is presented in following section. Each filter block of our RF receiver front-end contains a cascaded NDF filter and FIR filter [17]. The filtered signal is amplified by the variable gain amplifier (VGA) and finally sampled by the ADC, converted to the digital domain without any aliasing problem. The clock generator generates the multi-phase clock signals needed for the operations of the mixer and the filter chain with an external LO signal.

III. Circuit Implementation

A. Transconductance Amplifier and Sampling Mixer

After amplification by the LNA, the voltage input signal is converted to a current signal by the TA. Fig. 5(a) shows a schematic of the TA employing ac AC-coupled inverter-type common source amplifier using the multi-gated transistor

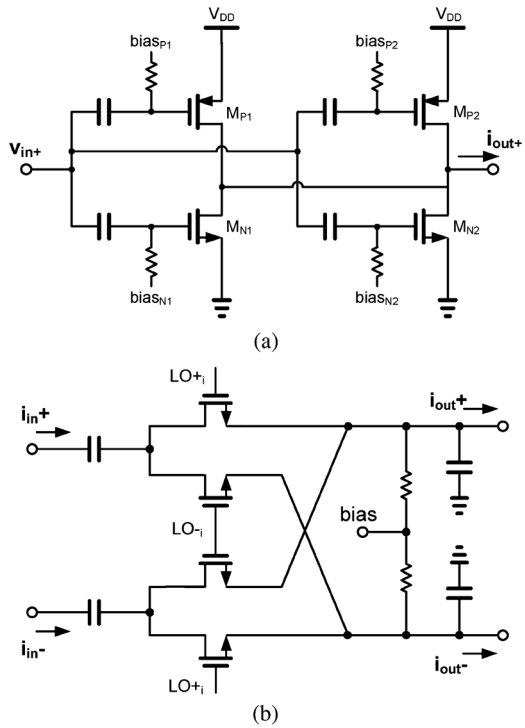

Fig. 5. Schematic of (a) transconductance amplifier and (b) sampling mixer.

(MGTR) technique [18]. The two branches of the TA are biased at different gate voltages to cancel the gm_3 components, which produces a high linearity. The series-connected pMOS and nMOS transistors contribute to the larger g_m but maintain low power consumption by reusing DC current.

The converted current signal is fed to the sampling mixer. The sampling mixer stage shown in Fig. 5(b) consists of a basic nMOS switch and the gates of the switches are driven by the differential I/Q LO signal generated by the clock generator. The current sampled by the mixer is stored in the capacitive load and is delivered to the switched-capacitor DT filters, which are operated in the charge domain. The *RC* component of the passive mixer load also acts as a passive *RC* low-pass filter, further attenuating the unwanted interferers. Because the sampling mixer consists of only the transistor switches with no DC bias current, it can mitigate the flicker noise problem, which is critical for a direct conversion receiver.

The conversion gain of the charge-domain double-balanced sampling mixer is given by

$$A_m \cong \frac{1}{2} sinc(f_{RF}\Delta t)\frac{T}{\Delta T} sin\left(\frac{\Delta T}{T}\pi\right) \tag{2}$$

where

$$\Delta T = \frac{\int_0^T g(t)\mathrm{d}t}{\mu_n C'_{OX}\frac{W}{L}V_C}. \tag{3}$$

Δt is the duration time during which the sampled charges stay in the load capacitor C_L and f_{RF} is the input signal frequency. Assuming $\Delta T/T = 0.5$ because of square wave LO, the calculated conversion gain of the passive mixer is -3.92 dB.

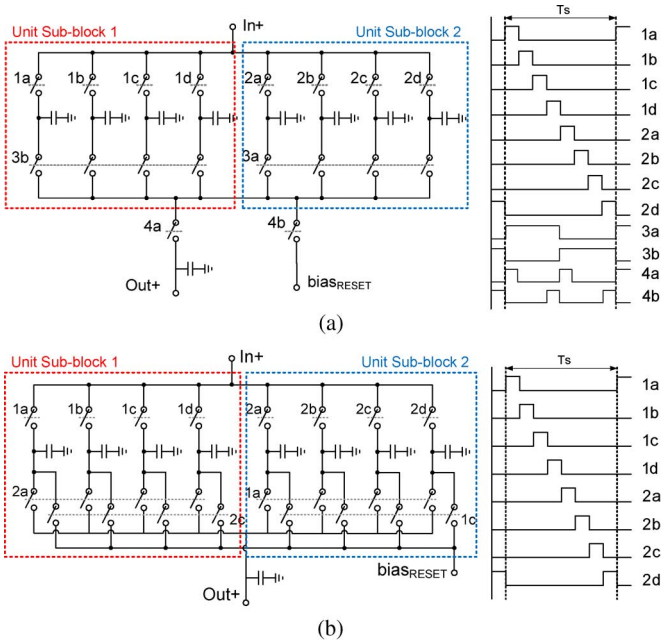

Fig. 6. Schematic and required clock signals of (a) conventional FIR filter and (b) noise-optimized FIR filter.

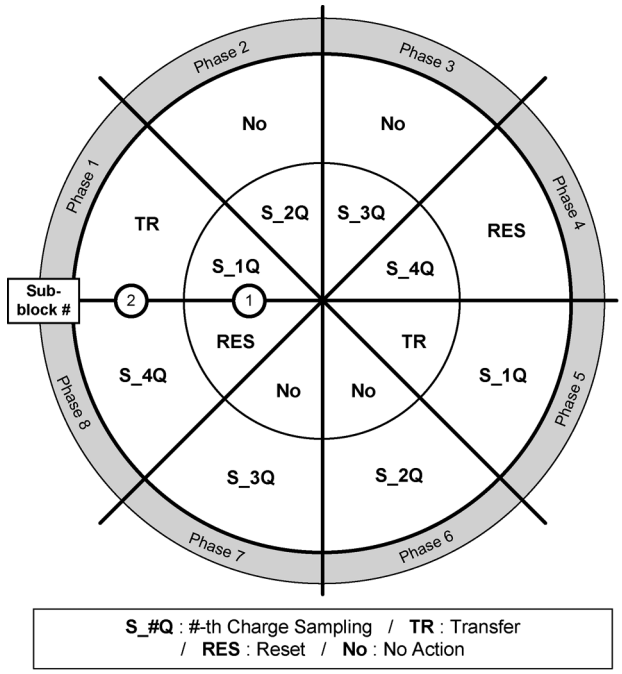

Fig. 7. Description of FIR filter operation.

The noise figure (NF) of the charge-domain sampling mixer is given by [19]–[21]

$$NF = 1 + \frac{4kT/g}{4kTR_S}\frac{1}{A_m^2} = 1 + \frac{\pi^2 \Delta T}{4Tg_{\max}R_S}\frac{1}{A_i^2 \sin^2\left(\frac{\Delta T}{T}\pi\right)}. \quad (4)$$

Assuming $g_{\max}R_S = 0.1$, the calculated DSB NF of the passive mixer is 14.1 dB.

B. Discrete-Time Filter

The digital RF receiver front-end employs the DT filter chain to prevent folding of the interferer into the baseband. The DT filter consists of the basic nMOS transistor switches and charge-storing capacitors as shown in Fig. 6.

The DT filter has some advantages compared to a continuous-time filter. First, the DT filter performs clock-based operation and its filtering response can be changed easily by controlling the LO frequency. Because of these features, the DT filter is flexible and programmable, and it can be used in multi-mode and multi-band applications. Following the passive sampling mixer, which uses a capacitive load, the DT filter also performs sample-and-hold operation in the charge domain. Thus, it is able to mitigate the voltage headroom problem and improve the linearity performance. These characteristics of the DT filter make it suitable for SDR application [7]. Even though the DT filter has an aliasing problem due to its sampling operation, this problem can be solved using pre-filtering in front of the filter. In addition, a large number of capacitors are also required; techniques to reduce the required capacitance are actively being studied now.

The baseband DT filter used in this study consists of two stages consisting of a divide-by-4 DT filter. In each stage, an NDF filter and an FIR filter are cascaded to obtain enough bandwidth, i.e., more than 8.75 MHz. The DT filter performs clock-based operation, and good clock generator is important for the accurate sampling operation, low power consumption and reduction of the chip area. In this study, clock simplification and filter noise performance improvement are achieved through optimization of the filter structure.

1) Noise-Optimized FIR Filter: An FIR filter is a basic DT filter. A schematic and the required clock signals of the conventional FIR filter are shown in Fig. 6(a). The operations of the FIR filter can be categorized as sample, transfer, and reset operations. This operation sequence is graphically described in Fig. 7. The dotted boxes in Fig. 6(a) and (b) are unit sub-blocks. Sub-block 1 sequentially does each operation in the order given in inner circle in Fig. 7, while sub-block 2 does the operations given in the outer circle. For example, when the sub-block 1 is performing charge sampling in the first sampling capacitor, the sub-block 2 is doing a transfer operation. To explain in detail, within a unit sub-block, each sampling capacitor stores the charge from the input current signal during the switch's ON period, which is controlled by the clock signal. After the sampling of the four charge-storing capacitors (clocks 1a–1d; see Fig. 6(a)), the charges are transferred to the output integrating capacitor during the common ON time of clock 3b and clock 4a, and the charges are averaged and stored in C_{out}. The remaining charges in the sampling capacitors are removed to the reset node during the common ON time of clocks 3b and 4b. The other sub-block, which has 4-tap samplers, does complementary sample, transfer, and reset operations. It performs sample operations during ON time of clock 2a–2d, transfer operation during the common ON time of clocks 3a and 4a, and reset operation during the common ON time of clocks 3a and 4b.

However, the required clock signals for this conventional FIR filter are quite complex. Clocks 1× and 2× and clocks 3× and 4× have different periods. Moreover, clock 3× and clock 4× have different pulse widths. Therefore, a clock generator must

have a very complicated structure, and we propose a new FIR filter, which is optimized for the reduction of the number of required clock signal and noise performance and presented in Fig. 6(b). The new FIR filter removes the separate switches for C_{out} and $bias_{RESET}$ and does the transfer and reset operations together with an average operation. This filter does not need clocks 3× and 4×, simplifying the clock generator structure. The required clock signals have the same periods and pulse widths and have only equal phase differences, so the clock generator can be realized area-efficiently with a very simple structure. The noise-optimized FIR filter operates in the same manner as the conventional FIR filter shown in Fig. 7.

The noise of the FIR filter consists of the kT/C noise from the sampling switches and the averaging switches and the flicker noise [22], [23]. Not only the kT/C noise but also the flicker noise of the transistor switches using clock 4b for the reset operation is an important noise source of the FIR filter. Using a non-stationary $1/f$ noise model, the noise voltage at the end of reset operation is given by [23]

$$V_n(t_r) = \int_0^{t_r} \frac{I_d(s)}{C} exp\left(-\int_s^{t_r} \frac{g_m(\tau)}{C} d\tau\right) ds. \tag{5}$$

Furthermore, the reset noise power is given by

$$\overline{V_n^2(t_r)} = \left(\frac{q}{A \cdot C_{OX}}\right)^2 \cdot \frac{1}{(t_r+\delta)^2} \int_0^{t_r}\int_0^{t_r}\int_{\lambda_H}^{\lambda_L} \cdot C_\lambda\left(s_1, |s_2 - s_1|\right) g(\lambda) d\lambda ds_1 ds_2 \tag{6}$$

where λ is the transition rate, and C_λ is the autocovariance of the trapped electron number $N(t)$. This flicker noise caused during the ON phase of clock 4b (t_r duration) is stored in sampling capacitors C_S and directly transferred to the output capacitor in the next ON-phase of clock 4a. Unlike in the noise-optimized FIR filter, in the conventional FIR filter the transistor switch 4b is used to do the reset operation for all filter sub-blocks. Thus, the limited size of the transistor switch and the higher switching speed cause higher flicker noise than that of the noise-optimized FIR filter and also contribute to high output noise. In a noise simulation (PNOISE simulation of Cadence Spectre RF), the noise-optimized FIR filter reduces the output noise by about 20% with an ideal clock.

In addition, the clock generator of the conventional FIR filter requires more circuitry to generate the clocks 3× and 4× than is required by the clock generator of the noise-optimized FIR filter. The flicker noise from this additional clock generator circuitry is induced to the transistor switch of the filter and critically raises the output noise. When the filter structure is optimized, the clocks 3× and 4× are no longer required, and the clock generator circuitry can be simplified. Thus, the flicker noise induced by the D flip-flop of the conventional clock generator is removed, and the noise performance improves. When a real clock generator is applied, the output noise of the conventional FIR filter is significantly larger than that of the noise-optimized FIR filter due to much larger effect of the direct switch noise and indirect switch noise [24]. The results of the total output noise

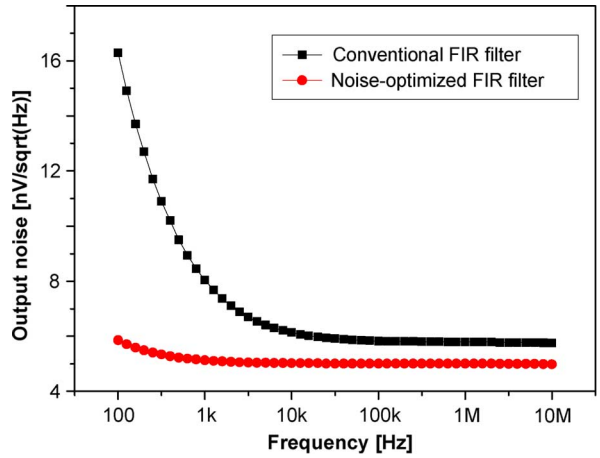

Fig. 8. Output noise simulation of FIR filters.

simulations with the real clocks of the two FIR filter structures are shown in Fig. 8.

The size of the sampling capacitor should be optimized by considering the chip area and the effects of parasitic capacitances or process variations. The sampling period and the number of taps determine the null point of the filtering response. However, the filter cannot be cascaded because the output sampling rate is decimated. In the case of a 4-tap FIR filter, the relation between the input and output sampling rate is given by

$$T_{S.out,FIR} = 4 \cdot T_{S.in,FIR}. \tag{7}$$

As a result, the conventional FIR filter has limitation on the attenuation level and bandwidth at the null points.

The filtering response of the FIR filter is given by

$$|H_{sinc}(f)| = \left|\frac{1 - e^{-j2\pi f T_S}}{j2\pi f T_S}\right| = sinc(fT_S) \tag{8}$$

$$|H_{avg}(f)| = \left|\frac{1}{m}\sum_{n=0}^{m-1} e^{-j2\pi f n T_S}\right| = \frac{sin(\pi f m T_S)}{m \cdot sin(\pi f T_S)} \tag{9}$$

$$\begin{aligned} |H_{FIR}(f)| &= |H_{sinc}(f)| \cdot |H_{avg}(f)| \\ &= sinc(fT_s) \cdot \frac{sin(\pi f m T_s)}{m \cdot sin(\pi f T_s)} \\ &= sinc(fmT_s). \end{aligned} \tag{10}$$

2) Non-Decimation FIR (NDF) Filter: To overcome the limitations of the conventional FIR filter, we proposed an NDF filter [17]. In this filter, the moving-average output is re-sampled at the original sampling rate. For example, the Div-4 FIR filter needs six sub-blocks to make up its 4-tap filter block: four for the sampling operation, one for the transfer operation, and one for the reset operation. A schematic of the NDF filter is shown in Fig. 9(a), and the principle of its operation is described in Fig. 10(a). The dotted box in Fig. 9(a) indicates a unit sub-block, and there are all six sub-blocks in an NDF filter. Each sub-block sequentially performs the first through fourth charge sampling, transfer, and reset operations with delays of the clock duration. For example, when sub-block 1 does the first charge sampling

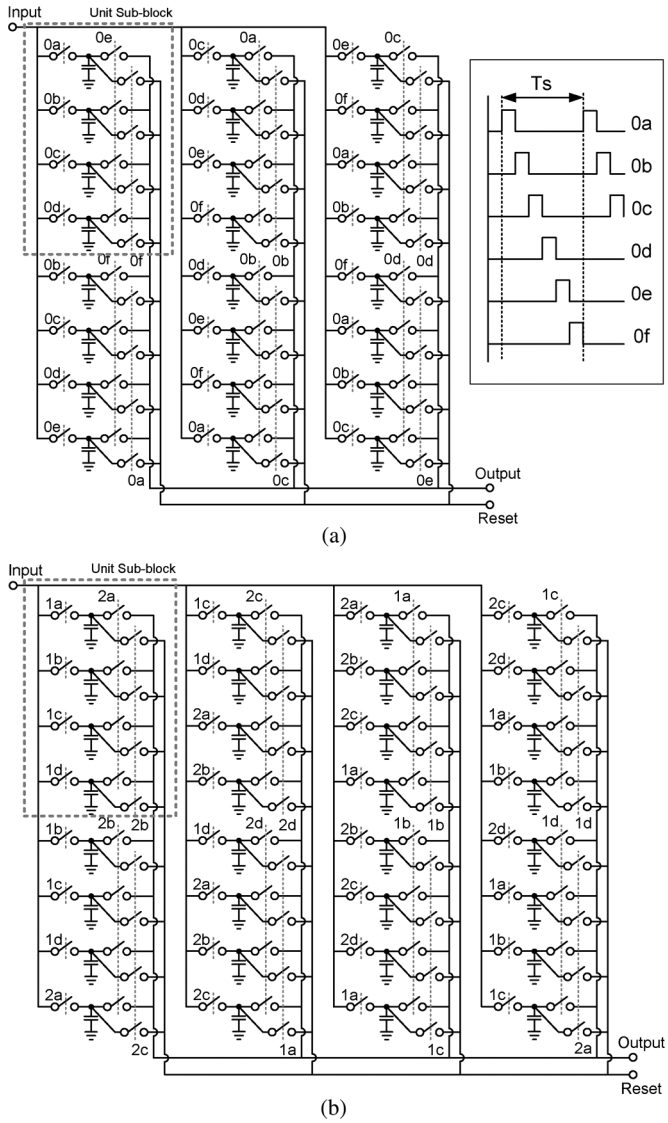

Fig. 9. Schematic and required clock signals of (a) NDF filter (6 sub-blocks) and (b) NDF filter (8 sub-blocks).

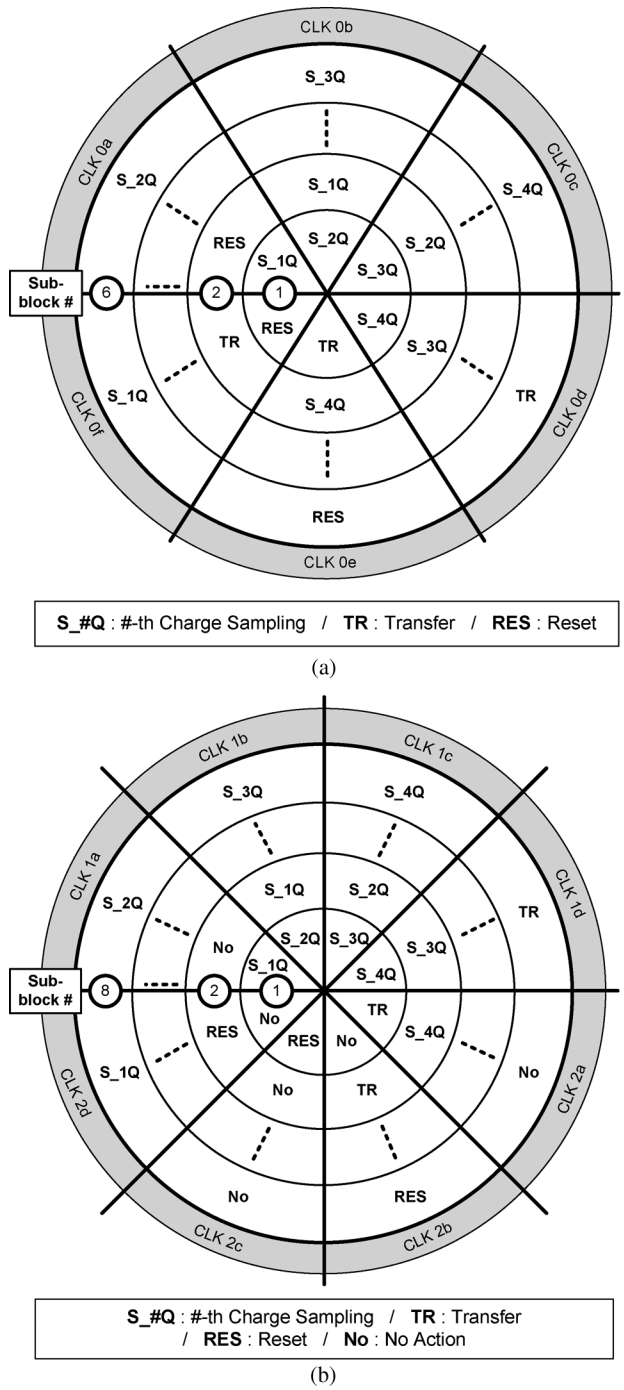

Fig. 10. Description of the operation of (a) NDF filter (6 sub-blocks) and (b) NDF filter (8 sub-blocks).

operation during ON time of clock 0a, sub-block 2 does the reset operation, sub-block 6 does the second charge sampling operation, and so on. During next clock 0b duration, the sub-block 1 does the second charge sampling operation, the sub-block 2 does the first charge sampling operation, the sub-block 5 does the third charge sampling operation, and so on. In this way, at least one of the sub-blocks is doing transfer operation at all times, so the input sampling rate of the NDF filter is the same as the output sampling rate

$$T_{S.out,NDF} = T_{S.in,NDF}. \tag{11}$$

In this NDF filter configuration, the clock signal of this 4-tap NDF filter is different from that of the decimation filter, as shown on the right side of Fig. 9(a). However, the NDF filter can share the same 8-phase clock signals of the FIR filter shown in right side of Fig. 6(b) through the addition of two more sub-blocks. The schematic of an NDF filter with the eight sub-blocks and its operational sequence are presented in Fig. 9(b) and Fig. 10(b), respectively. The details of its operation are similar to those of the operation of the NDF filter with six sub-blocks. Because it does not need any additional clock generator circuitry, we can reduce the chip area and power consumption.

As a result, the NDF filter can process the signal without any decimation effect. The filtering response of the NDF filter is the same as that of the FIR filter. Therefore, the order of the filtering response can be increased by cascading the NDF filter to an FIR

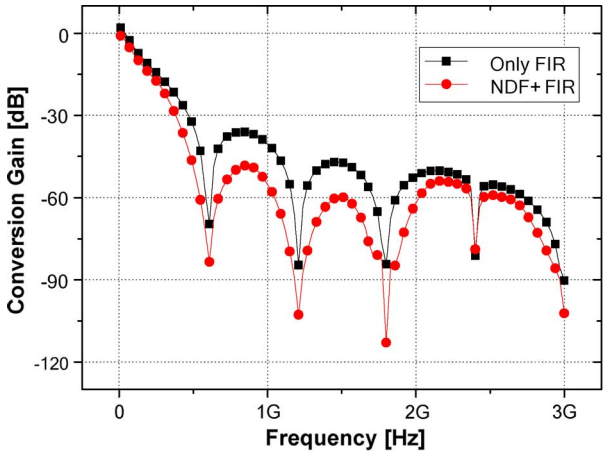

Fig. 11. Simulation results for FIR filter and NDF+FIR filter.

filter. The filtering response of the cascaded NDF and FIR filters can be presented as

$$\begin{aligned} |H_{NDF+FIR}(f)| &= |H_{NDF}(f)| \cdot |H_{FIR}(f)| \\ &= sinc(fmT_S) \cdot sinc(fmT_S) \\ &= sinc^2(fmT_s). \end{aligned} \tag{12}$$

Furthermore, a filtering response of $sinc^n$ is possible through the cascading of (n-1) NDF filters to a FIR filter. Simulated filtering responses of only the FIR filter and of the cascaded NDF+FIR filter are shown in Fig. 11. By cascading the filters, we can achieve a higher attenuation level and a wider bandwidth at the null points of the filtering response.

C. Clock Generator

The digital RF receiver front-end needs clock signals not only for the down-conversion mixer but also for the DT filter chain. A block diagram of the clock generator is given in Fig. 12. The clock generator takes a LO signal as an input and generates the multi-phase clock signal with the required sampling rate. The clock generator consists of a simple D flip-flops and an inverter. A divide-by-4 circuit generates a clock signal with 1/4 of the LO frequency. After a 45° phase delay is applied using a poly-phase filter, the two clock signals are applied to the $V_{\rm DD}$ node and input node of the inverter. The inverter output becomes one of the multi-phase clock signal and by applying a D flip-flop series, the clock generator generates the multi-phase clock signals. The generated clock signals are shown on right side of Fig. 6(b). Each multi-phase clock signal should be buffered enough to drive the capacitance loads. By optimizing the clock buffer size, the DC current consumption of the clock generator can be minimized.

IV. Implementation and Experimental Result

The designed digital RF receiver front-end was fabricated using an IBM 0.13-μm RF CMOS process, and a photograph of the fabricated die is shown in Fig. 13. The die size is 2200 μm $\times$ 1200 μm including pads, and its active area without pads is

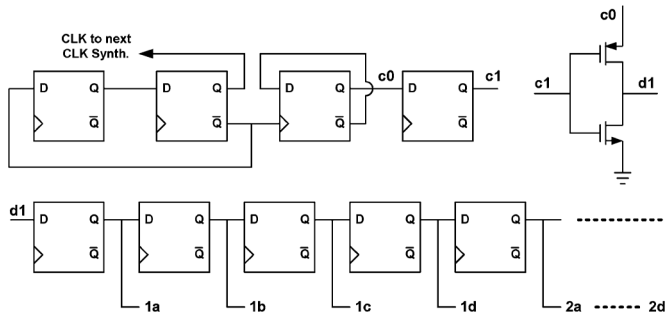

Fig. 12. Schematic of clock generator.

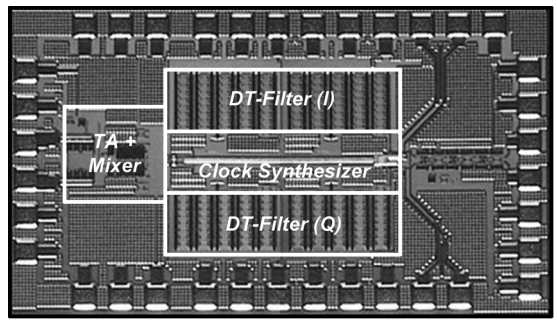

Fig. 13. Microphotograph of the fabricated chip.

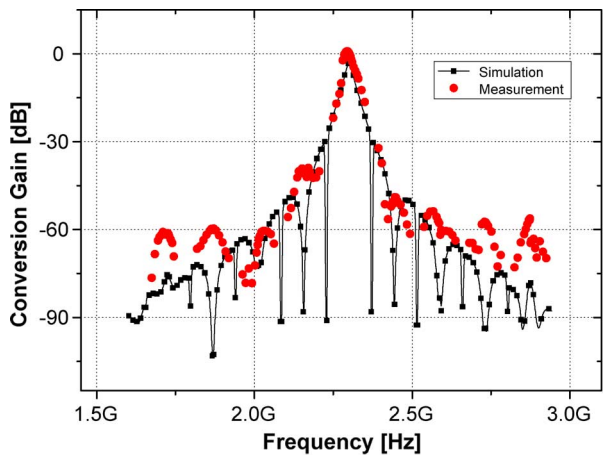

Fig. 14. Conversion gain of digital RF receiver system.

1100 μm $\times$ 800 μm, which is mainly occupied by the capacitors of the DT filter chain.

For the test, a single-tone RF input near the carrier frequency with the fixed 2.3 GHz LO frequency is swept, and the low-frequency output of the DT filter after the external VGA is measured. As shown in Fig. 14, the measured filtering response matches the simulation result very well. Harmonic suppression of the DT filter from the second harmonics of $f_{S,ADC}$ at 143.75 MHz is measured to be under -60 dBc.

Fig. 15 shows the attenuation level at the first harmonic of $f_{S,ADC}$. The measured result is about 90 dB, far below the required attenuation level of 67 dB. The null point slightly deviates from the theoretical value, because the real buffered clock signal is slightly different from the ideal clock signal. The in-band signal bandwidth for -3 dB is about 30 MHz, and the

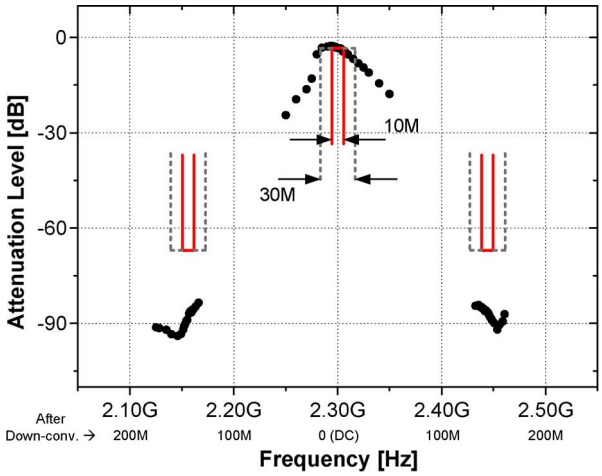

Fig. 15. Attenuation level of first null point on each side.

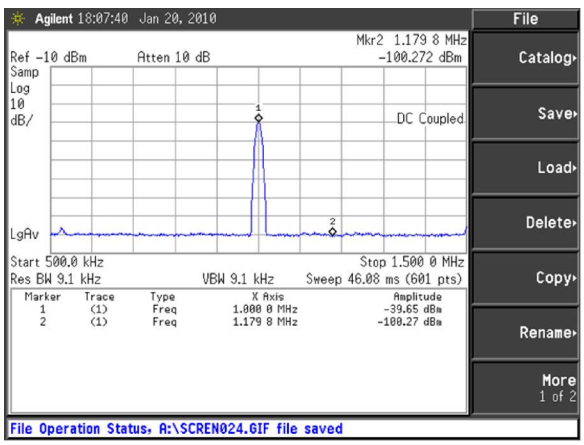

Fig. 16. Spectrum analysis for an input of −65 dBm (@ 2.301 GHz)/25 dB gain.

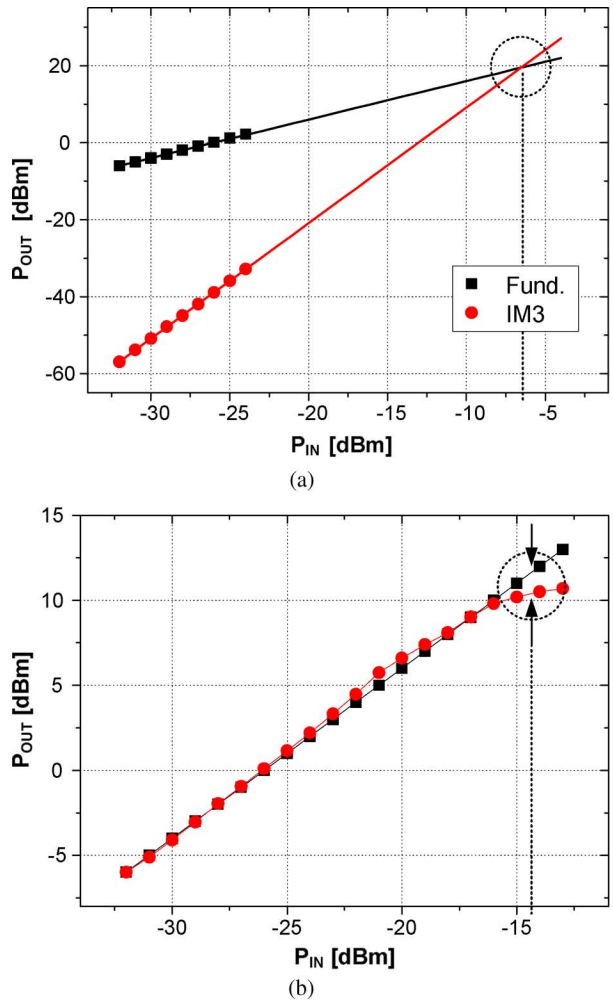

Fig. 17. Measurement result of (a) 2-tone test for $\mathrm{IIP_3}$ and (b) 1-tone test for $\mathrm{P_{1dB}}$.

attenuation bandwidth at the harmonics is wider than 30 MHz. Higher order harmonic components are attenuated well below the system requirement because of the $sinc^2$ function-type filtering response of the DT filter and the *RC* low pass filtering.

The system noise figure is calculated using the spectrum shown in Fig. 16. The measurement includes an external LNA and a single-to-differential SAW filter. A single-tone input of −65 dBm at 2.301 GHz is amplified and down-converted to the 1 MHz baseband through the receiver front-end. The resolution bandwidth of the spectrum analyzer is 9.1 kHz. For the maximum RF gain, the noise figure is obtained using the following equations:

$$\begin{aligned} NF_{SSB} &= CNR_{IN} - CNR_{OUT} \\ &= (-65 - (-174)) - (60.62 + 10 \cdot log(9.1k)) \\ &= 8.79 \text{ dB}. \end{aligned} \tag{13}$$

Thus, the calculated NF_{DSB} is 5.79 dB. Considering the connection loss, the real noise figure is less than this value.

A two-tone test and single-tone test are conducted to measure the linearity of the designed receiver front-end. Two-tone signals at 2.302 GHz and 2.303 GHz are used as RF input, and the fundamental IF output power at 2 MHz (or 3 MHz) and IM3 power at 1 MHz (or 4 MHz) were measured. For the single-tone test, the IF output power at 2 MHz was measured with a 2.302 GHz RF input. Fig. 17(a) and (b) shows the measurement results. The in-band $\mathrm{IIP_3}$ was measured to be −6.6 dBm and $\mathrm{P_{1dB}}$ was −14.5 dBm. The measurement results for the designed digital RF receiver front-end are summarized in Table I.

V. Conclusion

In this paper, we described a digital RF receiver front-end with wideband operation capability for m-WiMAX. The designed system employs a passive sampling mixer and a DT antialiasing filter. By controlling the LO signal, the filtering response of the DT filter can be changed flexibly. The modified FIR filter architecture is further optimized to reduce the number of required clock signals, simplifying the clock generator and improving the noise performance. In particular, the NDF filter, which has no decimation effect, is able to be cascaded to the conventional FIR filter. The new filter achieves $sinc^n$ function-type filtering response and can handle a wideband signal. The new DT filter chain has an attenuation level of about 90 dB for the 8.75 MHz channel bandwidth signal used in m-WiMAX

TABLE I
MEASUREMENT RESULTS FOR THE DESIGNED DIGITAL RF RECEIVER FRONT-END FOR M-WIMAX

Parameter	Value
Gain	$0 - 30$ dB
NF_{DSB}	5.79 dB (@ max RF gain)
Bandwidth	30 MHz
Attenuation @ $n \cdot f_{S,ADC}$	90 dBc (for 10 MHz BW)
IIP_3	-6.6 dBm
P_{1dB}	-14.5 dBm
Power Consumption	26.63 mA @ 1.5-V
Active Area (without pads)	1100 μm $\times$ 800 μm

applications, and the designed digital RF receiver front-end can process a signal with the maximum 30 MHz channel bandwidth.

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