Envelope-Tracking CMOS Power Amplifier Module for LTE Applications

Daehyun Kang, Byungjoon Park, Dongsu Kim, Jooseung Kim, Yunsung Cho, and Bumman Kim, *Fellow, IEEE*

***Abstract*—An envelope-tracking (ET) CMOS power amplifier (PA) is fabricated using a 0.18-μm CMOS process. The module containing the supply modulator, the PA, and the output transformer is implemented on a printed circuit board (PCB). The CMOS PA employs the second and third harmonic controls at the input and the second harmonic short at the output for improved linearity. The impact on the nonlinearity of the cascode differential structure is studied and optimized. A proposed output transformer on the PCB minimizes the loss and enhances the efficiency of the PA. The ET on the gate of the common gate transistor is proposed to achieve high linearity and efficiency without using a digital pre-distortion technique. For a long-term evolution (LTE) signal at 1.85 GHz with a 10-MHz bandwidth and a 16QAM 7.5-dB peak-to-average power ratio, the ET CMOS PA module achieves a power-added efficiency of 34%, an error vector magnitude of 2.8%, and an adjacent channel leakage ratio of -34.2 dBc at an average output power of 26 dBm. The ET operation reduces the total current consumption by 10% to 34%, according to the power level, over that of the standalone PA for the LTE signal.**

***Index Terms*—CMOS, efficient, envelope tracking (ET), linear, handset, power amplifier (PA), long-term evolution (LTE).**

I. Introduction

THE functionalities of both personal computers and mobile phones have been converging to a hand-sized smart phone. Higher-speed wireless communications are needed for a rapid processing of the large amounts of data. Efficient circuits and a battery with larger capacity are also demanded to handle the increased power consumption. The cost and size of the smart phones are essential features of this consumer product. Efforts to overcome the issues through improvements in the efficiency, speed, cost, and size of each element of a smart phone design are currently underway. Among the elements, power amplifiers (PAs) are one of the bottlenecks for increasing efficiency and reducing the cost and size of the smart phones.

The long-term evolution (LTE) infrastructure standard of mobile phones is currently being established, and the phones are beginning to support the LTE because of large demand on the high data-rate service. However, the high data rates result in large signal bandwidths (BWs) and high peak-to-average-power ratios (PAPRs). In particular, the high PAPR signal reduces the efficiency of PAs at a low average output power level because the supply voltage provided to the PAs is fixed and the output load is optimized only for the peak instantaneous power.

There are several techniques to enhance efficiency of the PAs for amplification of the high PAPR signals. The Doherty technique modulates the load impedance using a quarter-wavelength transformer for both the back-off power and peak power [1], [2]. The technique that uses reconfigurable output networks according to the power level can also enhance the efficiency of the high PAPR applications [3]. However, these techniques are sensitive to RF BWs and require complex output matching networks, which produce loss. The switched-capacitor technique introduced in [4] can maximize the load modulation effect by switching power cells on and off, but it has difficulty in generating high power appropriate for cellular applications because the fast switching MOSFET has a low breakdown voltage. Outphasing can also achieve a high efficiency at the back-off power [5], [6], but it has a limited dynamic power range and requires a complex power combining network. Envelope elimination and restoration (EER) and envelope tracking (ET) improve the efficiency by modulating the supply voltage of the PA. Conventional EER structures are nonlinear due to the delay mismatch between the amplitude and phase paths; furthermore, they encounter the severe problem of a large input power leakage at a low output operation [7]–[9]. The ET technique is less sensitive to the delay mismatch [10]–[14] and enables linear operation by utilizing a linear PA and supply modulator without using any additional linearization techniques [15], [16]. Therefore, the ET technique is applied in this paper because of its advantage of multimode/multiband functionality [17].

In mobile handset applications, an RF integrated circuit (RFIC) and baseband integrated circuit (IC) chips are being integrated onto a single die to reduce its size and cost. However, PAs are typically based on GaAs processes because of their higher reliability and performance. Eventually PAs will be integrated onto either CMOS processes along with RFICs or silicon-on-insulator (SOI) processes along with switches/duplexers to reduce the cost and size of the device. The silicon substrate has the drawbacks of lower breakdown voltage, no back via-hole for the ground, higher saturation voltage (i.e.,

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D. Kang is with the Broadcom Corporation, Matawan, NJ 07747 USA (e-mail: daehkang@gmail.com).

B. Park and Y. Cho are with the Division of Information Technology Convergence Engineering, Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk 790-784, Korea.

D. Kim is with Samsung Electronics, Suwon, Gyeonggi 443-742, Korea.

J. Kim is with the Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk, 790-784, Republic of Korea

B. Kim is with the Division of Information Technology Convergence Engineering and the Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk 790-784, Korea.

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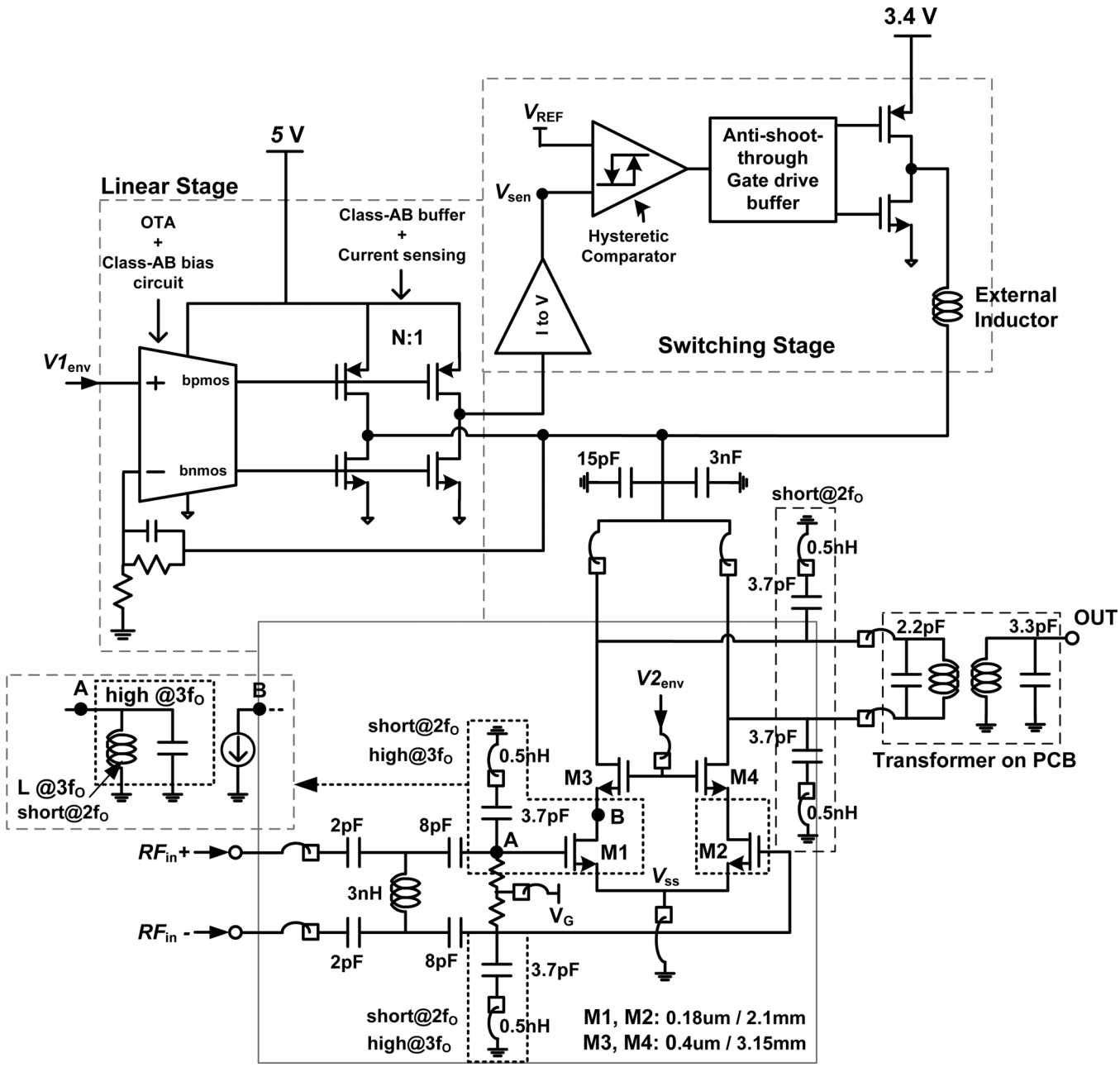

Fig. 1. Schematic of the ET CMOS PA with the supply modulator.

knee voltage), larger loss and are more nonlinear compared to their III–V counterparts. Even if the SOI process mitigates the loss in the substrate through the use of a high-resistivity substrate beneath the buried oxide, the other issues must be addressed at the circuit level as in bulk CMOS processes [18]–[21]. A cascode structure mitigates the problem of the low breakdown voltage [22]. The use of an output transformer helps solve the problems of no back via-hole and higher saturation voltages [23]. A virtual ground point at the source provides the effective grounding point and boosts the RF gain. The voltage combination increases the output load impedance of the transistors. The main nonlinearity of CMOS PAs caused by the input capacitance variation can be improved by a second harmonic control [24] or the capacitor compensation technique [25]. Although the second harmonic short circuits at the output are commonly employed to improve the linearity [18], [20], [24], [25] and efficiency [26] of CMOS PAs, the importance of the input second harmonic control on the linearity has been overlooked.

In this paper, we analyze the contribution of the common gate (CG) transistor in the cascode structure for generation of the nonlinearity and shows the importance of the second harmonic short circuits at both the input and output. The impact of the third harmonic control at the input is also studied. To design a CMOS PA that is sufficiently competitive compared to HBT PAs, we propose a design of a low-loss transformer on the PA module. Moreover, the ET technique is employed to overcome the inherently low efficiency of the CMOS PAs. The paper is organized as follows. Section II shows the improvement of the linearity in a CMOS PA using the harmonic control circuits and the

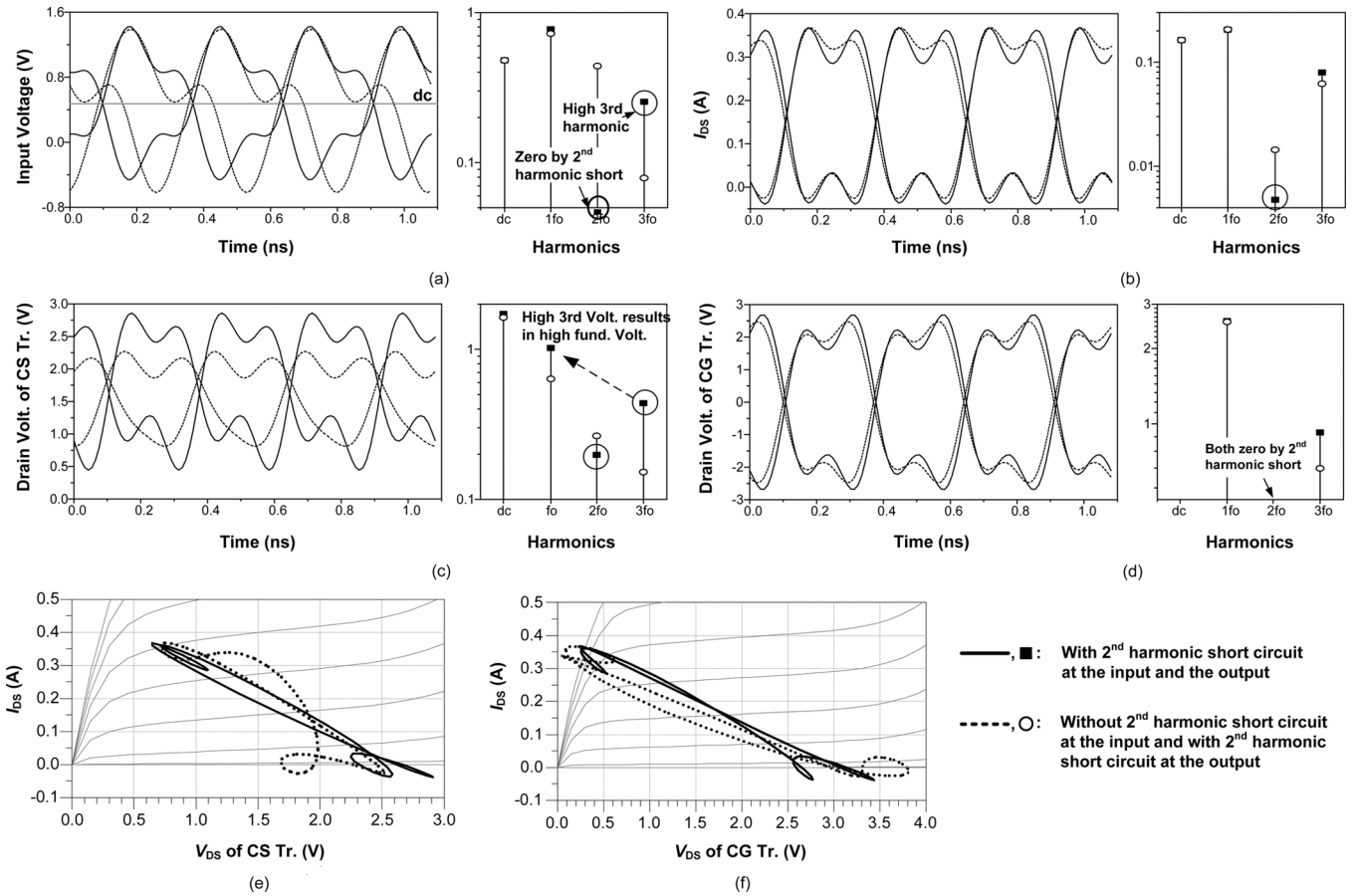

Fig. 2. (a)–(d) Simulated voltage and current waveforms of the cascode transistor and their harmonics components of the waveforms. (e) Load line in the CS transistor. (f) Load line in the CG transistor.

design of an output transformer to minimize losses. Section III describes the configuration of a hybrid switching supply modulator, and addresses the issues on the ET operation. Section IV shows the implementation and measurement results.

II. Design of CMOS PA

Fig. 1 is a schematic of the ET transmitter with a CMOS PA and a hybrid supply modulator [10]–[12]. The PA utilizes a single stage and differential structure to minimize the source degeneration. The 0.18-μm thin-oxide and 0.4-μm-thick oxide transistors are stacked to create a cascode structure that protects against the breakdown. In addition, harmonic control circuits are employed at the input and output of the amplifier.

A. Harmonic Control Circuit to Improve Linearity of the PA

The previous literature [24] focuses on the nonlinearity of common source (CS) transistors in CMOS PAs, and the authors in [28] describe that the AM–PM distortion is mainly caused by the nonlinearity of $C_{\rm gd}$ in the CG stage. In this section, we further analyze the contribution of the CG transistors to harmonic generation in the cascode structures.

The capacitance between the gate and source of the transistor increases with increasing the voltage across the terminals. The capacitance between the gate and drain of the transistor also increases, and this variation is more significant because the voltage at the drain is amplified, but the polarity is reversed compared to the voltage at the gate. Therefore, the capacitance at the higher level of the input voltage is larger, and the capacitance at the lower level is smaller. These nonlinear capacitances distort the sinusoidal input voltage waveform. The second harmonic control circuit at the input compensates for the distorted input signal generated by the nonlinear input capacitances of the transistors, resulting in more linear operation.

The second harmonic short circuit at the output eliminates the second harmonic voltage, thereby reducing the up-conversion of the component to the third-order intermodulation distortion (IMD3) and fifth-order intermodulation distortion (IMD5) and improving the efficiency of the devices. Note that the differential structure merely eliminates the even harmonic components at the combining output, but does not reduce the IMD3 or IMD5 because the intermodulation distortions (IMDs) can be generated from the second and third harmonic power trapped at the drain. A short-circuited third harmonic trap will also improve linearity by reducing the third harmonic, which is one of the components generating the IMD5, but its contribution is smaller than that of the second harmonic control circuit because the third harmonic is significantly lower than the second harmonic component.

A simulation is conducted to verify the effect of the second and third harmonic control circuits. The voltage and current waveforms are shown with their harmonic components in Fig. 2. Two CMOS PAs with and without the second harmonic control circuit at the input have the same ideal output transformer to clarify the effect of the control circuits. Both PAs have the

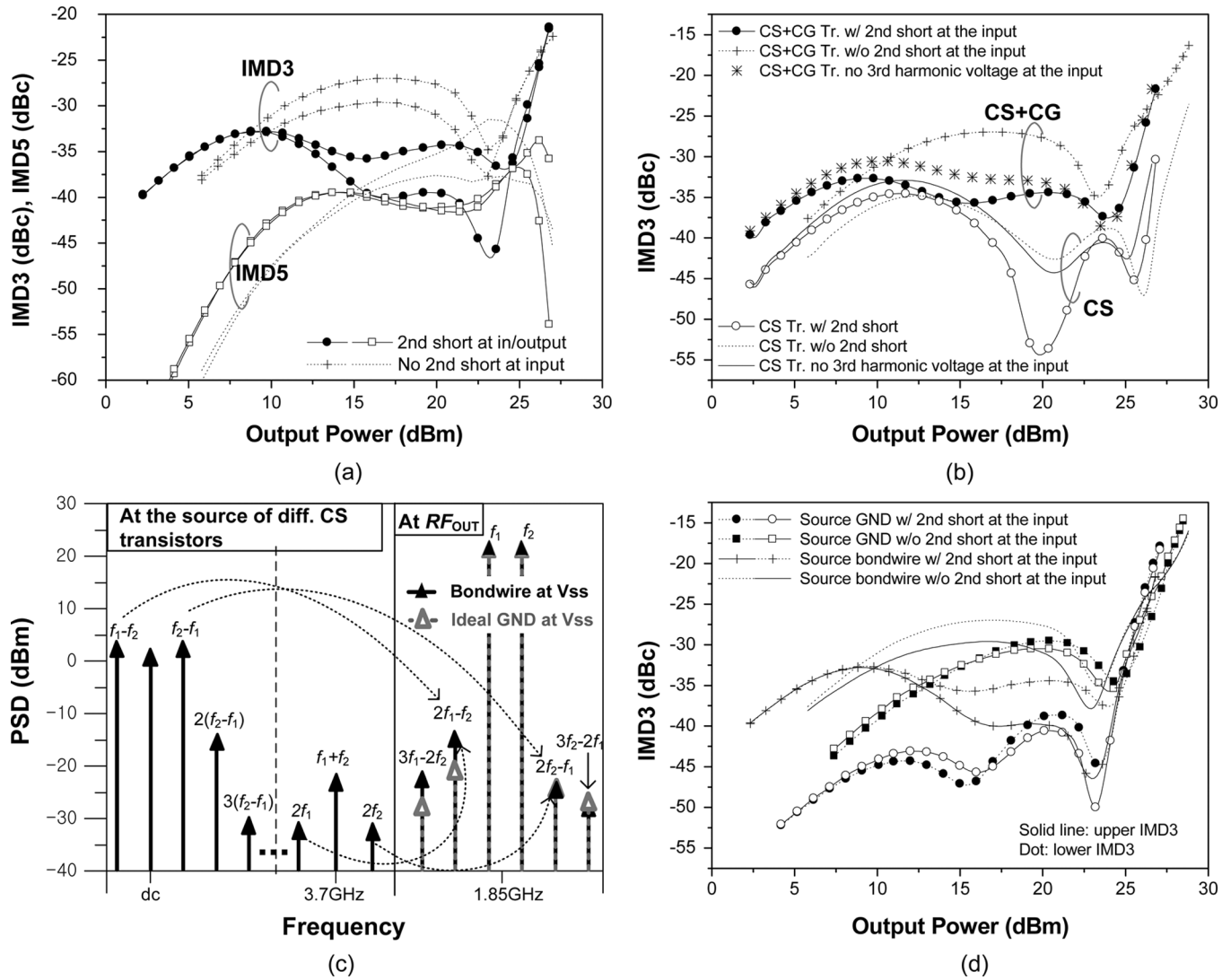

Fig. 3. (a) Comparison of the simulated IMD characteristics of the PA with/without the second harmonic control circuits at the input. Both PAs have the second harmonic control circuits at the output. (b) Contributions of the CS and CG transistors to the distortion in the cascode structure. The impact of the third harmonic on IMD3 is also shown in the plot. (c) Simulated intermodulation power spectral density (PSD) at the output power of 23 dBm for the case with the second harmonic short at the input. (d) Reduced IMD3 imbalance by an ideal ground at the source terminal of differential CS transistors.

second harmonic control circuits at the output and the stability factor K over 1.5 from 0 to 10 GHz. The drain voltage of the cascode structure is set to 3.5 V, and the gate voltage of the CS and CG transistors are set to 0.48 V and 2.3 V, respectively. The waveforms are probed at an output power of 26 dBm in a continuous wave (CW) simulation. A capacitor of 3.7 pF and an inductor of 0.5 nH are used in this design to resonate at the second harmonic frequency of 3.7 GHz. The input impedance of the differential structure is matched to 50 Ω and the load impedance of the single cascode structure is set to 12.5 Ω.

The harmonics of the PAs are generated by the nonlinear intrinsic capacitors and nonlinear dependent current source in the equivalent model of the transistor. The triode region of the transistor also contributes to the nonlinearity. The cascode structure is generally more nonlinear than a single CS structure because it has more nonlinear sources in the stack of the two transistors.

Figs. 2 and 3 show the impact of the CG transistor on the linearity of the PA. The input voltage waveform of the PA without the second harmonic control circuit at the input in Fig. 2(a) is highly distorted and has a large conduction angle on the upper dc level, which is caused by the second harmonic component generated by the nonlinear input capacitance. The second harmonic component of the input voltage is amplified and converted to the output current and drain voltage of the CS transistor. As shown in Fig. 2(b) and (c), the second harmonic components in the drain voltage and current of the CS transistor are larger for the case without the second harmonic control circuit at the input. The second harmonic components are mixed with the fundamental and third harmonic components due to the nonlinear gm of the CG transistor, thereby, generating the third-order intermodulation (IM3) and fifth-order intermodulation (IM5), respectively. Moreover, the CG transistor, which uses a thick oxide gate, has a higher saturation voltage than the CS transistor with a thin oxide. The higher saturation voltage clips the voltage waveform and generates larger nonlinearity. Thus, the PA without the second harmonic short circuit generates more IMD components than the PA with the circuit, as shown in Fig. 3(a).

The second harmonic short circuit at the input plays a role of providing a third harmonic open circuit since the series of the inductor and capacitor is equivalent to an inductor (0.27 nH) at the third harmonic, which can resonate out the average input capacitance (2.9 pF) of the CS transistor. Therefore, the large third harmonic component shown in Fig. 2(a) is in-phase with the fundamental voltage, but it becomes out-of-phase at the drain of CS transistor, thereby squaring the drain voltage of CS and increasing the magnitude of the fundamental voltage, as shown in Fig. 2(c). The higher fundamental drain voltage of CS results in lower voltage swing at the CG transistor, which has higher knee voltage, thereby ensuring the linear operation, as shown in Fig. 2(e) and (f). The voltage swing without the second harmonic short circuit hits the triode and cutoff regions of the CG transistor harder than that with the control circuit.

Fig. 3(b) shows the contributions of the CS and CG transistors to the distortion of the cascode structure. The IMD3 curves at the drain of the CS transistor with and without the second harmonic control circuits are drawn in the figure. The worst IMD curve between the upper and lower IMDs is selected for the plot. The IMD3 levels of the CS stage, before the signal passes through the CG transistor, are below -35 dBc and have significant sweet spots in both cases. However, the IMD3 characteristics deteriorate after passing through the CG transistor. The IMD3 is degraded more when the second harmonic components of the voltage and current at the CS transistor is larger. The impact of the high third harmonic input voltage on the IMD3 is also shown in the plot when the third harmonic voltage is set to near zero by an additional capacitor while maintaining the same fundamental and second harmonic voltages, which results in approximately 5 dB/1 dB higher IMD3 in the mid/high-power region, respectively. Consequently, the second harmonic control at the input of the cascode structure significantly improves the linearity by reducing the second harmonic components between the CS and CG transistors, and the resulting third harmonic control also helps improve linearity by ensuring the voltage swing in the linear region.

It is worthwhile to discuss the cause of the imbalance of the upper and lower IMD3s. The imbalance is commonly caused by the memory effect that $f_2 - f_1/f_1 - f_2$ and $2f_1/2f_2$ components generated in the past by the second-order distortion are mixed with f_2/f_1 components and added to the third-order interaction terms of $2f_2 - f_1/2f_1 - f_2$ having different phases, which results in the different magnitudes of the upper and lower IMD3s. The method to minimize the memory effect is well known to use a coupling capacitor for the $f_2 - f_1$ component at the drain/collector terminal. Due to no grounding back-via, however, CMOS processes introduce an additional source of the memory effect at the source terminal of transistors, which is connected to the ground using bond-wires. As shown in Fig. 3(c), the $f_2 - f_1/f_1 - f_2$ and $2f_1/2f_2$ components generated by the second-order distortion are trapped at the source terminal, leading to the IMD3 imbalance at the output port. The $f_2 - f_1/f_1 - f_2$ are 35 dB larger than the $2f_1/2f_2$ components, which are reduced by the second harmonic short circuits at the gate and drain terminals. The phases of the upper and lower IMD3 are measured in simulation to be 1° and -30°, respectively, showing that the vector summations with the different phases causes the IMD3 imbalance. An ideal ground at the source terminal removes the IMD components, reducing the IMD3 imbalance at the output port. In a real implementation, a flip-chip process could minimize the $f_2 - f_1/f_1 - f_2$ components, which are the main contributor to the memory effect. Fig. 3(d) shows the reduced IMD3 imbalance significantly by the ideal ground at the source terminal of the differential CS transistors for both the cases with and without the second harmonic short circuits. In this simulation, the gate bias is adjusted to optimize the PA without the source inductance such that the quiescent current is increased from 41 to 56 mA.

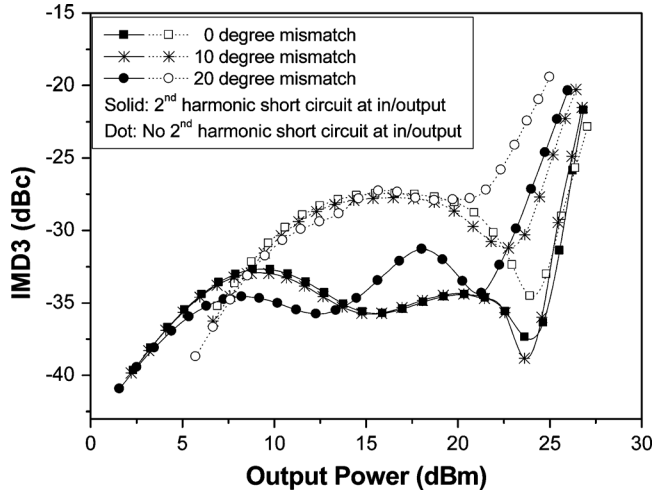

Fig. 4. Simulated IMD3 due to the phase mismatch of the output transformer on the IMD3 characteristics in the simulation.

The linearity improvement concepts for a single-ended cascode structure can be applied to the differential structures. For CMOS PAs, the differential structures are employed to minimize the source degeneration. Ideally, the even harmonic component of the drain voltage is a common mode and rejected by the output transformer, but without a proper even harmonic termination, the harmonic can be trapped and interacts with the fundamental, generating the third harmonic distortion. In practice, the transformer is not always symmetric with 180° out of phase, but rather has some phase mismatch. The second harmonic short circuits at the input and output help the PA to be insensitive to the phase mismatch of the output transformer, as plotted in Fig. 4. The IMD3 characteristics and linear output power are almost the same within the phase difference of 10° with the second harmonic control circuit, which can be achievable for the transformer.

B. Output Transformer Design

The parameters of the substrates (i.e., the loss tangent/conductivity and the thickness of the dielectrics) affect the quality (Q) factor of the lines of the output transformer and the effective coupling factor between the two lines. Once a specific substrate is chosen, the width and length of the metal line determine the self-inductance and Q of the transformers. The effective coupling k-factor is determined by the spacing between two metal lines. Fig. 5(a) depicts the layer information of the generic four-layer evaluation board that is employed for the PA module. This substrate has a higher loss tangent (0.025), thicker dielectric (42.5 μm), and higher minimum spacing (100 μm) than a

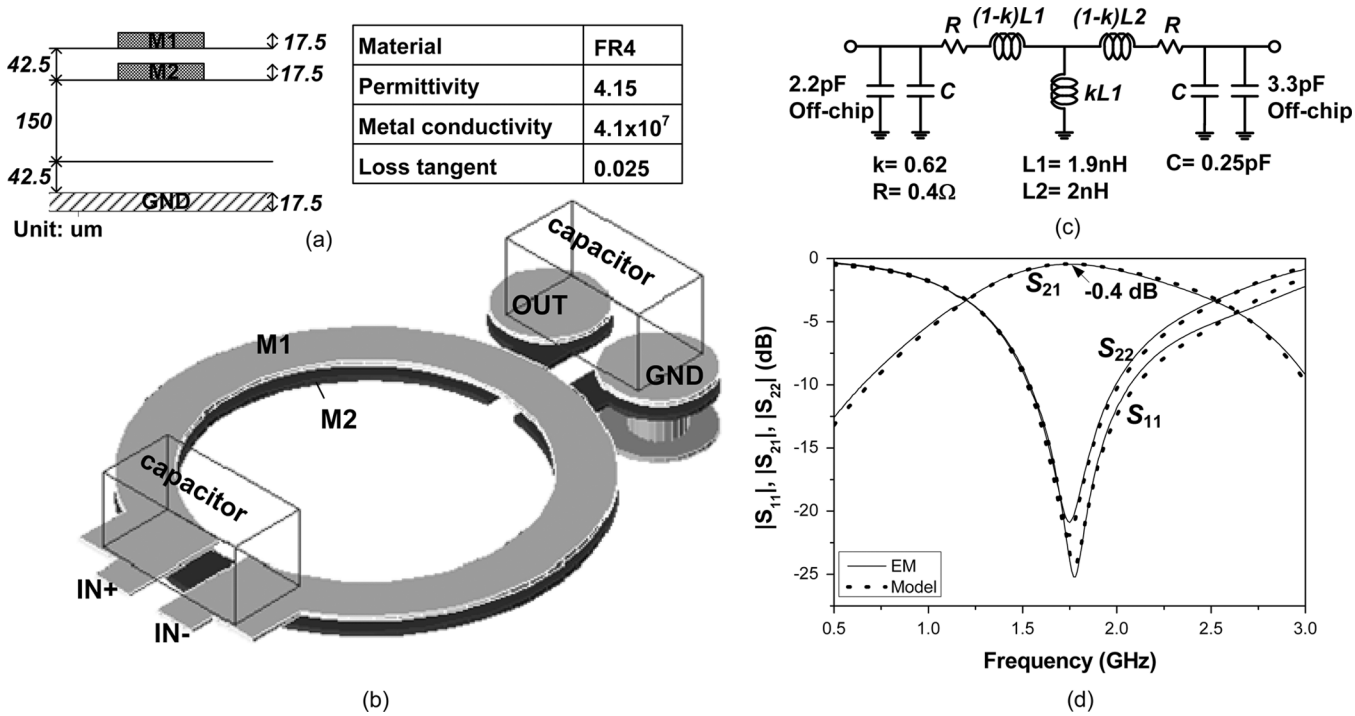

Fig. 5. (a) Layer information of the PCB used for the PA module. (b) 3-D view of the implemented output transformer. (c) Extracted equivalent circuit model of the output transformer. (d) Comparison of the S-parameters obtained from the EM simulation and equivalent circuit model of the output transformer.

laminate-based multi-layer substrate for PA modules. Fig. 5(b) shows the 3-D view of the implemented output transformer. The line is drawn as a circle to minimize the loss. The use of the two metal layers generates stronger coupling and has an advantage in size. Two off-chip capacitors (2.2 and 3.3 pF) with a size of 0.6 mm $\times$ 0.3 mm are used for impedance matching with the smaller inductance values of the primary and secondary traces.

Fig. 5(c) illustrates the extracted equivalent circuit model of the transformer. The extracted inductances are 1.9 and 2 nH for the primary and secondary traces, respectively. The primary and secondary see different inductance values in the overlay structure due to the different dielectric thickness above and below the structure and the longer leads of the secondary trace to the external capacitor. The extracted resistance is 0.4 Ω. The calculated quality factor $Q(Q = L/R)$ is 81, and the k-factor is 0.62. The extracted capacitance between the two metal lines is 0.5 pF, and it is divided into two parasitic capacitors on both the primary and secondary sides. Fig. 5(d) compares the S-parameters obtained from the electromagnetic (EM) simulation and the equivalent circuit model of the output transformer. This figure verifies that the model is well extracted. The simulated minimum loss is 0.4 dB. The input port is set to 25 Ω because the load impedance for each side of the transistors is 12.5 Ω and the output port is set to 50 Ω. The simulated loss when the circuit is perfectly matched is 0.35 dB. The loss of the transformer can be reduced further by using a laminate-based multi-layer substrate for the PA modules due to its lower loss, higher spacing/width resolution, and smaller dielectric thickness.

III. ET Operation

The supply modulator shown in Fig. 1 is revisited from the details in [17] to clearly explain the ET operation. The supply modulator consists of a linear stage and a switching stage. The linear stage functions as a voltage-controlled voltage source in which the output voltage follows the input voltage. The linear stage is comprised of a folded-cascode operational trans-conductance amplifier for a large BW and a high gain, as well as a class-AB biased CS buffer to produce a large current for rail-to-rail operation. The switching stage operates as a dependent current source that provides most of the currents to the output. A current-sensing circuit monitors the current flow at the output of the linear stage, and a hysteretic comparator controls the state of the switching stage in accordance with the sensed currents. The switching frequency of the switch stage depends on the width of the hysteresis, the BW of the envelope signal, and the value of the output inductor. The conduction and switching losses are considered to determine the size of the switches.

In this design, a boost converter is assumed to be employed in the linear stage, thereby, generating a constant voltage of 5 V to supply the linear stage and to boost the output voltage swing of the linear stage to the range from 0.5 to 4.5 V. The switch is directly driven by the battery to achieve a higher level of efficiency. Consequently, the boosted supply modulator is insensitive to the battery depletion, which helps to maximize the performance of the PA at all battery conditions, realizing the power management capability [27].

To minimize the impact of the switching noise generated by the supply modulator, the linear and switching stages are isolated by the deep N-well and the P+ guard ring in the die of the supply modulator. Not only the dies, but also the interlock of the supply modulator and PA are paid attention to in order to minimize the switching noise, which is approximately 7 MHz even though the switching noise spreads out to the wider frequencies due to the hybrid type modulator. A 15-pF capacitor, which is

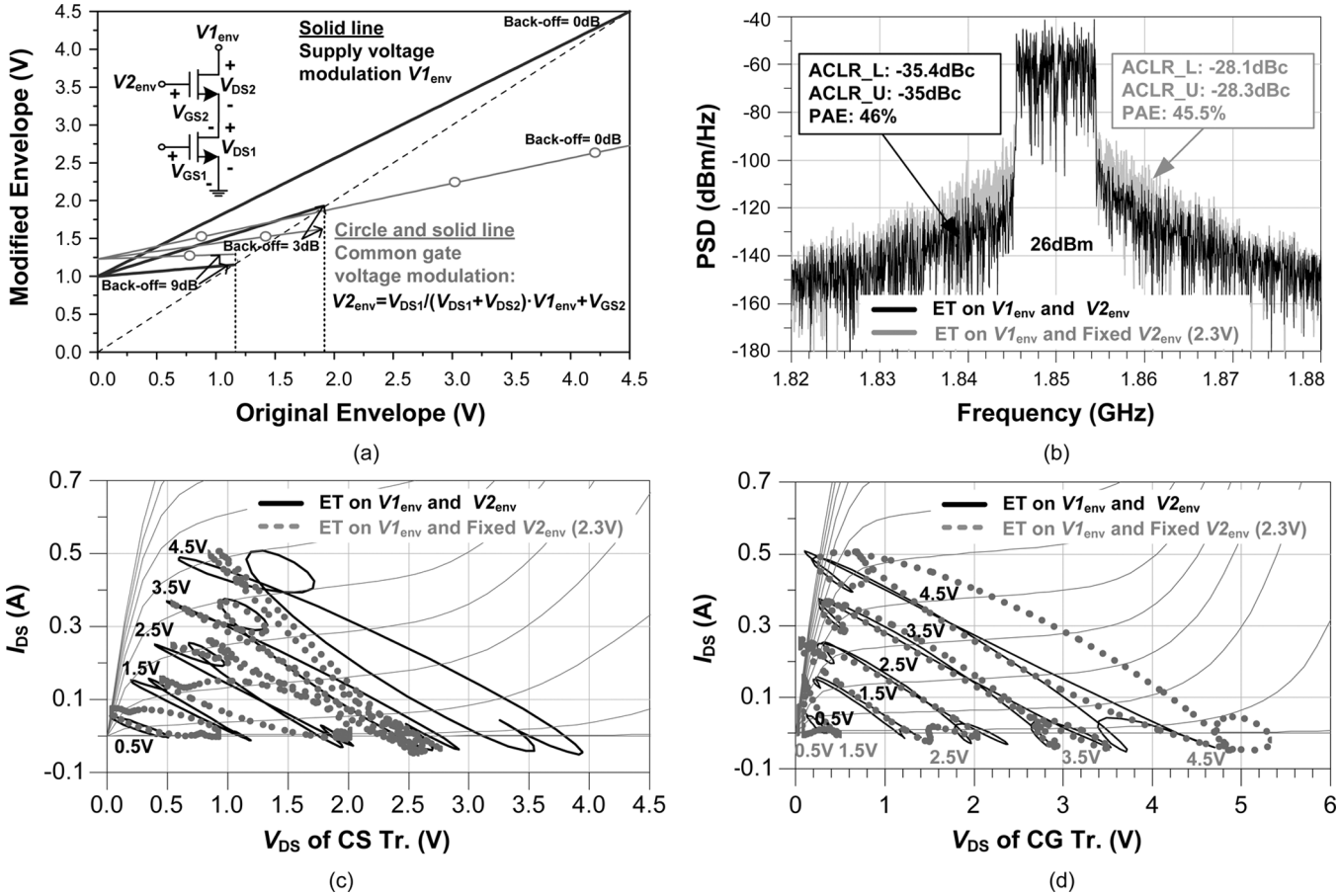

Fig. 6. (a) Envelope-shaping function for the drain and gate voltages of the CG transistor. (b) Simulated ACLRs for the ET on $V1_{\rm env}/V2_{\rm env}$ and $V1_{\rm env}$ only. (c) Load lines of the CS transistor for the ET and the fixed voltage of $V2_{\rm env}$, respectively. (d) Load lines of the CG transistor.

almost zero impedance at 1.85 GHz, is connected at the junction to ensure the PA's RF output matching to be consistent regardless the connection of the supply modulator, and a 3-nF capacitor is used to suppressed the out-band noise induced from the supply modulator. A few nanofarad capacitor could be handled by the BW enhanced technique of the supply modulator, which results in 100-MHz BW with a 70° phase margin by adding a zero at the feedback path of the linear amplifier [30].

To further enhance the efficiency of the ET PA, the idea proposed in [31] is employed in this work. The higher gate bias of the CS transistor increases the quiescent current of the PA and saves the waste of the sinking current in the linear stage of the supply modulator, which results in higher efficiency of the modulator and better linearity of the PA in the high-power region.

Moreover, this work proposes to utilize the ET on the gate of CG transistors, as shown in Fig. 6(a). There is little literature presenting ET operation for cascode transistors. Hassan, *et al.* [32] did not focus on the linearity issue of the ET PA since digital pre-distortion (DPD) was employed. Li *et al.* [33] employed the self bias structure for the gate of CG transistor to track the envelope, as well as the drain, but the gate voltage is always lower than the collector voltage. The CG voltage $V2_{\rm env}$ has to be greater than $V1_{\rm env}$ around the boundary of the saturation region since $V_{\rm GS2}+V_{\rm DS1}$ is greater than $V_{\rm DS1}+V_{\rm DS2}$ in the region. In this work, the values of $V2_{\rm env}$, $V_{\rm DS1}$, and $V_{\rm DS2}$ are selected to achieve the highest efficiency at a supply voltage of 2.8 V, as well as good linearity over all the power ranges. For

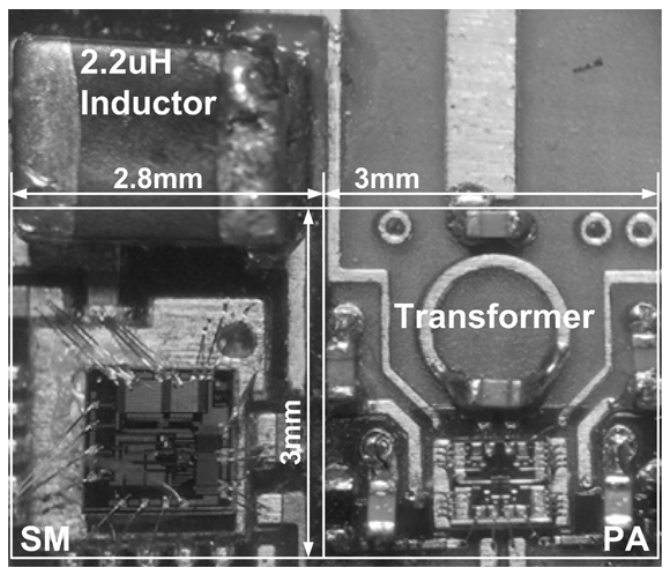

Fig. 7. Photograph of the ET PA module including the test chips of the PA and the supply modulator in a 0.18-μm CMOS process.

this purpose, the shaping function of $V2_{\rm env}$ is determined for a sweep of $V1_{\rm env}$ from 1 to 4.5 V, and the relationship is

$$V2_{\rm env} = V_{\rm DS1}/(V_{\rm DS1}+V_{\rm DS2})\cdot V1_{\rm env} + V_{\rm GS2} \qquad (1)$$

where $V_{\rm DS1}/(V_{\rm DS1}+V_{\rm DS2})$ and $V_{\rm GS2}$ are 3/7 and 0.8 V, respectively. The envelope of the signal $V1_{\rm env}$, which is the same

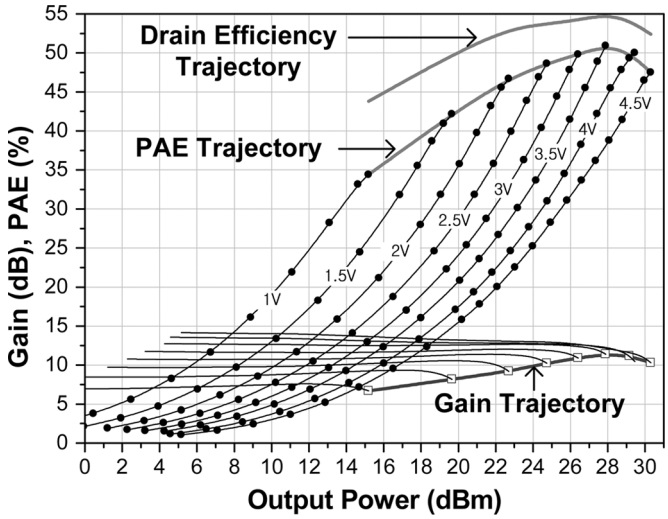

Fig. 8. Measured 1.85-GHz CW performance of the PA obtained by sweeping the drain voltage from 1 to 4.5 V and the CG voltage from 1.23 to 2.73 V.

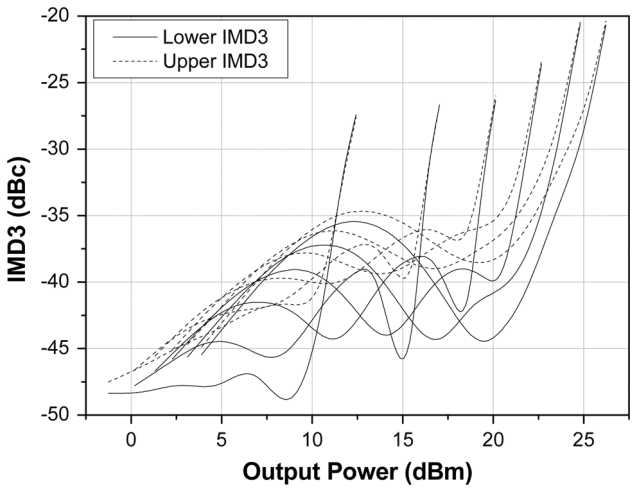

Fig. 9. Measured IMD3 of the PA using a 10-MHz-spacing two-tone CW signal. The drain voltage is swept from 1 to 3.5 V and the CG voltage from 1.23 to 2.3 V.

as the supply voltage to the PA itself, is modified linearly with a minimum value of 1 V and a variable slope of the envelope according to the power level because the PA under ET operation has large AM/AM and AM/PM distortions at a low supply voltage because the output capacitance and saturation voltage effects are increased.

Fig. 6(b) shows the simulated spectra at an output power of 26 dBm with and without the ET of $V2_{\rm env}$. The efficiencies are almost the same in both cases, but linearity is significantly improved by 7 dB in E-UTRA adjacent channel leakage ratio (ACLR) for the ET of $V2_{\rm env}$. It is worthwhile to note that the upper and lower ACLRs are almost identical because the delay between the ET and the RF paths is adjusted to minimize the ACLR imbalance of the CMOS PA itself, shown in Fig. 3(d). The consistent load lines through the ET operation of both $V1_{\rm env}$ and $V2_{\rm env}$ ensure the linear ET operation, as shown in Fig. 6(c) and (d). For the fixed $V2_{\rm env}$, the load impedance of the CS increases when the supply voltage decreases, causing nonlinearity in the CS transistor. The CG transistor also suffers from nonlinearity because the voltage swing decreases at a lower supply voltage due to the fixed $V2_{\rm env}$.

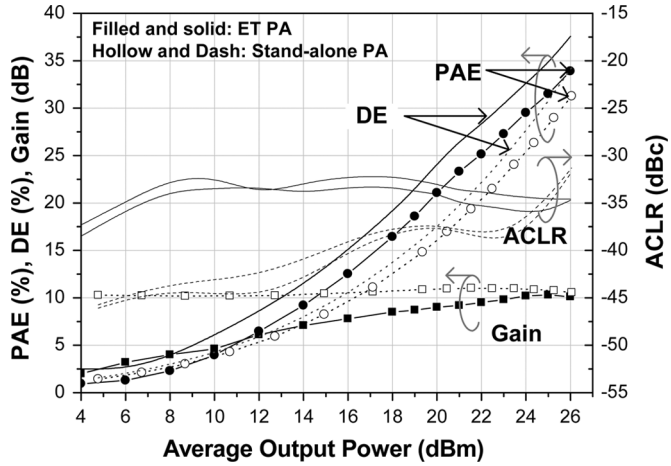

Fig. 10. Measured performances of the ET PA and standalone PA at 1.85 GHz for a 10-MHz BW, 16QAM, 7.5-dB PAPR LTE signal.

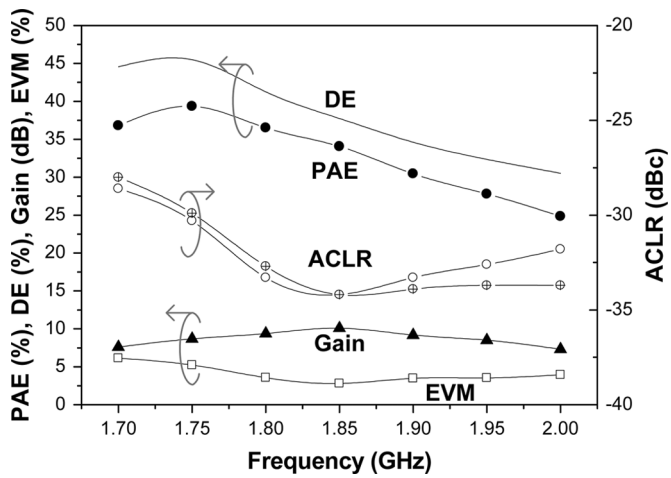

Fig. 11. Measured performances of the ET PA between 1.7–2 GHz at an output power of 26 dBm for the 10-MHz BW, 16QAM, and 7.5-dB PAPR LTE signal.

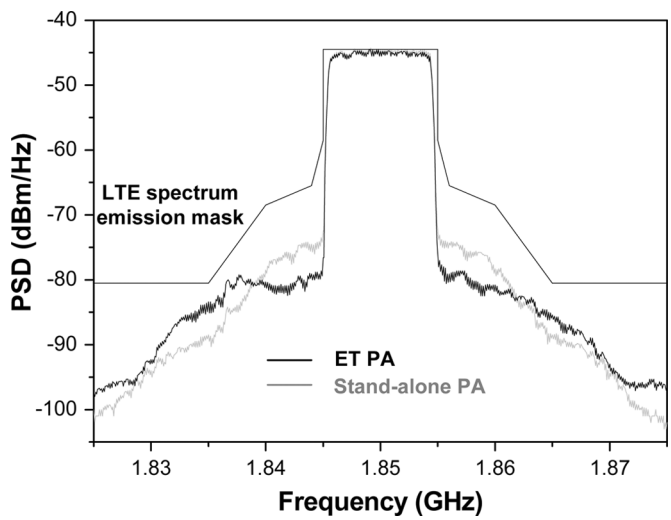

Fig. 12. Measured spectra of the ET PA and standalone PA at an output power of 26 dBm for the LTE signal.

IV. Implementation and Measurement Results

The PA and modulator are fabricated using a 0.18-μm CMOS process and are 0.7 mm $\times$ 0.95 mm and 1.3 mm $\times$ 1.3 mm in size, respectively. The inductors for the second harmonic control circuits are implemented using bond-wires to minimize the

TABLE I
COMPARISON OF THE ET PA MODULE WITH THE STATE-OF-THE-ART PAS

		[18]	[21]	[30]	[35]	[36]	[37] Commercial Avago PA	[32] ET PA	[33] ET PA	[39] ET PA	**This Work**	
											Stand-alone PA	**ET PA**
Technology		90nm CMOS	65nm CMOS	0.18um CMOS	0.18um CMOS	90nm CMOS	InGaP HBT	0.35um CMOS SOS	0.35um SiGe BiCMOS	65nm CMOS	**0.18um CMOS**	**0.18um CMOS**
Freq (GHz)		2.3	2.35	2.4	1.95	0.93	0.707	0.782	1.9	2.4	**1.85**	**1.85**
Application	**CH BW (MHz)**	10	20	20	3.84	10	10	10	5	20	**10**	**10**
	PAPR (dB)	-	-		3.5	6.9	-	6.6	7.5	~10	**7.5**	**7.5**
	Modulation	16QAM WiMAX	64QAM WLAN	64QAM WLAN	QPSK WCDMA	16QAM LTE	LTE	16QAM LTE	16QAM LTE	64QAM WLAN	**16QAM LTE**	**16QAM LTE**
Supply (V)		3.3	3.3	3.3	3.4	2	3.4	-	5.5	1.2	**3.5/4.5**	**5**
Psat (dBm)		30.1	33.5	34	30.5	29.4	-	-	-	-	**28/30.2**	**-**
PAE @Psat (%)		33	37.6	34.9	42.1	24	-	-	-	-	**51/48**	**-**
Pavg (dBm)		22.7	23.9/ 26.4*	23.5	28	25.1/26*	27.5	27.5/29.3*	26.1	22.7	**23.8/26**	**26**
PAE@Pavg (%)		12.4	14/22*	~13	36.4	15/17*	37.1	46.6/50.1*	35		**31.8/31.2**	**34.1**
ACLR (dBc)		-	-	-	-35	-	-36	-29.3/-46.5	-	-	**-32.5/-32**	**-34.2**
EVM (%)		5.62	5.62	5.62	-	5.62	-	10.1/4*	4.2	5%	**3.2/3.97**	**2.8**
Silicon Area (mm x mm)		2.1 x 2.06	3 x 2	2.1 x 1.64	2.0 x 1.3	1.8 x 1.85	-	-	1.5 x 1.1	1.1 x 1.2	**0.77 x 0.95**	**0.77 x 0.95, 1.3 x 1.3**
Output Matching Network		On-chip	On-chip	On-chip	On-chip	On chip	Off-chip On-package	-	Off-chip	Off-chip On-package	**Off-chip On-package**	**Off-chip On-package**

loss. The two fabricated chips are mounted on the four-layer printed circuit board (PCB). Fig. 7 shows the PA module, which includes the output transformer with the two off-chip capacitors and occupies an area of 3 mm × 3 mm. The area of the supply modulator is less than 2.8 mm × 3 mm excluding the off-chip inductor. The gate voltage of the CG transistors is provided externally using a signal generator. The output transformer designed on this PCB can be smaller if the laminate-based multi-layer substrate is used because the minimum width/space is smaller and the k-factor is higher on the laminate. The measured loss of the output transformer is 0.5 dB.

Fig. 8 shows the measured CW performance of the standalone PA at 1.85 GHz, generated by sweeping the drain voltage from 1 to 4.5 V and the CG voltage from 1.23 to 2.73 V. The power-added efficiency (PAE) and gain of the PA under ET operation are expected to follow these PAE and gain trajectories. For a supply voltage of 2.8 V, the PAE and drain efficiency (DE) are 50% and 55%, respectively, at a CW power of 26 dBm. With the envelope-shaping function, the PAE trace under ET operation is optimized at an output power of 26 dBm. With the envelope shaping, the PA operates at the IMD sweet spot points tracked by the envelope, and the overall IMD is improved [29]. Fig. 9 shows the measured performance of the PA tested with a 10-MHz-spacing two-tone CW signal, while sweeping the drain voltage from 1 to 3.5 V and the CG voltage from 1.23 to 2.3 V.

Fig. 10 shows the measured performance of the ET PA and standalone PA for an LTE signal at 1.85 GHz with 10-MHz BW, 16QAM, and 7.5-dB PAPR. The standalone PA with a supply voltage of 4.5 V delivers a PAE of 31.2%, an error vector magnitude (EVM) of 3.97%, and an ACLR of −32 dBc at an average output power of 26 dBm. The ET operation of the CMOS PA improves the PAE by 2.8% compared to the standalone CMOS PA for the same LTE signal. The PAE of the ET PA includes the current consumption of the supply modulator. The ET PA achieves a PAE of 34%, an EVM of 2.8%, and an ACLR of −34.2 dBc at an average output power of 26 dBm. When the ET PA module is used, the total consumed current is reduced by 10% at 26 dBm, 27% at 20 dBm, and 34% at 10 dBm compared to the standalone PA. The measured switching frequency of the switching stage in the supply modulator is 7 MHz to cover the 10-MHz LTE signal. The linear amplifier has a BW of greater than 50 MHz and a dc gain of greater than 50 dB. The peak efficiency of the supply modulator is 90% and the average efficiency is 75% under ET operation for the LTE signal.

Fig. 11 illustrates the measured performance versus frequency of the ET PA between 1.7–2 GHz at an output power of 26 dBm. The maximum PAE of 40% is measured at a frequency of 1.75 GHz. The PA is optimized at a frequency of 1.85 GHz for the ACLR.

Fig. 12 shows the measured spectra of the ET PA and standalone PA at an output power of 26 dBm for the LTE signal.

The ACLR is measured with a BW resolution of 9 MHz at the center frequency and a 10-MHz offset. The ACLR of the ET PA is −34.2 dBc, which is 2 dB better than that of the standalone PA because of the sweet-spot tracking in the ET operation. The ET PA with the selected envelope-shaping function follows the IMD3 sweet spot rather than the IMD5 sweet spot. Thus, the inner skirt of the spectra improves while the outer skirt becomes a little degraded.

Table I shows a comparison of the ET PA module with the state-of-the-art PAs. The proposed ET PA module outperforms the CMOS PAs in terms of linearity and efficiency without DPD. It is clear that it cannot be a one-to-one comparison because our ET PA uses the off-chip transformer, but it is worthwhile to note that commercial cellular PAs use off-chip matching networks to minimize their loss and die size and to maximize their efficiency. The proposed ET PA shows competitive performance compared to the commercial InGaP HBT PA [37] and the SiGe BiCMOS ET PA [38] for LTE applications.

V. Conclusion

An ET CMOS PA has been fabricated using a 0.18-μm CMOS process, and a module containing the modulator and PA, including the output transformer, has been implemented on a four-layer PCB. The linearity of the cascode differential structure PA has been analyzed and improved by utilizing the second and third harmonic controls at the input and the second harmonic control at the output. The proposed output transformer on a PCB minimizes the loss and enhances the efficiency of the PA. The ET on the gate of the CG transistor is proposed to achieve high linearity and efficiency without using a DPD technique. Realistic issues on implementing the ET PA are visited and addressed. The ET CMOS PA module achieves a PAE of 34%, an EVM of 2.8%, and an ACLR of −34.2 dBc at an average output power of 26 dBm and a frequency of 1.85 GHz for a 10-MHz BW, 16QAM, and 7.5-dB PAPR LTE signal. The ET operation reduces the total current consumption by 10%–34%, according to the power level, over the standalone PA for the LTE signal.

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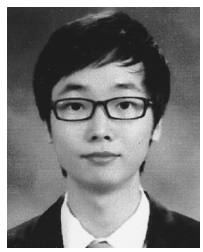
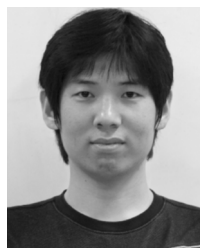
Daehyun Kang received the B.S. degree in electronic and electrical engineering from Kyungpook National University, Daegu, Korea, in 2006, and the Ph.D. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2012. His doctoral research focused on RF circuits for wireless communications, especially efficient RF TX and RF PA design.

In 2011, he was an Intern with RF Micro Devices, Cedar Rapids, IA, USA, where he designed balanced and single-ended LTE PAs. Since 2012, he has been with the Broadcom Corporation, Matawan, NJ, USA, where he is involved with mobile system designs. His current research interests include advanced transmit/receive (TX/RX) architectures for mobile communications.



Byungjoon Park received the B.S. degree in electrical engineering from Hanyang University, Seoul, Korea, in 2010, and is currently working toward the Ph.D. degree in electrical engineering at the Pohang University of Science and Technology (POSTECH), Pohang, Korea.

His research interests are CMOS RF circuits for wireless communications with a special focus on highly efficient RF transmitters and RF CMOS PA design.



Dongsu Kim received the B.S. and Ph.D. degrees in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2007 and 2013, respectively.

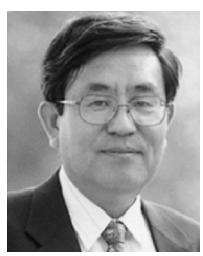
His research interests are CMOS RF circuits for wireless communications with a special focus on highly efficient and linear RF transmitter design.

Jooseung Kim received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2010, and is currently working toward the Ph.D. degree in electrical engineering at POSTECH.

His research interests are CMOS RF circuits for wireless communications with a special focus on highly efficient and linear RF transmitter design.

Yunsung Cho received the B.S. degree in electrical engineering from Hanyang University, Ansan, Korea, in 2010, and is currently working toward the Ph.D. degree in electrical engineering at the Pohang University of Science and Technology (POSTECH), Pohang, Korea.

His main interests are RF circuits for wireless communications with a special focus on highly efficient RF transmitters and RF PA design.



Bumman Kim (M'78–SM'97–F'07) received the Ph.D. degree in electrical engineering from Carnegie Mellon University, Pittsburgh, PA, USA, in 1979.

From 1978 to 1981, he was engaged in fiber-optic network component research with GTE Laboratories Inc. In 1981, he joined the Central Research Laboratories, Texas Instruments Incorporated, where he was involved in development of GaAs power field-effect transistors (FETs) and monolithic microwave integrated circuits (MMICs). He has developed a large-signal model of a power FET, dual-gate FETs for gain control, high-power distributed amplifiers, and various millimeter-wave MMICs. In 1989, he joined the Pohang University of Science and Technology (POSTECH), Pohang, Gyungbuk, Korea, where he is a POSTECH Fellow and a Namko Professor with the Department of Electrical Engineering, and Director of the Microwave Application Research Center. He is involved in device and circuit technology for RFICs and PAs. He has authored over 350 technical papers.

Prof. Kim is a member of the Korean Academy of Science and Technology and the Natioal Academy of Engineering of Korea. He was an associate editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, a Distinguished Lecturer of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S), and an Administrative Committee (AdCom) member.