Envelope-Tracking Two-Stage Power Amplifier With Dual-Mode Supply Modulator for LTE Applications

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***Abstract*—This paper presents an envelope tracking power amplifier (ET PA) using a dual-mode supply modulator for handset application. The supply modulator has a combined structure with a linear amplifier and a switching amplifier. The dual-mode supply modulator operates in high-power mode and low-power mode by providing the supply voltage of the linear amplifier of 5 and 2.5 V, respectively. For 1.74-GHz long-term evolution signal with 10-MHz bandwidth, 6.44-dB peak-to-average power ratio, and 16-quadrature amplitude modulation, the ET PA delivers a power-added efficiency (PAE) of 39.8%, an evolved universal terrestrial radio access adjacent channel leakage ratio ($\text{E-UTRA}_{\text{ACLR}}$) of −35.7 dBc, and an error vector magnitude (EVM) of 3.81% at an average output power of 27 dBm. The ET PA also delivers a PAE of 22.6% at an average output power of 18 dBm, which is 6.6% higher than that of the conventional ET PA and 13.1% higher than that of the standalone PA. The supply modulator is connected to a drive stage and a power stage of the PA simultaneously for further enhanced efficiency at a power back-off region. The dual-mode two-stage ET PA delivers a PAE of 38.1%, an $\text{E-UTRA}_{\text{ACLR}}$ of −32.9 dBc, and an EVM of 4.74% at an average output power of 27 dBm. The dual-mode two-stage ET PA also delivers a PAE of 26.3% at an average output power of 18 dBm, which is 7.8% higher than that of the conventional two-stage ET PA and 16.7% higher than that of the standalone PA.**

***Index Terms*—Dual mode, envelope tracking (ET), high-power mode (HPM), linear amplifier, long-term evolution (LTE), low-power mode (LPM), power amplifier (PA), switching amplifier, two stage.**

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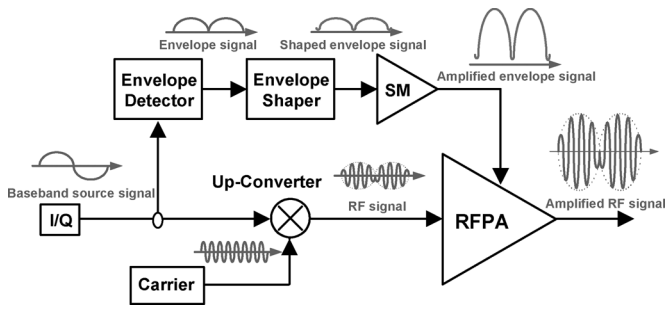

Fig. 1. Simplified block diagram of ET system.

I. Introduction

FOR FOURTH-GENERATION (4G) wireless communication systems such as Mobile-WiMAX and 3GPP long-term evolution (LTE), the signals have a high peak-to-average power ratio (PAPR) and a wide channel bandwidth. To maintain linearity for the signals with high PAPR, the power amplifier (PA) should operate at a large back-off power, in which the PA has poor efficiency. Furthermore, due to the power control strategy for 4G handset applications, the PA usually operates at a back-off power level, but the efficiency of the PA is low at frequently used power levels [1]. Therefore, the PA, which consumes a large portion of the power from a handset battery, is required to be efficient to extend the battery life. This requirement becomes even more critical for high-end mobile handsets due to the high level of integration and functionality. To improve the efficiency of the PA over the whole output power range, many techniques have been investigated [2]–[25].

An envelope tracking (ET) technique achieves the high efficiency by modulating the supply voltage of the PA. Fig. 1 shows a simplified block diagram of the ET system. An envelope signal is generated and reshaped by an envelope detector and an envelope shaper, respectively. A supply modulator amplifies the reshaped envelope signal and supplies the reshaped voltage to a RF PA. Thus, the high efficiency is maintained at the back-off power region, as shown in Fig. 2. To maximize efficiency of the ET system, not only is the efficiency of the PA important, but also that of the supply modulator. In [3] and [4], a low drop-out (LDO) regulator is employed as the supply modulator. It operates over a wide bandwidth, but is not efficient enough for high PAPR signals. In [5]–[7], a switched-mode power supply (SMPS) delivers high efficiency, but its bandwidth is too narrow to use in 4G systems such as Mobile-WiMAX and 3GPP LTE. In [8]–[20], a hybrid switching amplifier (HSA) combining the

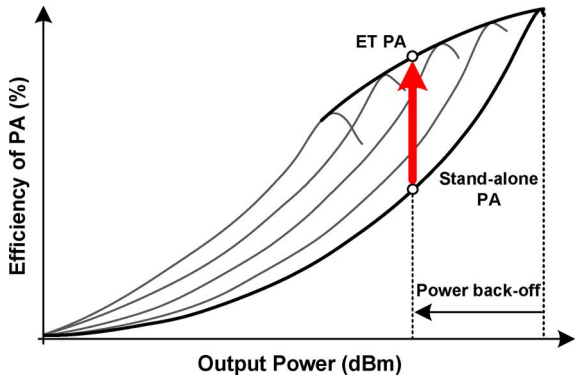

Fig. 2. Efficiency curves of standalone PA and ET PA.

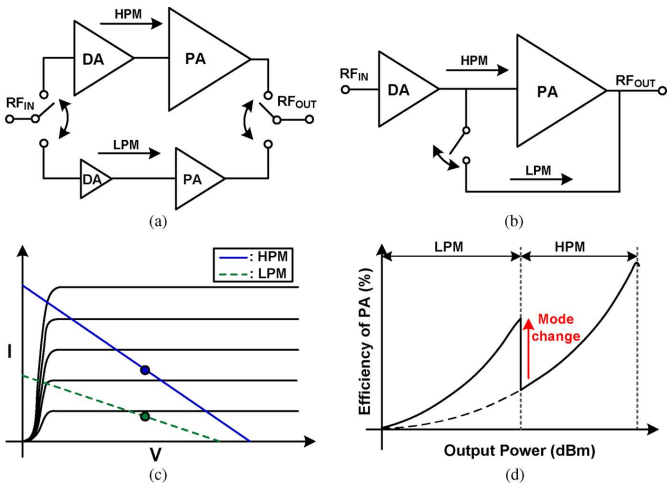

Fig. 3. Simplified block diagram of: (a) dual-mode PA and (b) bypass PA. (c) Loadline. (d) Efficiency curve.

advantages of the two modulators is used to achieve high efficiency and good linearity simultaneously. In this architecture, the switching amplifier operates slowly as a quasi-constant current source compared to a conventional SMPS, while the wideband linear amplifier regulates the output voltage and compensates the ripple current of the switching amplifier. However, the efficiency of the HSA is also low at a low-power operation.

To improve the efficiency at the low output power, many researchers have also studied the PAs with enhanced efficiency at a back-off power region, such as dual-mode PAs and bypass PAs [21], [22]. These PAs have different paths with optimized device sizes to save current under the back-off operation, as depicted in Fig. 3(a) and (b). The load impedances are optimized for multipower mode operation over two or three output power ranges, improving efficiency at the low output power. Generally, the optimum output impedance of the low-power mode (LPM) with a small device is higher than that of the high-power mode (HPM), as shown in Fig. 3(c). Depending on the output power requirement, the PA is switched between the HPM and LPM, achieving higher efficiency in the LPM. Although the PAs provide high efficiency at the maximum output power in LPM and HPM, the efficiencies at the back-off power region decrease rapidly if the PA is operated at a large back-off from its maximum output power, as depicted in Fig. 3(d). To address this limitation, we

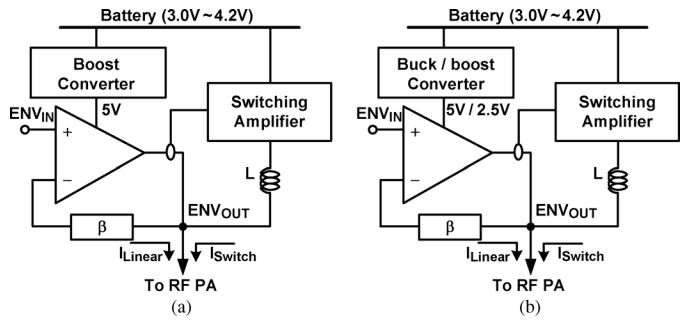

Fig. 4. Simplified block diagram of: (a) boost-mode supply modulator and (b) dual-mode supply modulator.

have developed a dual-mode supply modulator for ET operation at the HPM and LPM, further enhancing the efficiency of the RF PA over the whole low output power region. Though the ET PA with the dual-mode supply modulator is demonstrated in [12], this paper presents more detailed analyses for a dual-mode two-stage ET PA and experiment results.

The dual-mode supply modulator operates in the HPM and LPM, resulting in high efficiency at a low output power, as well as a high output power. This paper is organized as follows. Section II details the concept and effect of the dual-mode supply modulator. Section III proposes the two-stage ET PA with the dual-mode supply modulator for further enhanced efficiency in the overall output power region. Section IV presents the measurement results, and conclusions are discussed in Section V.

II. Dual-Mode Supply Modulator

A. Concept of Designed Dual-Mode Supply Modulator

For a practical operation environment, where the modulator is directly connected to a battery, a boost-mode hybrid switching supply modulator is introduced in [10] and [18], forming a power management integrated circuit (PMIC), as shown in Fig. 4(a). By boosting the supply voltage of the linear amplifier to a fixed 5 V regardless of the battery voltage variation, the PA can provide a good performance over the entire battery voltage range. Although the power consumption of the boost converter can degrade the efficiency of the ET system, the degradation is not serious because the linear amplifier provides only a small amount of the total current to the load, while the switching amplifier, which is directly connected to the battery, generates a large portion of the current. However, the 5-V supply to the linear amplifier is not optimal and can waste power for the supply modulator at a low envelope output voltage operation, as shown in Fig. 5(a). To improve efficiency of the supply modulator in the low output power region, the supply voltage of the linear amplifier is stepped down to 2.5 V, as depicted in Fig. 5(b) [12]. Fig. 4(b) shows a simplified block diagram of the dual-mode supply modulator. The supply voltage of the linear amplifier is 5 and 2.5 V for HPM and LPM, respectively. A highly efficient linear output stage without cross over distortion can be realized by a rail-to-rail push–pull class-AB configuration, as shown in Fig. 6. If the supply voltage of the linear amplifier is stepped down from 5 to 2.5 V for the low-power operation, the push–pull output stage is changed from class-AB

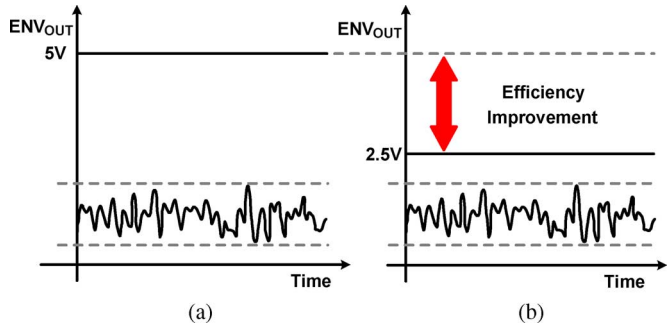

Fig. 5. (a) Low envelope output voltage generation in boost-mode supply modulator. (b) Low envelope output voltage generation in dual-mode supply modulator.

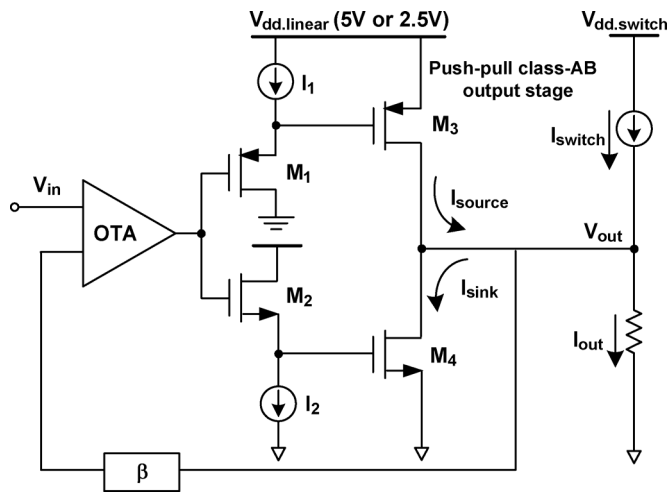

Fig. 6. Circuit topology of the push–pull class-AB output stage in the linear amplifier. (The load and switching amplifier are simplified as a resistor and a dc current source, respectively.)

state to class-B state, generating the cross over distortion and noise at the output. To maintain the class-AB operation in the low supply voltage of the linear amplifier, $V_{\rm GS}$ of floating voltage sources (M_1, M_2) should be reduced. It is possible by decreasing drive currents (I_1, I_2) or by increasing the size of floating voltage sources. If the drive current is reduced, it is difficult to drive the buffer (M_3, M_4), which is designed for a high-power operation using a large size device. To maintain the class-AB operation while driving the large size buffer, the size of the floating voltage sources is increased. For this purpose, additional operational transconductance amplifier (OTA) and class-AB bias circuits for the LPM are added in the linear amplifier.

Fig. 7 shows the architecture of the proposed dual-mode supply modulator with an RF PA. The linear amplifier operates as an independent voltage source with HPM (5 V) and LPM (2.5 V), while the switching amplifier operates as a dependent current source. Each OTA and class-AB bias circuits for the HPM and LPM are designed to achieve high efficiency without cross over distortion. These OTAs and class-AB bias circuits share the same buffer in the linear amplifier. There are no problems arising from the shared buffer because one of them is disabled by an enable pin, which is determined automatically by the supply voltage of the linear amplifier. Although the efficiency of the buck–boost converter is generally lower than that of a boost converter, the efficiency degradation is not serious because the difference between the efficiencies of the two converters is not much, and the linear amplifier does not supply the current needed at the output as much as switching amplifier does. The control stage, which is composed of a current sensing circuit and a hysteretic comparator, changes the states of the switching amplifier according to the polarity and magnitude of the sensed current from the linear amplifier to output. For the switching amplifier, the reference voltages of the hysteretic comparator are adjusted for the HPM and LPM. The enable pin for each power mode determines whether the reference voltage of the hysteretic comparator is connected to $V_{\rm ref.HPM}$ or $V_{\rm ref.LPM}$.

B. *Effect of Dual-Mode Supply Modulator*

The efficiency of the proposed supply modulator is calculated and compared with that of the conventional supply modulator. Typically, $\eta_{\rm linear}$, $\eta_{\rm switch}$, and $\eta_{\rm overall}$ can be expressed as

$$\eta_{\rm linear} = \frac{\langle V_{\rm out} \cdot I_{\rm source} \rangle}{P_{\rm dc.linear}} = \frac{\langle V_{\rm out} \cdot I_{\rm source} \rangle}{\langle V_{\rm dd.linear} \cdot I_{\rm dc.linear} \cdot 1/\eta_{\rm buck-boost} \rangle} \quad (1)$$

$$\eta_{\rm switch} = \frac{\langle V_{\rm out} \cdot (I_{\rm switch} - I_{\rm sink}) \rangle}{P_{\rm dc.switch}} = \frac{\langle V_{\rm out} \cdot (I_{\rm switch} - I_{\rm sink}) \rangle >}{\langle V_{dd.switch} \cdot I_{\rm dc.switch} \rangle} \quad (2)$$

$$\eta_{\rm overall} = \frac{\langle V_{\rm out} \cdot I_{\rm out} \rangle}{P_{\rm dc.linear} + P_{\rm dc.switch}} = \frac{\langle V_{\rm out} \cdot (I_{\rm switch} + I_{\rm source} - I_{\rm sink}) \rangle}{P_{\rm dc.linear} + P_{\rm dc.switch}}. \quad (3)$$

The terms in the above equations are depicted in Fig. 7. Ideally, the output voltage, output current, sourcing current, sinking current, and switch current of the conventional and dual-mode supply modulators are the same, except the supply voltage of the linear amplifier and efficiency of the boost/buck–boost converter. Assuming that $\eta_{\rm boost}$ and $\eta_{\rm buck-boost}$ are 90% and 85%, respectively, $V_{\rm dd.Linear.HPM}(5\ {\rm V})/\eta_{\rm boost}$ is 5.56 V and $V_{\rm dd.Linear.LPM}(2.5\ {\rm V})/\eta_{\rm buck-boost}$ is 2.94 V. When these values are applied to the (1), the efficiency of the linear amplifier in the low envelope output is enhanced by two times compared to the conventional supply modulator. Fig. 8 shows the simulated efficiencies of the linear amplifier for the boost-mode and dual-mode supply modulators. The efficiencies are calculated considering the efficiencies of the boost converter and buck–boost converter under the assumption that the switching amplifier is a dc current source. The overall efficiency of the supply modulator at the low-power region is improved significantly because the power consumption of the linear amplifier [$P_{\rm dc.linear}$ in (3)] is reduced by converting the supply voltage of the linear amplifier from 5 to 2.5 V. Fig. 9 shows the simulated overall efficiency comparison between the conventional and proposed supply modulators with a variable load. The variable load is the real PA model based on a class-AB biased PA [11].

The output voltage swing is from 0.5 to 4.5 V for the HPM and from 0.5 to 1.92 V for the LPM, considering the

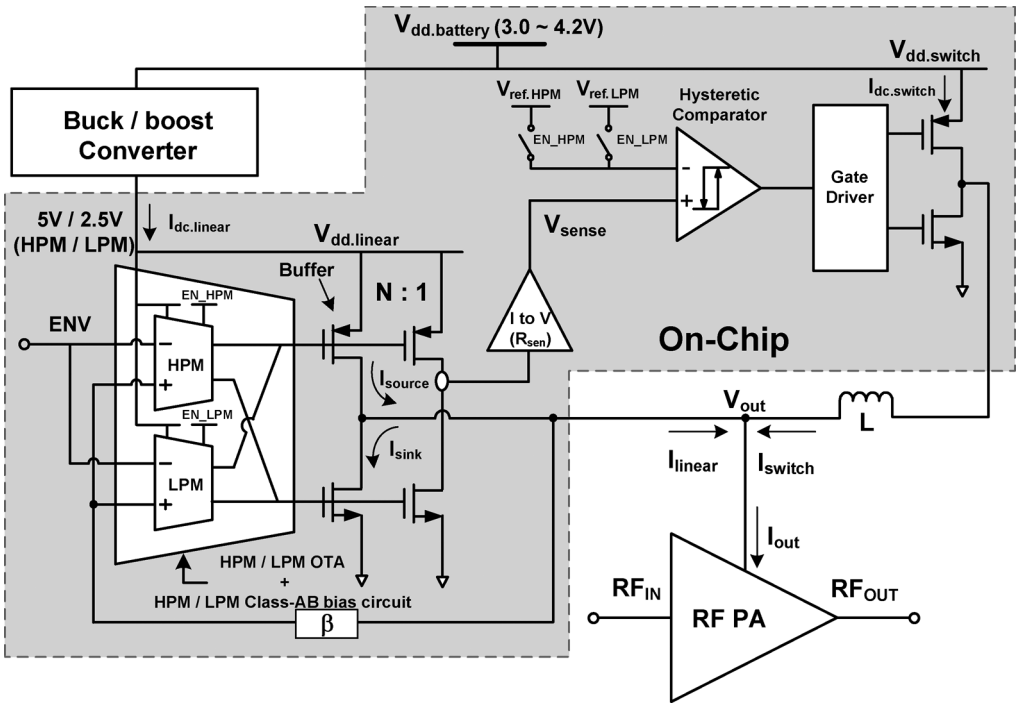

Fig. 7. Schematic of the proposed dual-mode supply modulator with the RF PA.

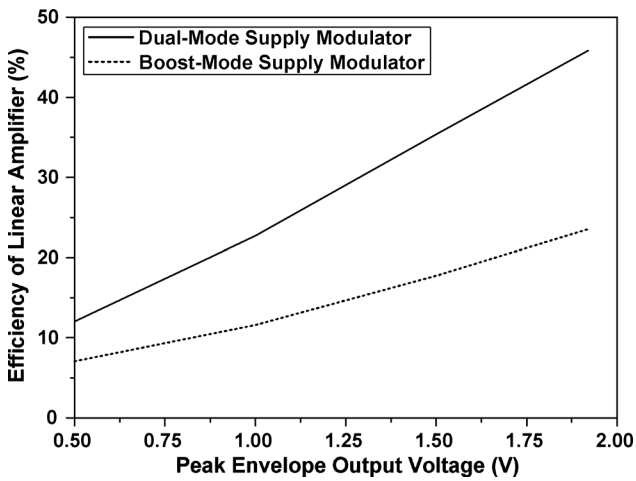

Fig. 8. Efficiencies of the linear amplifier for boost-mode and dual-mode supply modulators. (Switching amplifier is modeled as a dc current source.)

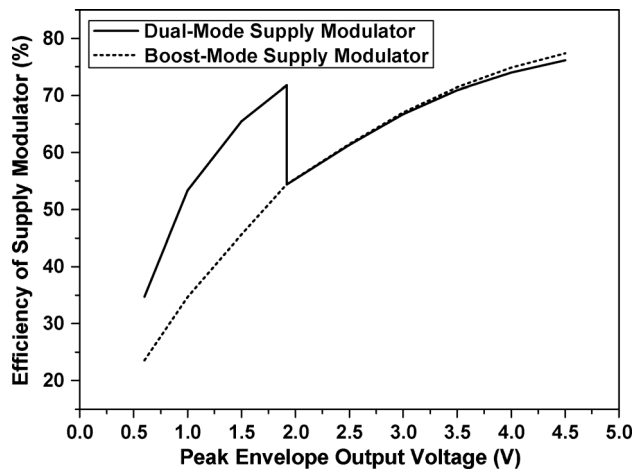

Fig. 9. Overall efficiencies of the boost-mode and dual-mode supply modulators with variable load.

linear operation of the PA without having the knee effect and the voltage drop through the linear amplifier. With envelope shaping method introduced in [11], the peak envelope output voltage is 1.92 V at a 9-dB back-off power level. The maximum output power in HPM is 925.1 mW with the overall efficiency of 76.3% at the peak envelope output voltage of 4.5 V. The maximum output power in LPM is 186.1 mW with the peak envelope output voltage of 1.92 V, in which the overall efficiency is 71.7%, improved by 17.3% using the dual-mode technique. The simulated performance of the dual-mode supply modulator is summarized in Table I.

III. Two-Stage ET PA with Dual-Mode Supply Modulator

Usually, a supply modulator is utilized only for the power stage of an RF PA, as shown in Fig. 10(a). The RF PA for handheld devices should have a multistage because of the gain budget of a transmitter system. Although the ET PA coupled only to a power stage improves efficiency by reducing the supply voltage in the power stage, the power consumption in the drive stage also significantly affects the overall efficiency at a low output power. Therefore, we have investigated feasibility of a dual-mode two-stage ET PA configuration for further

TABLE I
PERFORMANCE SUMMARY OF DUAL-MODE SUPPLY MODULATOR FOR 10-MHz LTE WITH 6.44-dB PAPR

Parameters	HPM	LPM
Output power (mW)	925.1	186.1
Supply voltage of linear amplifier (V)	5	2.5
Supply voltage of switching amplifier (V)	3.4	3.4
Output voltage range (V)	0.5-4.5	0.5-1.92
Assumed efficiency of buck-boost (%)	85	85
Efficiency of linear amplifier (%)	56.3	45.8
Overall efficiency (%)	76.3	71.7
GBW (MHz)	72.9	53.8
Phase Margin (degrees)	75.1	74.1

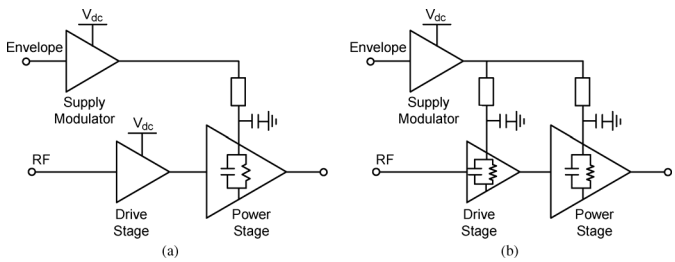

Fig. 10. ET structures. (a) ET operation only for power stage. (b) ET operation for both the drive and power stages.

enhanced efficiency at a power back-off region [see Fig. 10(b)].

A. Challenges of PA

Fig. 11 shows performances of the PA with a continuous wave (CW) by sweeping the collector bias from 1.0 to 4.5 V. Solid lines are simulated results of the ET operation for both the drive and power stages. Dash lines are simulated results of the ET operation only for power stage, and the collector bias of the drive stage is fixed to 3.4 V. The PAE and gain trajectories show those of the PA when the collector bias of the PA is dynamically changed by the supply modulator for the ET operation. We can expect that the two-stage ET PA has higher PAE than the single-stage ET PA. However, the gain of the two-stage ET PA is smaller than that of the single-stage ET PA, and the gain degradation is serious at low output power. Usually, the drive stage is designed for linear operation with a sufficient gain instead of the high efficiency. When the drive stage is also ET-operated using the supply modulator, it is operated in saturation mode, resulting in the reduced gain, but the enhanced efficiency, as shown in the trajectories of Fig. 11(a). For the ET operation of both the drive and power stages, the RF input power should be increased because of the suppressed gain.

For the two-stage ET operation, the drive stage generates a small amount of harmonic terms at a high collector bias, but the distortion increases rapidly as the collector bias is reduced, as shown in Fig. 11(b). These distortion terms are amplified by the

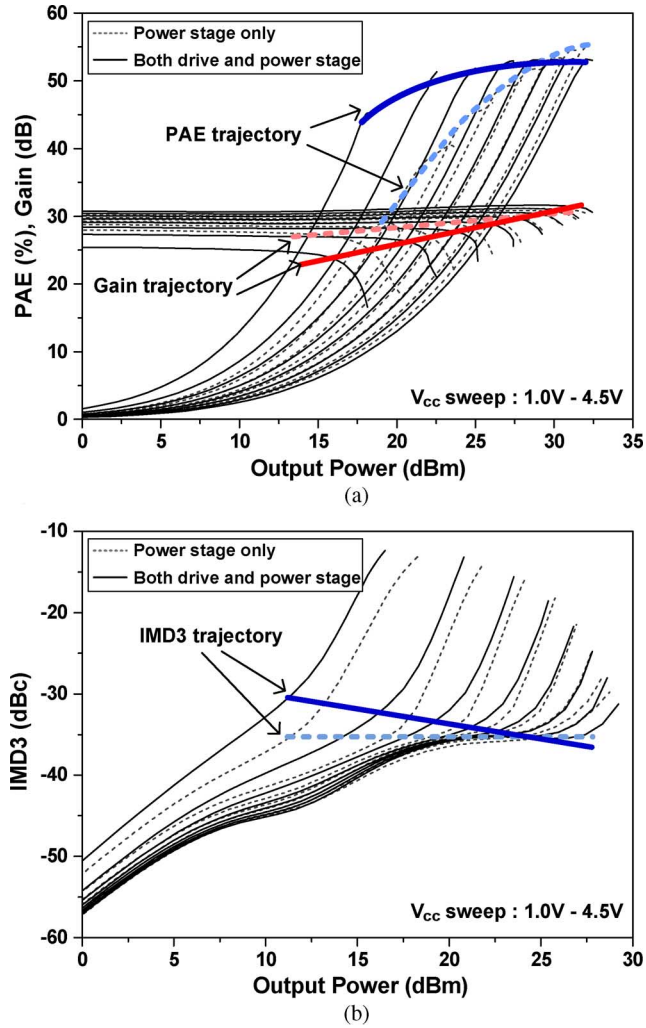

Fig. 11. Simulation results of RF PA. (a) PAE, gain, and (b) third-order intermodulation distortion (IMD3) with the supply voltage from 1.0 to 4.5 V.

power stage, degrading the linearity. Since the bias lines of the drive and power stages are shared without dc de-coupling capacitor, the low-frequency harmonics can be coupled, generating memory effects. The envelope signal can be reshaped to prevent the saturated operation of the drive stage. However, in this case, the efficiency of the power stage is decreased because the power stage does not operate in a saturation mode, either. Therefore, there is a tradeoff between the linearity and efficiency when the supply modulator is connected to the two stages of the PA at the same time. Instead of the envelope shaping method, the drive and power stages of the PA can be designed to have a gain compression characteristic, compensating the gain expansion occurred from the two-stage ET operation, and achieving a high efficiency and good linearity simultaneously.

B. Challenges of Supply Modulator

DC de-coupling capacitors with several μF, which is commonly employed for a standalone PA, cannot be connected to the bias lines of the PA in the ET operation because the envelope signal passes through the capacitor. However, the linear amplifier of the supply modulator operates itself as a dc de-coupling capacitor, and compensates the ripple voltage of the switching

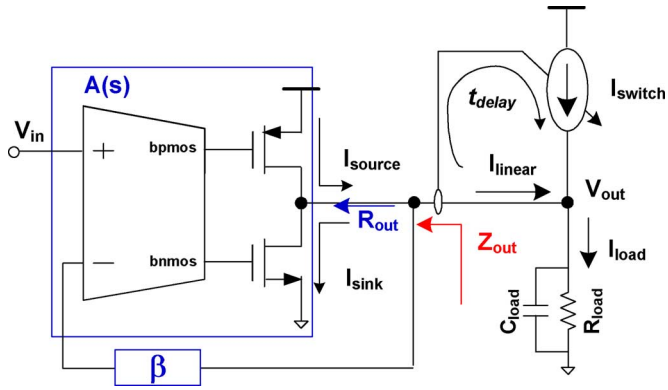

Fig. 12. Simplified block diagram of class-AB biased linear amplifier.

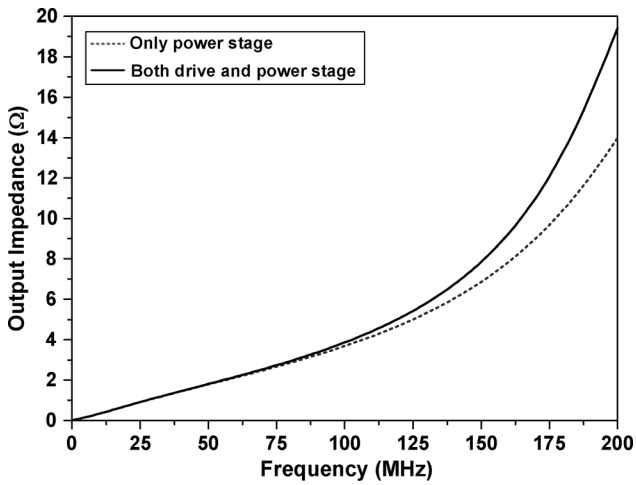

Fig. 13. Output impedance of the supply modulator.

amplifier and suppresses the noise from the PA. Fig. 12 shows a simplified block diagram of the class-AB biased linear amplifier. As reported in [15] and [19], output impedance of the linear amplifier can be expressed as

$$Z_{\text{out}}(s) = \frac{R_{\text{out}}}{1 + \beta \cdot A(s)} \tag{4}$$

where R_{out} is an output impedance of the class-AB biased buffer and $A(s)$ is a frequency response of the OTA. Since R_{out} and β are nearly constant values, Z_{out} are dependent on the $A(s)$. Since $A(s)$ is large at a low frequency, Z_{out} is small, but Z_{out} increases as the frequency increases due to the reduced gain $(A(s))$. The output impedance at the near switching frequency (a few megahertz) is very low and the supply modulator does not generate a large distortion. When the supply modulator is connected to the bias line of the drive stage, as well as the power stage, the load capacitance is increased because of larger RF short capacitors and larger device output capacitance. In this case, the bandwidth of the linear amplifier is reduced, increasing the output impedance of the linear amplifier, as shown in Fig. 13. The curves are simulated with the loads modeled as a parallel connected resistor and capacitor for the power stage and the two stage cases, respectively. The output impedances are large at a high frequency, and it is more serious for the two-stage ET operation. The failure of proper RF grounding

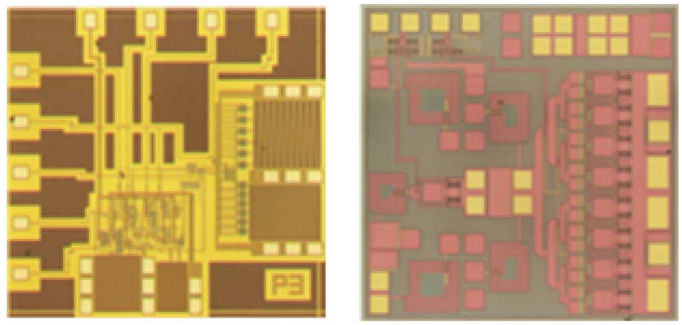

Fig. 14. Chip microphotographs. (a) Supply modulator. (b) PA.

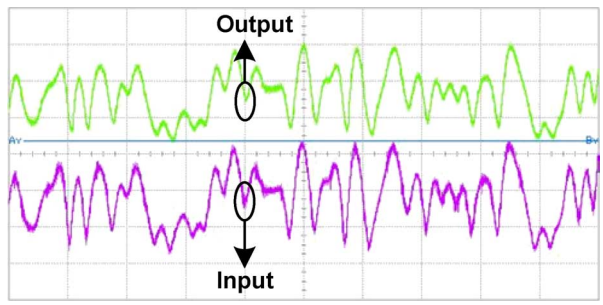

Fig. 15. Measured LTE time-domain waveforms of the proposed supply modulator. The vertical axis scale ratio of output/input is 1/5.

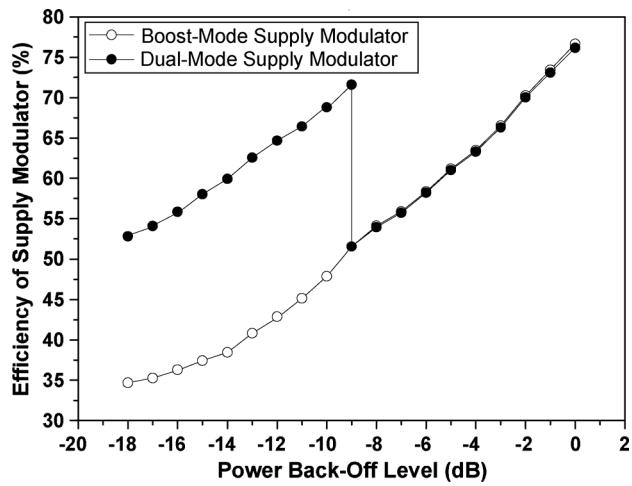

Fig. 16. Measured efficiencies of dual-mode and boost-mode supply modulators.

causes instability and nonlinearity of the PA. Therefore, the supply modulator should be designed with sufficient bandwidth and stable operation. In this proposed supply modulator, the bandwidth is expanded by inserting a zero in a feedback path of the linear amplifier [17].

IV. Measurement Results

The proposed dual-mode supply modulator is fabricated using a 0.18-μm CMOS process with thick oxide I/O devices for high-voltage operation. Chip microphotographs of the fabricated supply modulator and PA are shown in Fig. 14. This modulator and PA are 1.35 mm $\times$ 1.35 mm and 1.2 mm $\times$

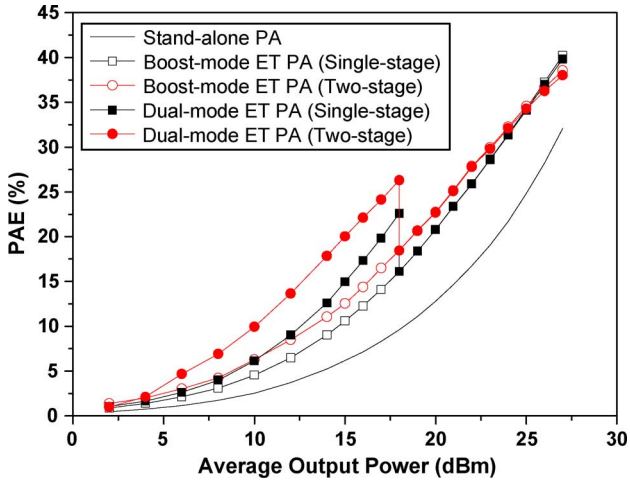

Fig. 17. Measured PAE comparison of the standalone PA, boost-mode single-stage and two-stage ET PA, and dual-mode single-stage and two-stage ET PA.

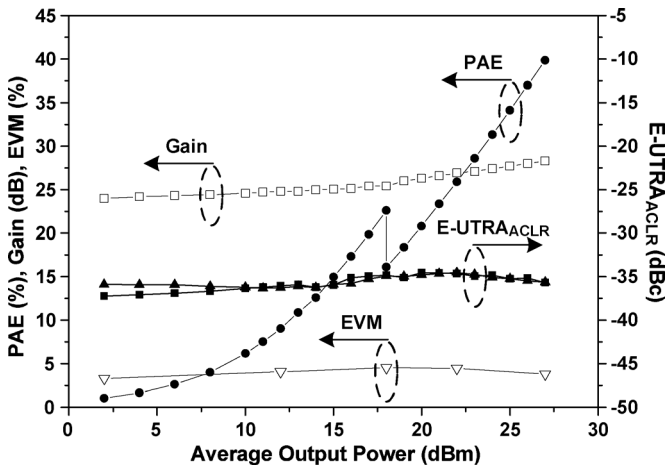

Fig. 18. Measured PAE, gain, EVM, and E-UTRA$_{\mathrm{ACLR}}$ of dual-mode single-stage ET PA.

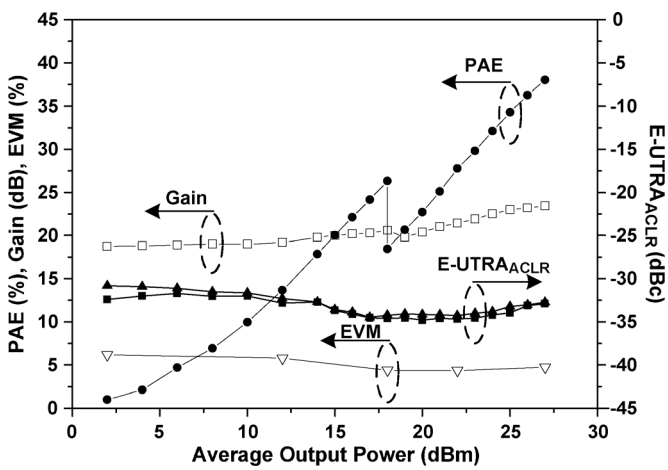

Fig. 19. Measured PAE, gain, EVM, and E-UTRA$_{\mathrm{ACLR}}$ of dual-mode two-stage ET PA.

1.2 mm in size, respectively, including all the pads. To test performance of the proposed supply modulator, the PA is simply modeled as a 6.5-Ω resistive load. Fig. 15 shows the measured time-domain input/output envelope signals of the proposed

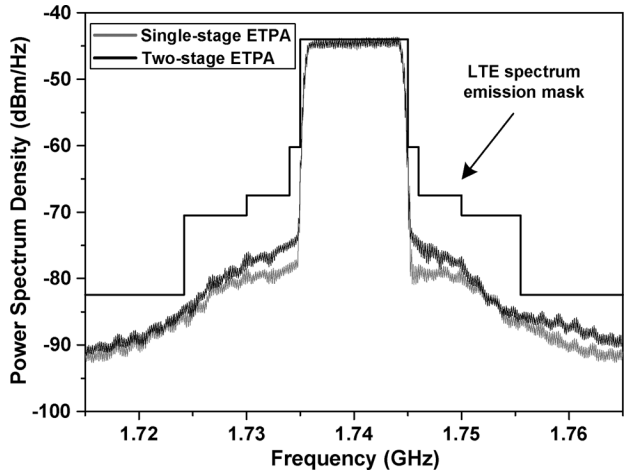

Fig. 20. Measured spectra of the dual-mode single-stage and two-stage ET PA at an average output power of 27 dBm with spectrum emission mask for 10-MHz LTE signal.

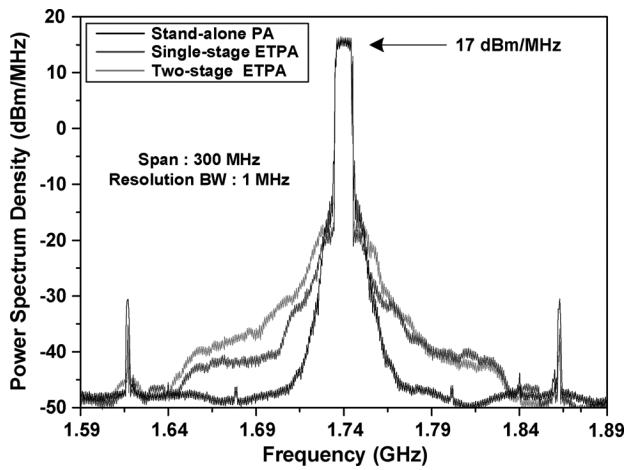

Fig. 21. Measured far-out spectra of the standalone PA and single-stage and two-stage ET PAs at an average output power of 27 dBm.

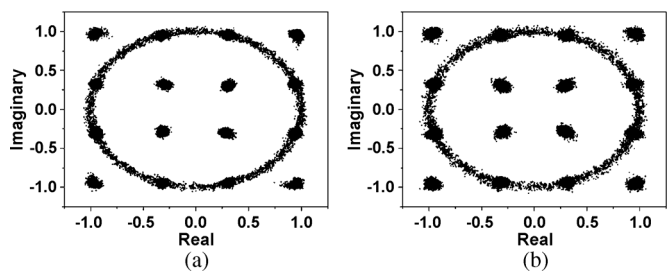

Fig. 22. Measured EVM plot of: (a) signle-stage ET PA and (b) two-stage ET PA.

supply modulator. It is shown that an input and output envelope signals are almost identical. For the 16-quadrature amplitude modulation (QAM) LTE envelope signal with 6.44-dB PAPR and 10-MHz bandwidth, the supply modulator delivers 4.5-V/1.92-V peak envelope output voltage for HPM/LPM with the efficiencies of 76.2%/71.6%, respectively. As shown in Fig. 16, the measured efficiency of the supply modulator at the power back-off level of 9 dB is improved by 20.1% compared to the conventional supply modulator.

TABLE II
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART RESULTS

Ref.	Modulation	PAPR (dB)	Freq. (MHz)	Pout (dBm)	PAE (%)	Gain (dB)	UTRA$_{\mathbf{ACLR1}}$* (dBc)	E-UTRA$_{\mathbf{ACLR}}$* (dBc)	DPD	Technology
[11]	LTE 16-QAM	7.44	1850	28.9	42.2	24.5†	-	-	No	0.18-μm CMOS,
	10-MHz			18	14†	23†	-	-		HBT
[13]	LTE 16-QAM	7	2400	24.3	42	16.3	-	-	No	0.35-μm SiGe BiCMOS
	5-MHz			18	18†	17†	-	-		
[14]	LTE	6.6	2535	29	43	28.5	-49	-	Yes	0.15-μm CMOS,
	20-MHz			18	15†	-	-	-		HBT
[16]	LTE 16-QAM	7.5	1900	24	41	15†	-	-	No	0.35-μm SiGe BiCMOS
	5-MHz			18	22	16.5†	-	-		
[21]	LTE 16-QAM	-	835	27	34.5	27.2	-	-31.2	No	HBT/pHEMT
	10-MHz			17	18.9	22	-	-31.6		
[22]	LTE QPSK	-	1950	27.5	38	27	-39	-	No	HBT/pHEMT
	10-MHz			16	24	14	-39	-		
This work1‡	LTE 16-QAM	6.44	1740	27	39.8	28.3	-39.6	-35.7	No	0.18-μm CMOS,
	10-MHz			18	22.6	25.4	-38.5	-34.9		HBT
This work2§	LTE 16-QAM	6.44	1740	27	38.1	23.4	-36.7	-32.9	No	0.18-μm CMOS,
	10-MHz			18	26.3	20.6	-38.5	-34.2		HBT

*LTE specifications: UTRA$_{\mathrm{ACLR1}} < -33$ dBc, E-UTRA$_{\mathrm{ACLR}} < -30$ dBc.
†graphically estimated ‡ Dual-mode single-stage ET PA § dual-mode two-stage ET PA

A two-stage class-AB PA at 1.74-GHz is fabricated using the InGaP/GaAs HBT process to implement the ET PA. The PA with a supply voltage of 4.5 V delivers a P1dB of 32.2 dBm, a gain of 31 dB, and a PAE of 55%.

The PA is ET-operated using the reshaped envelope voltage to prevent the operation below the knee voltage region for linear operation, as introduced in [11]. The ET PA delivers improved efficiency over a wide dynamic range compared to the standalone PA. The two-stage ET PA delivers higher efficiency than single-stage ET PA due to the reduced power consumption of the drive stage. By applying the dual-mode technique to the drive stage and power stage of the RF PA, the dual-mode two-stage ET PA significantly achieves enhanced efficiency over the whole low output power range, as well as at the maximum output power in the LPM. Fig. 17 shows the measured PAE comparison of the standalone PA, boost-mode single-stage and two-stage ET PA, and dual-mode single-stage and two-stage ET PA. At an average output power of 27 dBm, the dual-mode single-stage ET PA gives a PAE of 39.8%, which is 7.7% higher than that of a standalone PA. It also delivers a PAE of 22.6% at an average output power of 18 dBm, which is 6.5% higher than that of a boost-mode single-stage ET PA and 13.1% higher than that of a standalone PA. The dual-mode single-stage ET PA shows a gain of 28.3 dB, an evolved universal terrestrial radio access adjacent channel leakage ratio (E-UTRA$_{\mathrm{ACLR}}$) of -35.7 dBc, an UTRA$_{\mathrm{ACLR1}}$ of -39.6 dBc, an UTRA$_{\mathrm{ACLR2}}$ of -42.5 dBc, and an error vector magnitude (EVM) of 3.81% at an average output power of 27 dBm (Fig. 18). The dual-mode two-stage ET PA delivers a PAE of 38.1%, a gain of 23.4 dB, an E-UTRA$_{\mathrm{ACLR}}$ of -32.9 dBc, an UTRA$_{\mathrm{ACLR1}}$ of -36.7 dBc, an UTRA$_{\mathrm{ACLR2}}$ of -39.1 dBc, and an EVM of 4.74% at an average output power of 27 dBm (Fig. 19).

The dual-mode two-stage ET PA also delivers a PAE of 26.3% at an average output power of 18 dBm, which is 7.8% higher than that of the boost-mode two-stage ET PA and 16.7% higher than that of the standalone PA. Fig. 20 shows the measured spectra of the dual-mode single-stage and two-stage ET PAs at an average output power of 27 dBm with the spectrum mask for the 10-MHz LTE signal [26]. The measured far-out output spectra of the standalone PA, single-stage ET PA, and two-stage ET PA are plotted in Fig. 21 without any external filter. Compared to the standalone PA, the ET PA shows a noise up to the offset of 100 MHz from the center frequency, and the two-stage ET PA is more serious than the single-stage ET PA. The spur at the offset of 120 MHz from the center frequency is caused by the sampling rate of the source signal. The emission noise can be further suppressed by adding an extra filter. Fig. 22 shows the measured EVM plots of the single-stage and two-stage ET PAs, respectively. The performances of the designed dual-mode single-stage and two-stage ET PA are summarized together with recent state-of-art results in Table II.

V. CONCLUSION

An ET PA with a dual-mode supply modulator has been implemented using a 1.74-GHz class-AB HBT PA and 0.18-μm CMOS supply modulator. For the LPM operation of the supply modulator, the supply voltage of the linear amplifier is reduced from 5 to 2.5 V, together with proper sized OTA and reference voltage of the hysteretic comparator. The efficiency of the proposed supply modulator is improved in the whole low-power

region. For the 16-QAM LTE signal with 6.44-dB PAPR and 10-MHz bandwidth, the dual-mode supply modulator achieves the efficiencies of 76.2%/71.6% at the power back-off levels of 0 dB/9 dB, respectively. In particular, the measured efficiency at the power back-off level of 9 dB is improved by 20.1% compared to a conventional supply modulator. The dual-mode single-stage ET PA gives a PAE of 39.8% and an E-UTRA$_{\mathrm{ACLR}}$ of -35.7 dBc at an average output power of 27 dBm. The ET PA also delivers a PAE of 22.6% at an average output power of 18 dBm; this performance is 6.6% higher than that of boost-mode single-stage ET PA and 13.1% higher than that of the standalone PA. For further enhanced efficiency at a power back-off region, the supply modulator is employed to the drive stage and power stage of the RF PA at the same time. The dual-mode two-stage ET PA delivers PAE of 38.1% and an E-UTRA$_{\mathrm{ACLR}}$ of -32.9 dBc at an average output power of 27 dBm. This ET PA also delivers a PAE of 26.3% at an average output power of 18 dBm, which is 7.8% higher than that of the boost-mode two-stage ET PA and 16.7% higher than that of the standalone PA. These results indicate that the dual-mode technique in the supply modulator for the two-stage ET PA configuration can be a promising candidate to extend the battery life of handheld devices in 4G wireless communication systems.

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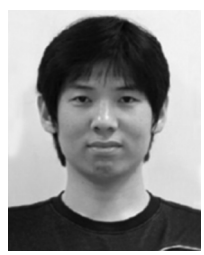

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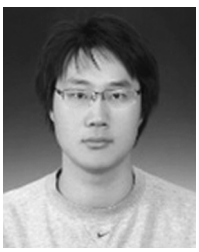

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