Control of IMD Asymmetry of CMOS Power Amplifier for Broadband Operation Using Wideband Signal

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***Abstract*—A fully integrated linear CMOS power amplifier (PA) for the broadband operation is developed for handset applications. This amplifier can handle a wideband signal. To achieve broadband/wideband operation, an analysis of the intermodulation distortion for the asymmetric source in a differential cascode structure is presented. Based on the analysis, the linearization technique using a second harmonic circuit at the gate of the common gate is proposed to reduce the asymmetry. The proposed PA with an on-chip transmission-line transformer, which has a broadband matching characteristic, is fabricated using a 0.18-μm RF CMOS technology. The measurement results show that the sideband asymmetry is less than 0.6 dB for a signal with up to 50-MHz bandwidth, and the peak average power is improved by 1.2 dB within the linearity spec of a 16-QAM 7.5-dB peak-to-average power ratio long-term evolution signal. The PA delivers a power-added efficiency of 36.5%–31.2% and an average output power of 27.5–27.1 dBm under an $\mathrm{ACLR}_{\mathrm{E-UTRA}}$ of -30.5 dBc for a 50-MHz bandwidth signal across 1.4–2.0-GHz carrier frequency.**

***Index Terms*—Adjacent channel leakage ratio (ACLR), broadband, cascode, CMOS class-AB, common gate (CG), differential, intermodulation distortion (IMD), linearity, linearization, linear amplifier, long-term evolution (LTE), memory effect, power amplifier (PA), third-order intermodulation distortion (IMD3) asymmetry, transmission-line transformer (TLT), wideband.**

I. Introduction

As MODERN communication systems evolve, mobile equipment should be able to handle voice, video streaming, and broadcast with global roaming capability. The applications, such as long-term evolution (LTE), mobile worldwide interoperability for microwave access (m-WiMAX), and wideband code division multiple access (WCDMA), require transmitting a signal at a programmable center frequency with a wide bandwidth. As the information content increases, the signals of the communication systems are coded by spectrally efficient modulation, such as orthogonal frequency-division multiplexing (OFDM). The market of handheld devices also demands a fully integrated single-chip solution with low cost. To satisfy these requirements, power amplifiers (PAs) should have a capability to handle multiband and wideband signals to cover a number of functions and should be implemented by the CMOS process.

The output power, efficiency, and linearity of the PAs are dramatically degraded as the signal bandwidth and/or operation frequency increases because the sideband asymmetry of PAs that is generated by memory effects are directly proportional to the channel bandwidth. Moreover, the amplifier performance is degraded as the PA bandwidth is increased. For these reasons, both multiband and wideband requirements are a challenging job in CMOS PA design. To overcome these limitations, the PA design for multiband and wideband signal techniques have been hot research items for a long period of time [1]–[4].

Digital-predistortion (DPD) is known as one of the most effective linearization techniques. The DPD can be used to reduce memory effects for achieving a wideband signal operation [5]–[8]. Since a DPD is composed of a predistorter, digital-to-analog converters (DACs), and digital signal processing (DSP), the power consumption of the DPD increases as the signal bandwidth increases.

A polar structure using a digitally modulated power amplifier (DPA) has been investigated for a broadband signal operation [9], [10]. A DPA is based on switching on and off of sub-PAs, which should be an inherently broadband operation. However, because of an AM/PM time misalignment in the polar architecture, the linearity is degraded as the signal bandwidth increases [11].

It has been reported that the sideband asymmetry is caused by the reflections of the envelope frequency and second harmonics at the device terminals [12]. Previous reports focus on the envelope impedance, which should be terminated by a short-circuit condition at the bias network of PAs [13]–[15]. In a differential cascode structure, the second harmonic is generated by mismatches of the differential pairs, voltage-dependent gate–source nonlinear capacitances, and frequency-dependent

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parasitic components due to the large feeding structure. For realization of a linear CMOS differential cascode amplifier, therefore, it is important to reduce the second harmonic component. However, there has been no research reported on the differential cascode PA with different harmonic impedances at the gates of the common-gate (CG) stage due to the mismatch between each sub-cell pair. We analyze the intermodulation distortion (IMD) asymmetries for broadband/wideband channel signals and propose an improvement technique. To the authors' best knowledge, this PA is the first one to simultaneously achieve the broadband/wideband CMOS linear PA with a high linearity and power-added efficiency (PAE).

This paper is organized as follows. In Section II, the node impedance at the sub-cell of the CG stage is investigated to eliminate the sideband asymmetry using a proposed harmonic control circuit. The proposed linearization technique delivers a significantly reduced sideband asymmetry, as explained in Section III. In Section IV, the implementation of the proposed PA and experimental results are presented. Finally, conclusions of this work are summarized in Section V.

II. Sideband Asymmetry of Differential Cascode CMOS PA

A. Review of Generation Mechanism for Sideband Asymmetries

To investigate causes of the sideband asymmetry, we briefly review the expression of third-order intermodulation distortion (IMD3) following the previous studies [16], [17]. To find the characteristic of IMD3, which is the primary source of asymmetry, the nonlinear drain current (i_d) can be expanded in a Taylor series

$$i_d = G_m v_g + G_d v_d + G_{m2} v_g^2 + G_{d2} v_d^2 + G_{md} v_g v_d + G_{m3} v_g^3 \ldots \quad (1)$$

where v_g and v_d are the gate and drain signal voltages, and the G terms represent transconductance, drain conductance, and cross terms, respectively. The higher order nonlinearities are ignored to reduce the complexity of the analysis.

The drain of the common-source (CS) stage is connected to a frequency-dependent load impedance $Z_L(\omega)$, which consisted of the CG stage input impedance and the bias network or virtual ground in a differential cascode amplifier, as shown in Fig. 1. The common node of the CG provides a virtual ground at odd terms, but does not provide the ground at even terms. Thus, the even harmonic impedance $Z_L(\omega_{\text{even}})$ is neither a real, nor a low impedance, generating significant harmonics. The lower and upper IMD3s of the drain voltage in the CS stage can be derived [18]–[22] and simplified as

$$V_{d3}(2\omega_2 - \omega_1) = v_g^3 Z_L(\omega_c) \left[\frac{1}{2} G_{m2} G_{md} Z_L(\omega_2 - \omega_1) + \frac{1}{4} G_{m2} G_{md} Z_L(2\omega_c) + \frac{3}{4} G_{m3} \right] \quad (2)$$

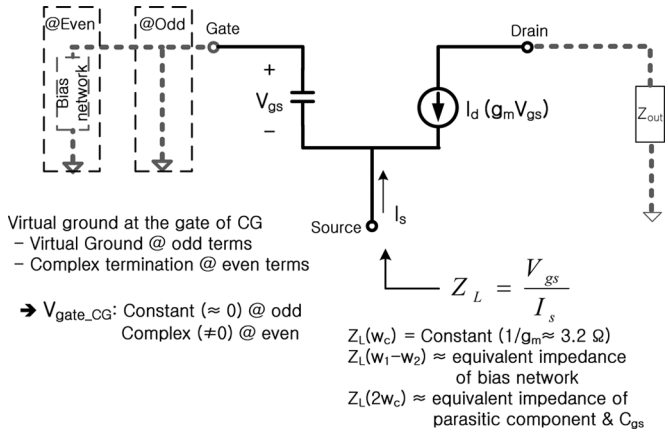

Fig. 1. Simplified CG amplifier model used for the analysis.

$$V_{d3}(2\omega_1 - \omega_2) = v_g^3 Z_L(\omega_c) \left[\frac{1}{2} G_{m2} G_{md} Z_L(\omega_1 - \omega_2) + \frac{1}{4} G_{m2} G_{md} Z_L(2\omega_c) + \frac{3}{4} G_{m3} \right] \quad (3)$$

where ω_1 and ω_2 are the lower and upper input tone frequencies, respectively, ω_c is the center frequency of $(\omega_1 + \omega_2)/2$, and Z_L is the frequency-dependent load impedance, which generates the asymmetry through its imaginary part for simplicity. For simplicity, $Z_L(2\omega_c)$ is assumed to be a constant value for frequency range of $2\omega_1 \sim 2\omega_2$, which is true for a properly designed handset PA [23]. The significant difference between (2) and (3) is the phase of the envelope third-order intermodulation (IM3) terms ($\theta(\Delta\omega) = \tan^{-1}[\mathrm{Im}(Z_L(\Delta\omega))/\mathrm{Re}(Z_L(\Delta\omega))]$), which are changed to the opposite direction according to the tone spacing, and $\Delta\omega$ is the different frequency of $(\omega_1 - \omega_2)$.

From (2) and (3), we can see that the IMD3 term is generated through two different mechanisms, which are the third-order interaction and the second-order and fundamental nonlinear mixing. The memoryless-IMD3 components are generated by the third-order mechanisms, which provide the same magnitude and phase between the lower and upper IMD3s. The second-order mixing products generated by the envelope signal have different imaginary parts for the upper and lower IMD3, and the second-order mixing products generated by the second harmonic terms have the same phase ($\theta(2\omega_c) = \tan^{-1}[\mathrm{Im}(Z_L(2\omega_c))/\mathrm{Re}(Z_L(2\omega_c))]$). The memory effect on the IMD3 component is created by the mixings of the envelope and fundamental and of the second harmonic and fundamental through the second-order nonlinearity. The process can be represented by a vector diagram of the IMD3 composition in Fig. 2. As shown in the figure, the imaginary parts of the envelope impedance contribute to the IMD3 asymmetries with help of the imaginary part of the second harmonic impedance. There are two cases that can eliminate the sideband asymmetries; the second harmonic load termination is real or shorted and the load at the envelope frequency is terminated at a short-circuit condition. However, the second harmonic should be shorted because the impedance is not controlled in the differential structure.

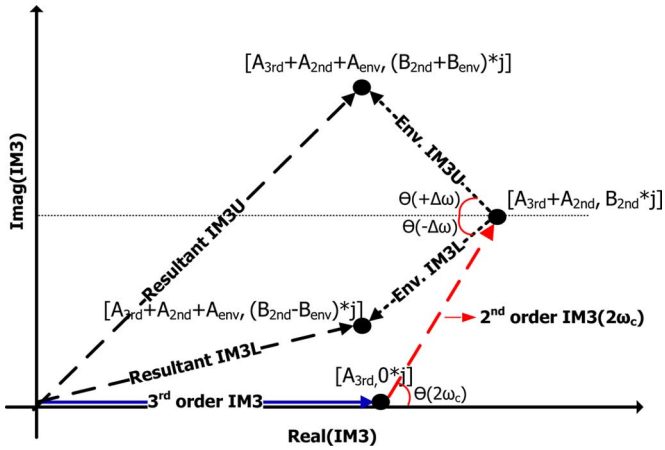

Fig. 2. Vector representation for composition of the IM3 normalized to $Z_L(\omega_c)$. The phase notation of envelope frequency and second harmonic IM3 terms: $\theta(\Delta\omega) = \tan^{-1}[\mathrm{Im}(Z_L(\Delta\omega))/\mathrm{Re}(Z_L(\Delta\omega))]$ and $\theta(2\omega_c) = \tan^{-1}[\mathrm{Im}(Z_L(2\omega_c))/\mathrm{Re}(Z_L(2\omega_c))]$.

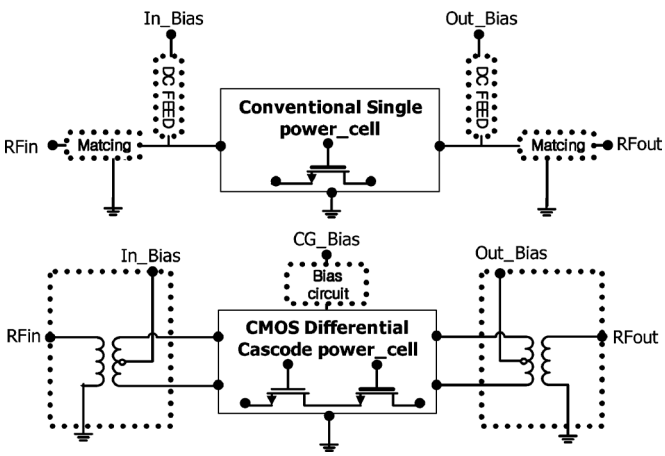

Fig. 3. Basic configurations of single-ended and differential structure amplifiers.

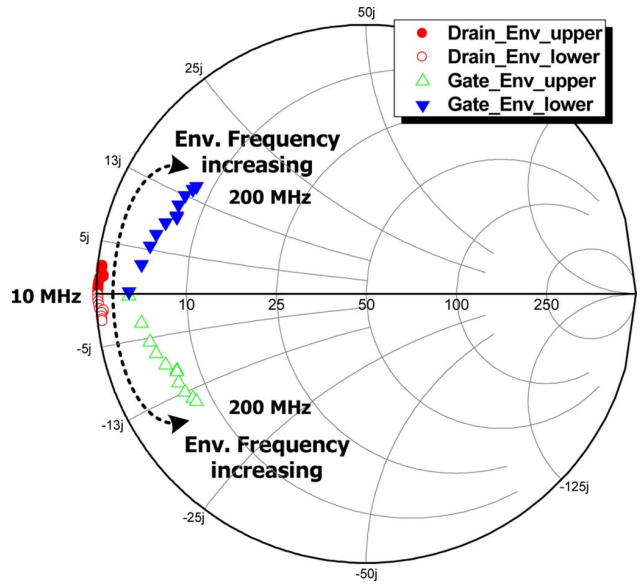

Fig. 4. Envelope impedances at the gate of the CS and the drain of the CG according to the envelope frequency (tone-spacing: 10–200 MHz).

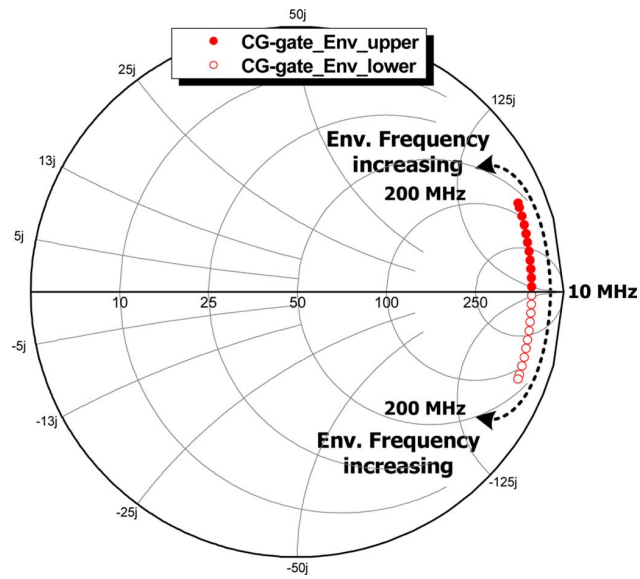

Fig. 5. Envelope admittances at the gate of the CG stage according to the envelope frequency (10–200 MHz).

B. CMOS PA Structure Using a Transmission-Line Transformer (TLT)

In the CMOS process, there are some problems, such as no support of ground via-holes, low breakdown voltages, and low-current-driving capabilities. To overcome these problems, a differential cascode structure PA is widely used to reduce the source grounding inductance of the CS amplifier and to enhance the breakdown voltage by stacking two transistor into a cascode configuration [24]–[27]. Since the differential structure doubles the voltage swing to a balanced load; the load impedance can be two times larger. For the same load impedance, the output power can be four times larger than that of a single-ended structure. In the differential structure, besides a balanced source and load, baluns are required at the input and output to convert single-ended into differential mode and vice versa. However, the balun can be functioned simultaneously as an impedance transformer and a power combiner [28]. The TLT transmits the energy from the input to the output by a transmission line mode and not by a flux leakage, as in the conventional transformer [29]. If the TLT is used as the output transformer, the PA has a wide bandwidth and high efficiency [30]. Therefore, a broadband matching network can be achieved using the TLT.

C. Node Impedance of Differential Cascode PA at the Envelope Frequency

In general, PAs are composed of three parts: an input and output matching, bias networks, and a power cell for amplification. The single-ended and differential structure PAs comprise the three components, as shown in Fig. 3. However, the methods for applying biases are different; the single structure uses separated matching and bias networks, and the differential structure uses a single merged matching and bias network. Therefore, the node impedances of the PAs have two different values for the input/output RF matching network and the bias network. At the gate and drain of the single-ended structure,

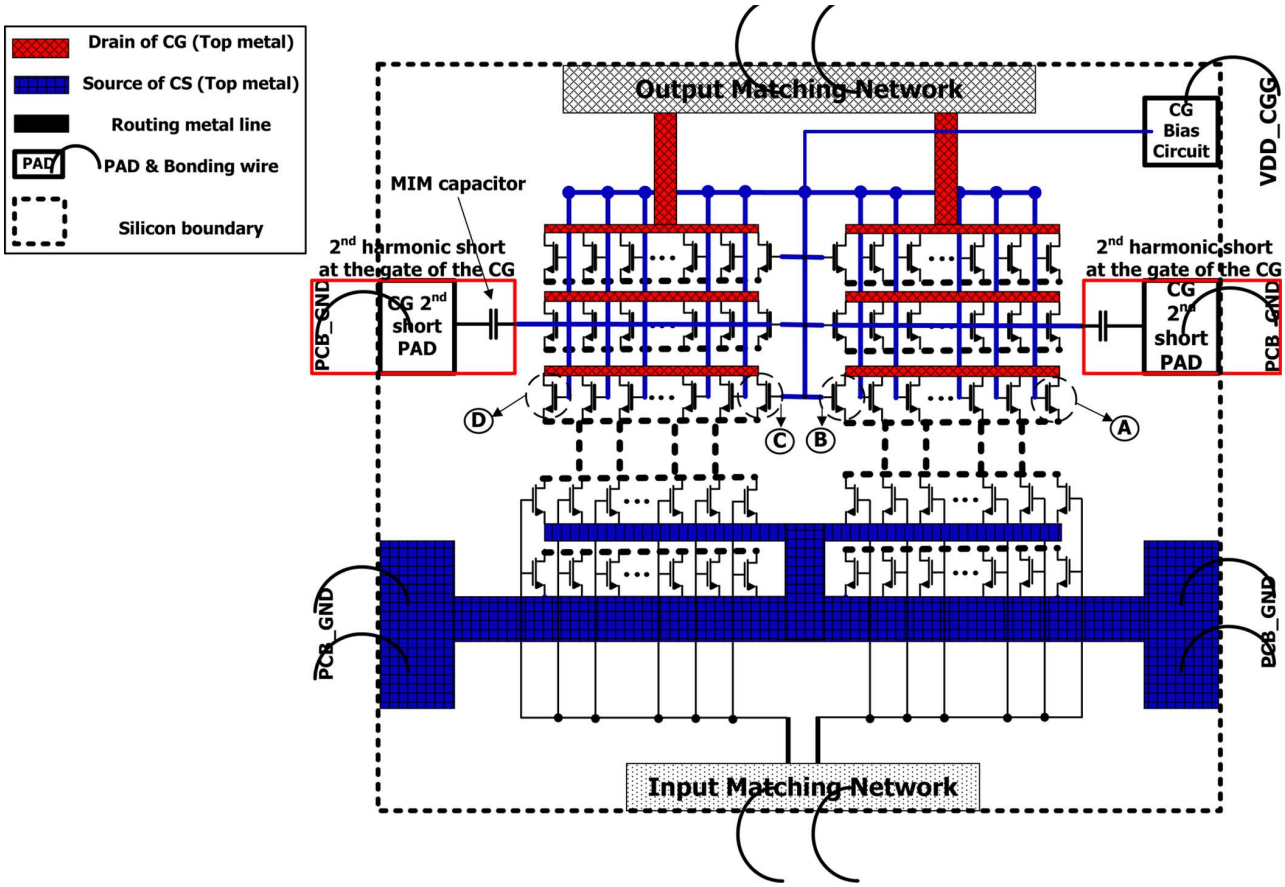

Fig. 6. Schematic diagram of the power-cell layout, which the proposed second harmonic termination.

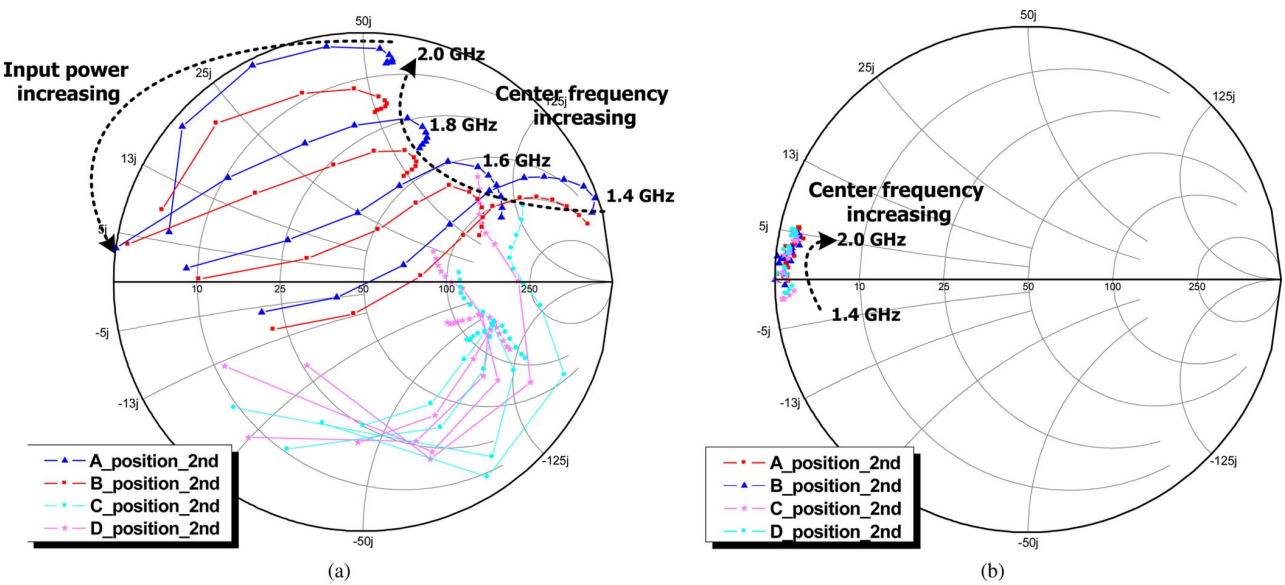

Fig. 7. Second harmonic impedances at the gate of the CG stage according to frequency (1.4–2.0 GHz) and input power: (a) without and (b) with second harmonic circuits.

there are two connections; a dc-feed circuit with higher frequency blocking and a matching network for the fundamental, second, and third harmonics to achieve the maximized performance. Since the dc-feed circuit needs a large time constant for low-pass filtering, the circuit has a large reactance at a low frequency and the memory effect can be appeared.

The bias nodes of the differential cascode structure have virtual grounds at the center tap of the input and output baluns and the gate of the CG stage. The virtual grounds make it possible to provide a short-circuit condition at the fundamental frequency and odd harmonics. The center taps of the input and output baluns are used in biasing, as well as even harmonic

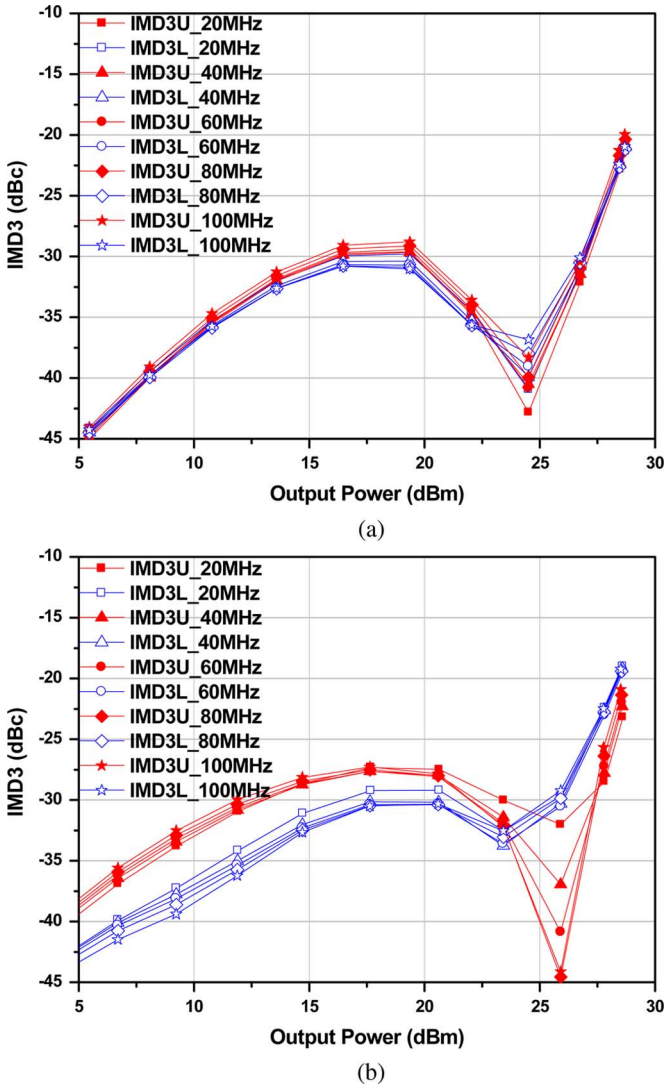

Fig. 8. Simulated IMD3s versus output power for different envelope frequency: (a) with proposed second harmonic circuit and (b) without second harmonic circuit at the gate of the CG.

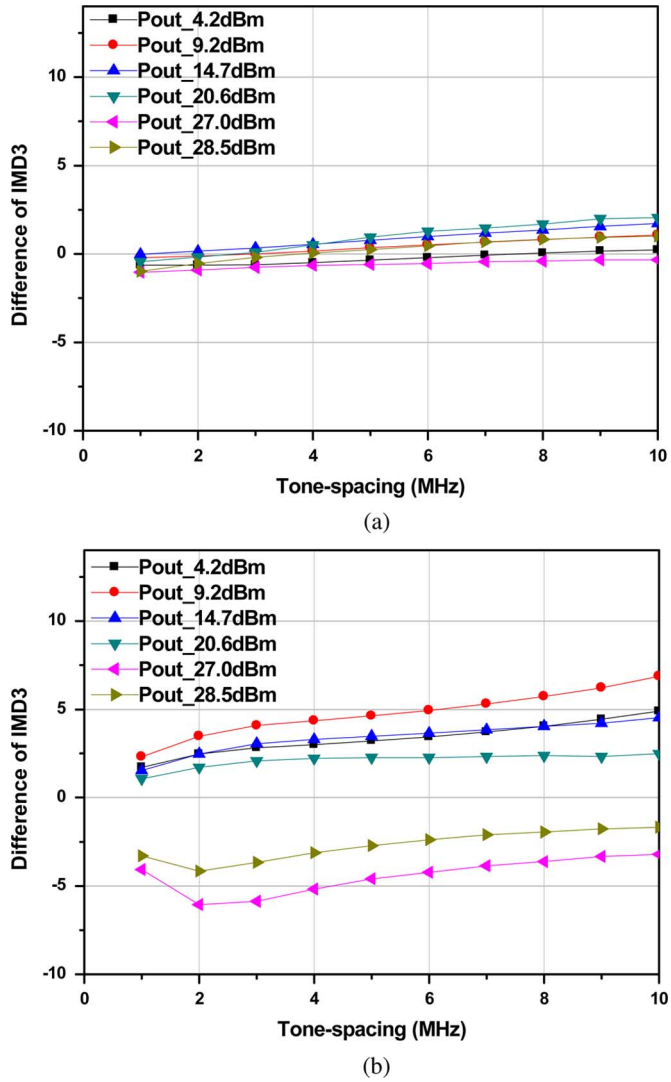

Fig. 9. Simulated differences of IMD3s versus envelope frequency for different output power: (a) with proposed second harmonic circuit and (b) without second harmonic circuit at the gate of the CG.

matching. The center taps are directly connected to an external voltage source through bonding wire for applying the drain and gate biases. Since the short-length bonding wire and the inductance of the primary coil in the balun generate a small amount of reactance, the impedances of the source and load nodes at the envelope frequency are properly terminated at low impedances without any extra circuit. However, the second harmonics should be properly terminated, which can be carried out easily. Therefore, there are no sources of memory effects in the source and load matching networks due to the use of the bias circuit with the balun in a differential PA. However, the grounding of the CG stage can be a problem.

Fig. 4 shows the envelope impedances at the gate of the CS and the drain of the CG according to the envelope frequency (tone spacing). As the envelope frequency increases, the impedances at the gate of the CS and the drain of the CG increase like an inductor. For the envelope frequency, the imaginary parts of the impedances are increased in opposite directions. Since the input balun is designed using a narrow metal with several turns to provide the desired source impedance, the envelope impedances at the gate have larger variation than those at the drain. On the other hand, as the envelope frequency increases, the envelope admittance at the gate of the CG increases as a capacitor, as shown in Fig. 5. Since the node impedance at the gate of the CG stage is composed of voltage-supply dividing resistors, voltage-dependent nonlinear capacitance of the transistor, and bonding wire connecting each other, the equivalent node impedance is large and capacitive [31], [32]. Therefore, the CG stage can generate a strong memory if the second harmonic short is not provided properly.

D. Investigation on Second-Order Nonlinearity in a Differential Cascode PA

A differential cascode amplifier is composed of CS and CG amplifiers. The common nodes of the CS and CG create a virtual ground at the fundamental and odd harmonic frequencies, but do not create the ground at even harmonics. The low-impedance terminations at the even harmonics are very

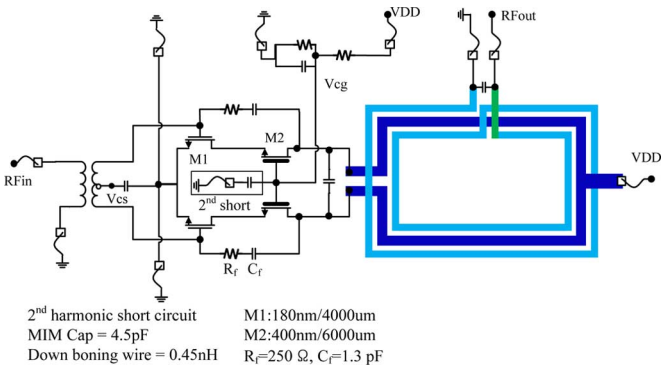

Fig. 10. Schematic of fully integrated CMOS PA.

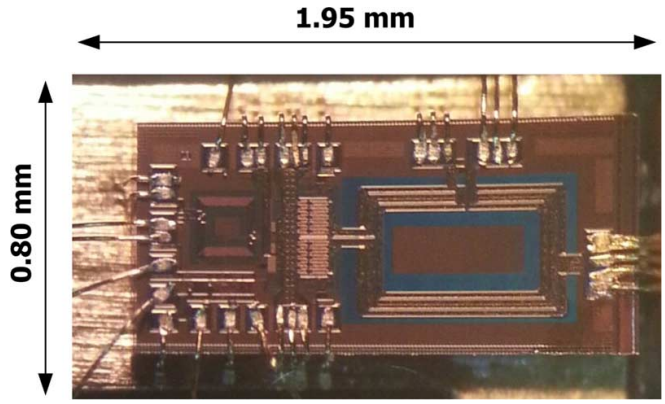

Fig. 11. Microphotograph of the CMOS PA.

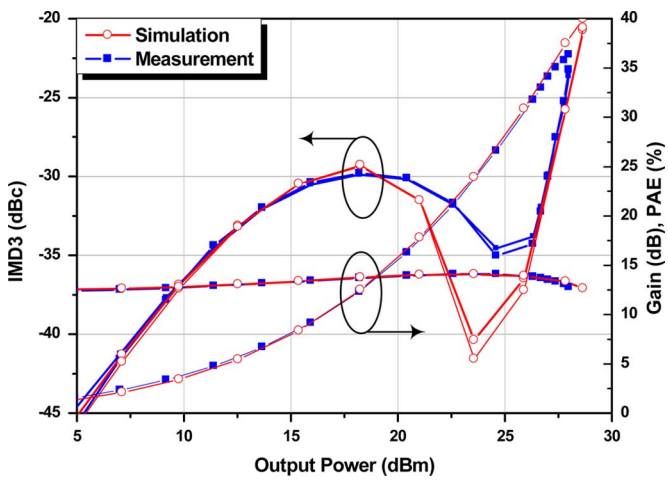

Fig. 12. Simulation and measurement data of gain, PAE, and IMD3s.

important for overall performance of the PA. As discussed previously, the nodes connected to the virtual grounds can be easily terminated to a short circuit, and is done properly in many previous designs, but the drain of the CS and the gate of the CG stages should be terminated properly for the even harmonics, but it has been neglected thus far. In the real device, however, it is necessary to maintain a low-impedance termination at the envelope and second harmonic frequency. The gate of the CG stage has two different roles; one is voltage biasing the gate of the CG and the other is to provide a ground at the fundamental and odd harmonics. To supply a bias, the gate of the CG is connected by an external voltage source with blocking resistor (typically 1 kΩ) or inductor through bonding wire. Therefore, the impedance at the second harmonic frequency is not properly terminated as a short because the inductive connection of the CG makes a high-impedance path as frequency increases. Moreover, mismatches of the differential pair and the large feeding lines can generate different second harmonic impedances at the unit cells. The even harmonics at the common nodes are suppressed in the differential structure, but it does not prevent the internal third harmonic generation processes.

To simplify the subsequent discussion without losing the important insights, let us make an observation on the differential cascode amplifier. In the amplifier, the node impedances at the envelope frequency are properly terminated at a low-impedance condition through the center taps of input/output baluns. However, because of the reasons discussed above, the envelope and second harmonic impedances at the gate of the CG are not properly terminated in a short-circuit condition if a special tuning circuit is not provided. In other words, the sideband asymmetry can be reduced by controlling the second harmonic impedances at the gate of the differential cascode amplifiers. As the IMD3 related with the second harmonic component is reduced, the linearity is also improved. Based on this analysis, we propose a proper grounding circuit for the second harmonic impedance at the gate for an improved performance with reduced asymmetry, as shown in Fig. 2.

III. Proposed Second Harmonic Termination Circuit at the Gate of the CG Stage

The bias network at the gate in the CG stage is different from the biases at the gate of the CS and the drain of the CG. Normally, the bias network is designed by using a resistor and a capacitor to supply a proper bias voltage according to the given voltage swing [25]. Since the roles of the CG are a current buffer as a second stage and a part of the output load seen by the CS, the harmonic impedance of the CG node is the most important element for the overall linearity of the amplifier. The CG bias network must provide a low-impedance termination at the envelope frequency and second harmonics. As discussed above, due to the large area of the power cells and feeding lines, mismatches of the differential pairs, dc feed (resistor and/or inductor), etc. can provide different impedances at the second harmonics, which are dependent on their locations in the layout, while the imaginary parts of the envelope impedances can be controlled to a low impedance condition without using a tuning circuit.

Fig. 6 shows the schematic diagram of the conventional power-cell layout. In this layout, the second harmonic impedances at the each unit cell are different. To verify this feature, we perform a harmonic-balance (HB) simulation on Agilent Technologies' Advanced Design System (ADS). Fig. 7(a) shows the second harmonic impedances at each terminal (labeled Ⓐ–Ⓓ in Fig. 6) of sub-cells (transistor) in the drawn layout according to the input power level and center frequency (1.4–2.0 GHz). As shown, the second harmonic impedances are dependent on the power level and the frequency band and its location, and the impedances vary quite a lot. These different second harmonic impedances can make the sideband

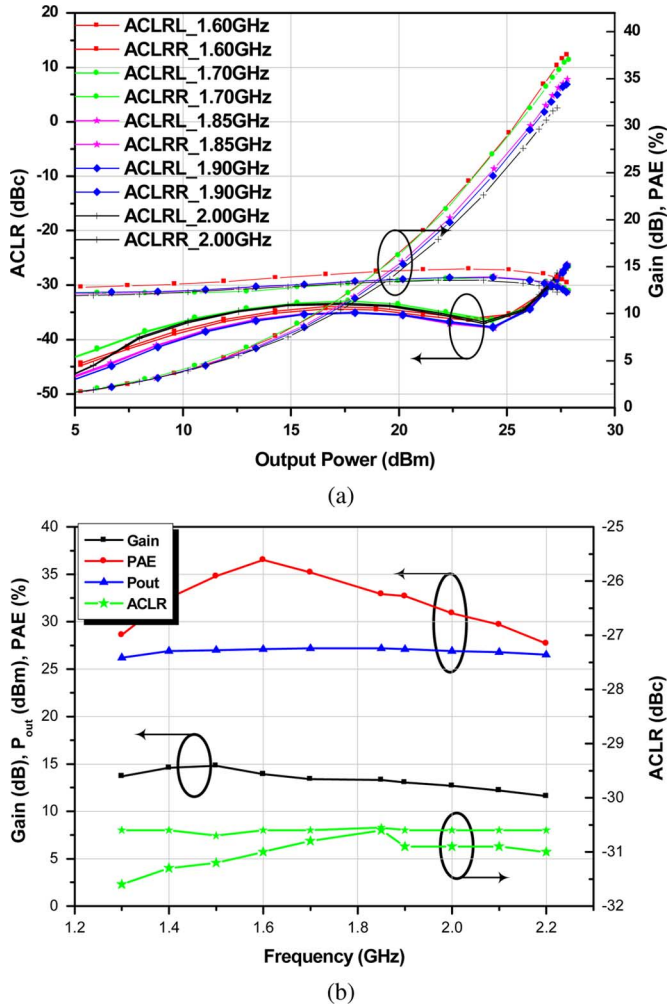

Fig. 13. Measured performance for broadband operation with 10-MHz bandwidth LTE signal: (a) according to the output power and (b) according to the center frequency.

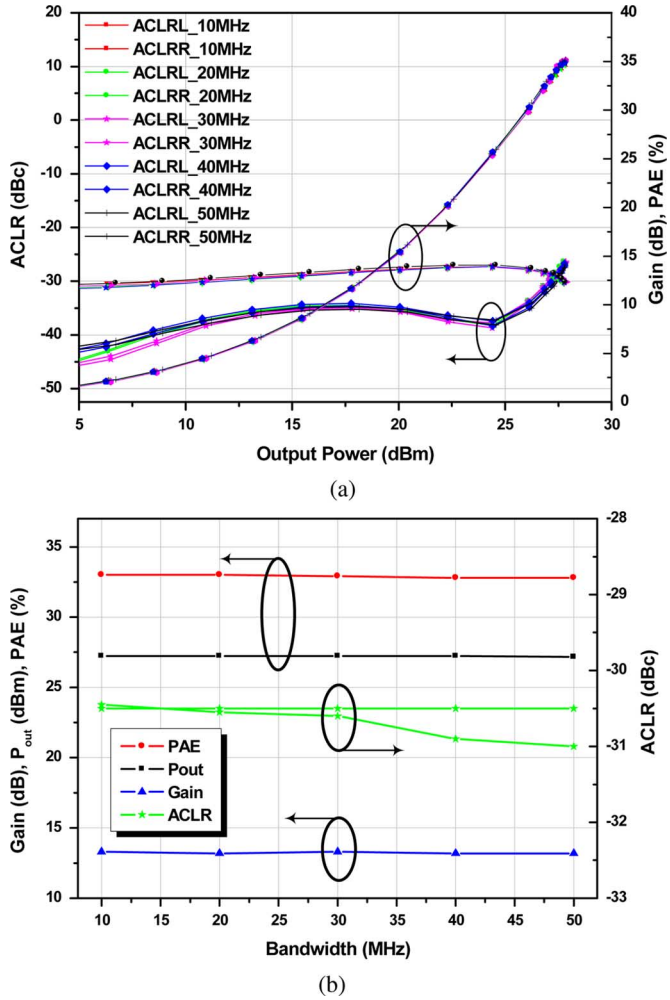

Fig. 14. Measured performance for wideband operation at 1.85 GHz: (a) according to output power and (b) according to channel bandwidth.

asymmetries and degrade the IMD3 by (2) and (3). The conventional layout cannot achieve a short-circuit condition for the second harmonic impedance at the unit cells. Therefore, a second harmonic short circuit at the gate of the CG stage should be provided at near to the cells. After applying the proposed second harmonic short circuit as shown in Fig. 6, the second harmonic impedance at the gates of each unit cell is properly terminated to a short-circuit condition in the frequency range of 1.4–2.0 GHz, as shown in Fig. 7(b). Simulation results of the IMD3 for two-tone signals with spacing from 10 to 100 MHz at 1.85-GHz center frequency are represented in Fig. 8. When the harmonic circuit is attached, almost all of the asymmetry has been disappeared, and the IMD3 is improved. The maximum difference between the upper and lower IMD3 according to the output power and envelope frequency is less than 2.0 dB significantly reduced from the conventional layout, as shown in Fig. 9. We can clearly see the improvement on overall linearity of the PA by achieving the almost symmetrical sideband in the IMD3 using the proposed second harmonic control circuit at the cells. As shown in Fig. 7(b), the second harmonic impedances are controlled properly across the 1.4–2.0 GHz, and the amplifier can be operated linearly across the bandwidth since the TLT provides the proper matching across the band.

IV. Implementation and Measurement Results

A. Implementation

The schematic of the differential cascode PA with the proposed second harmonic short circuit is shown in Fig. 10. A thick-oxide 0.4-μm device for the CG and thin-oxide 0.18-μm device for the CS is stacked in a cascode structure to mitigate the problem of the low breakdown voltage. The total gate width of the thin and thick devices are 4000 and 6000 μm, respectively. A feedback network with series resistor (250 Ω) and capacitor (1.3 pF) between the drain of the CG and the gate of the CS is used to improve linearity and stability. The second harmonic short circuit is composed of a metal–insulator–metal (MIM) capacitor (4.5 pF) and an inductor (0.45 nH) implemented by down-bonding wires, which is designed to resonate at the second harmonic frequency.

The optimum output impedance of each power cell is 6–7 Ω at each cell, which is determined through the load–pull simulation. Generally, the transformer occupies about 60% of the total PA area. To reduce the size of the transformer and match directly to the optimum output impedance, 1:2 TLT is employed, as shown in Fig. 10. The output on-chip transformer is implemented using a stack of two thick copper metals to reduce the

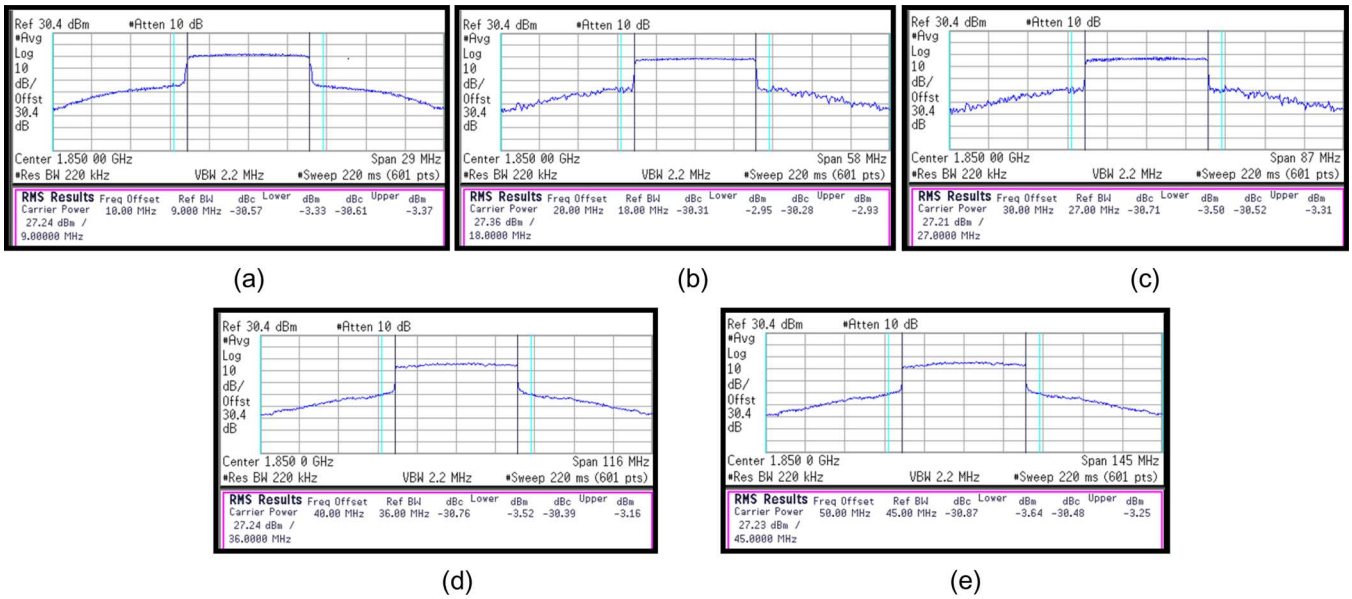

Fig. 15. Measured output spectra while applying an LTE signal at 1.85 GHz with: (a) 10-, (b) 20-, (c) 30-, (d) 40-, and (e) 50-MHz bandwidths.

insertion loss. The spacing between the primary and secondary of the transformer is 10 μm. The widths of the primary and secondary are 35 and 20 μm, respectively. The size of the output transformer is 0.85 mm $\times$ 0.54 mm. The insertion loss of the output matching network including the two matching capacitors is 1.15 dB at 1.85 GHz, and is less than 1.3 dB from 1.4 to 2 GHz.

B. Measurement Results

The differential cascode PA with the proposed CG bias circuit is fabricated using a 0.18-μm RF CMOS technology. A chip micrograph of the fabricated PA is presented in Fig. 11. For measurement, the chip dies are directly attached to the ground plane of the printed circuit board (PCB) of FR-4 using an electrically conductive silver epoxy. All signal and bias feeding pads are wire bonded to the PCB with gold wires. Since all of the matching circuits are integrated on-chip, there is no external component on the PCB. The bias condition of the PA with no input signal is a 3.5-V supply voltage and 42-mA current.

The PA with and without the proposed harmonic control circuit at the CG are compared by a two-tone test. The two tone measurements are performed at a 1.85-GHz center frequency with 10-MHz tone spacing. Fig. 12 shows the two-tone measured power gain, PAE, and IMD3s with respect to the output power together with the simulation results. When we apply the proposed linearization technique, the asymmetry of the upper and lower IMD3 is not observed. The measurement and simulation results are in good agreement, as shown in the figure.

For a demonstration of the broadband operation, the proposed PA is tested with 10-MHz bandwidth 16-QAM 7.5-dB peak-to-average power ratio (PAPR) LTE signal. The adjacent channel leakage ratio (ACLR) is measured under evolved universal terrestrial radio access (E-UTRA) specification with a 9-MHz resolution bandwidth at both a center frequency and a 10-MHz offset. Fig. 13 shows the measured performance of the proposed PA to confirm broadband operation across a

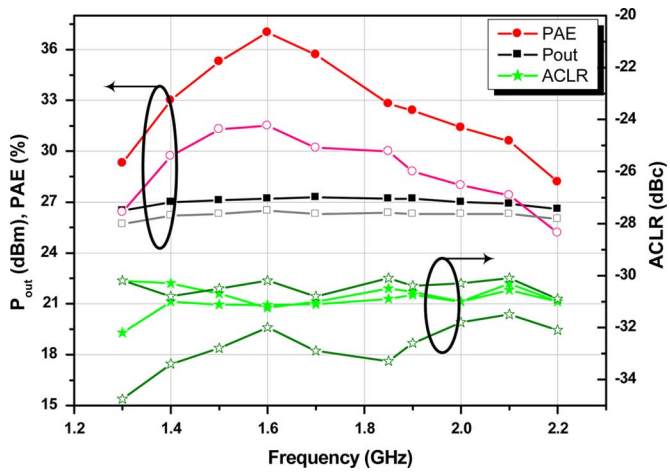

Fig. 16. Measured performances for the 50-MHz BW LTE signal across 1.3–2.2-GHz bandwidth. (Hollow symbol: without proposed linearization. Filled symbol: with proposed linearization.)

1.4-2-GHz band. The PA has an average output power and a PAE of 27.5–27.1 dBm and 36.5%–31.2%, respectively, while the $\mathrm{ACLR_{E-UTRA}}$ level is under -30.5 dBc, which is below the LTE specification of -30 dBc. The upper and lower $\mathrm{ACLR_{E-UTRA}}$ differ by less than 0.6 dB across the band. The gain is 14.8–12.7 dB across the frequency range.

To confirm the operation for a wideband signal, the PA is tested using LTE signals with 10–50-MHz channel bandwidth at a 1.85-GHz center frequency. Since the LTE signals with 30–50-MHz bandwidths are not yet defined, it is created by increasing the sampling rate of the existing LTE signal. The PA has an average output power and a PAE of 27.3 dBm and 33.0%–32.7%, respectively, while the $\mathrm{ACLR_{E-UTRA}}$ level is under -30.5 dBc, as shown in Fig. 14. The performance does not change with the signal bandwidth although the ACLR is spread a little for a wideband signal. Fig. 15 shows the measured spectra of the PA for 10–50-MHz bandwidth signals at a

1.85-GHz center frequency, which are within the LTE spectrum mask.

To show the broadband/wideband signal operation, the measured average output power, $\mathrm{ACLR_{E-UTRA}}$, and PAE as a function of center frequency using 50-MHz bandwidth signal are measured for the PAs with and without the proposed linearization, and are shown in Fig. 16. The proposed PA provides a significant improvement in sideband asymmetries of the ACLR, which are reduced from 4.8 to 0.6 dB. The average output power and PAE are improved by 1.2 dB and 5.2%, respectively. The proposed second harmonic control circuit in this work can deliver the broadband/wideband operation without DPDs.

V. Conclusion

In this paper, we have presented an analysis for sources of the IMD3 asymmetry in a differential cascode PA and proposed a technique to reduce it. The second harmonic control circuit at the gate of the CG stage is required for the purpose. With the linearization circuit, the fully integrated CMOS PA could operate across the broadband using a wideband signal. We demonstrate that this approach reduces the sideband asymmetry for 50-MHz signal across 1.4–2.0-GHz bandwidth. The measurement results show maximum 0.6-dB sideband asymmetry of $\mathrm{ACLR_{E-UTRA}}$ up to 50-MHz signal bandwidth and 1.2-dB improvement in peak average power. We achieve a PAE of 36.5%–31.2%, an average output power of 27.5–27.1 dBm, $\mathrm{ACLR_{E-UTRA}}$ of -30.5 dBc across 1.4–2.0-GHz band for a 50-MHz bandwidth 16-QAM 7.5-dB PAPR LTE signal. These results verify that the proposed design can deliver a linear power amplification for a broadband/wideband signal of wireless handheld applications. This proposed linearization technique is an attractive solution for implementing handheld CMOS PAs.

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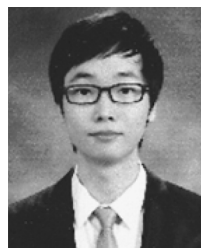

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