Linearization of CMOS Cascode Power Amplifiers Through Adaptive Bias Control

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***Abstract*—Highly linear and efficient CMOS cascode power amplifiers (PAs) are developed for handset applications. The linearity of the PAs is improved using adaptive bias circuits at the gates of the common-source (CS) and the common-gate (CG) stages. The memory effects that are generated by the bias circuits are reduced using second harmonic control circuits at the source of the CS and the gate of the CG stages. The proposed PA, including the integrated bias circuits, is fabricated using a $0.18-\mu\mathrm{m}$ RF CMOS technology. The adaptive gate bias circuits improve the linearity and efficiency significantly. The measurement results show that the sideband asymmetry is less than 1.5 dB and the peak average power is improved by 1.2 dB within the linearity specification for a 16-QAM 7.5 dB PAPR LTE signal. The bias circuits improve the linearity of the PA within the specification without using digital pre-distortions. The CMOS PA delivers a power-added efficiency (PAE) of 41.0%, an error vector magnitude (EVM) of 4.6%, and an average output power of 27.8 dBm under an ACLR_{E-UTRA} of -31.0 dBc for a 10-MHz bandwidth signal at 1.85-GHz carrier frequency.**

***Index Terms*—ACLR asymmetric, adaptive bias circuit, AM-to-AM, baseband injection, bias circuit, cascode, class-AB, CMOS, common-gate, deep class-AB, differential, envelope injection, IMD asymmetry, inter-modulation distortion (IMD), linear power amplifier, linearity, linearization, long term evolution (LTE), low quiescent current, memory effect, PCB transformer, power amplifier (PA), transmission line transformer (TLT).**

I. Introduction

With an explosive demand for smart handheld devices that can handle various functions, including modern high-speed wireless communications and tablet computer, the devices must ensure longtime usage of the battery. In the handheld devices, the power amplifier (PA) is one of the most power-consuming blocks, and techniques to improve the efficiency for prolonged battery life of the devices are required.

To handle the increased information of contents using the limited available frequency spectrum, modern wireless applications, such as long-term evolution (LTE) and mobile world-wide interoperability for microwave access (m-WIMAX), the signals of the applications are coded by spectrally efficient modulation, such as quadrature amplitude modulation (QAM), quadrature phase shift keying (QPSK), and orthogonal frequency-division multiplexing (OFDM). The modulated signals have high peak-to-average-power ratios (PAPR) with wide bandwidths. Therefore, the PAs should be operated at a back-off power from the peak to satisfy the stringent linearity requirements. The back-off operation results in a serious efficiency degradation.

Furthermore, integration of RF integrated circuits (RFIC) with baseband processors is required for system-on-chip (SOC) realization to reduce cost and size of the handheld devices. For this purpose, the PAs should be implemented in a CMOS process. However, implementation of the PAs using the CMOS process is a major challenge because of low-current-driving capabilities, no substrate via-holes, low quality factor, and the low breakdown voltage. To address these limitations, a cascode PA with differential structure is popularly employed. Various linearization techniques have been studied, such as capacitance compensation, the use of multi-gate transistors (MGTRs), analog and digital pre-distortion, feedback structure, and adaptive bias circuit [1]–[11].

Because the performances of the PAs are strongly dependent on their bias conditions, integrated bias circuits can be utilized for linearization, which is one of the advantages of the CMOS process. The PAs with a deep class-AB operation are the most attractive operation in terms of the linearity and the efficiency [12]. However, the deep class-AB PA with the bias near the threshold voltage generates a large inter-modulation distortion (IMD) at low and mid power regions, and it has a strong gain-expansion characteristic that degrades the AM-AM [13], [14]. The adaptive bias circuit at the gate of the common-gate (CG) amplifier is proposed to suppress the distortion and gain deviation in [15]. Injecting the envelope signal through a bias circuit at the gate of the common-source (CS) amplifier reduces the IMD components at a high power region canceling the distortions [16]–[20]. The gain of the PA is expanded at the saturated region when the envelope signal is injected at the gate. Therefore, the performance of the PA can be further improved by collaboration of the two adaptive bias circuits.

Memory effects, which are caused by the reflections of the envelope frequency and second harmonics at the device ter-

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minal, determine the linearity of the PA [21]. Because the adaptive bias circuits inject the envelope signal into the gate, a conventional method, such as an envelope impedance termination, cannot be applied to reduce the sideband asymmetries. Therefore, the second harmonic impedances at the source of the CS and the gate of the CG stages are adjusted to eliminate the sideband asymmetric. To the authors' best knowledge, the resulting PA delivers the state-of-the-art performances for linear amplification using CMOS process.

This paper is organized as follows. Section II presents the proposed linearization through adaptive gate bias circuits for linear CMOS PAs. Memory effects which are generated by harmonic impedances at the device nodes and bias circuits are discussed in Section III, together with the second harmonic control circuits at the device nodes to reduce the memory effects. The implementation of the proposed PA and experimental results are presented in Section IV. Finally, conclusions of this work are discussed in Section V.

II. Linearization Technique of Cascode PAs Using Adaptive Bias Circuits

Despite the attractive advantages of the CMOS technology in integration and cost, there are some problems to implement CMOS PA, such as no support of ground via, low reliability due to a low breakdown voltage, conductive substrate, and a low-current-driving capability. In the CMOS process, a differential cascode structure PA is widely used to minimize the source grounding effect of the CS amplifier and to enhance the breakdown voltage by stacking two transistors into a cascode configuration [22], [23]. Because of the low transconductance of the CMOS device, large power cells are required to achieve a high output power. Parasitic components due to the large cells can lead to degradation of the efficiency and linearity of the PA. Since the differential structure doubles the voltage swing to a balanced load; the load impedance can be two times larger. For the same load impedance, the output power can be four times larger than that of a single-ended structure. Hence, the use of a differential structure helps to mitigate the drawback of the source degeneration.

A. Bias Dependent Characteristics of Cascode PAs

The overall performance of a PA is strongly dependent on its operation class, which is determined by the gate bias. Generally, a deep class-AB mode with low quiescent-current operates more linearly and efficiently than that with class-AB or class-A mode at a high power region because the IMD minimum point (sweet-spot) moves towards near the compression point as shown in Fig. 1. It can be achieved through biasing the gate of the CS amplifier at a deep class-AB in the cascode PAs. Therefore, deep class-AB operation is the most attractive operation for linear PAs design at a high power region. As mentioned earlier, the PA presents a severe nonlinear behavior near turn-on voltage in the deep class-AB operation and generates a large distortion at low and mid power regions.

A differential cascode amplifier is composed of the CS and CG amplifiers. The CS and CG amplifiers function as a main amplification as the first stage and a current buffer as the second stage, respectively, with a part of the output load seen by the CS stage. Combining a gain-expansion stage (deep class-AB) and

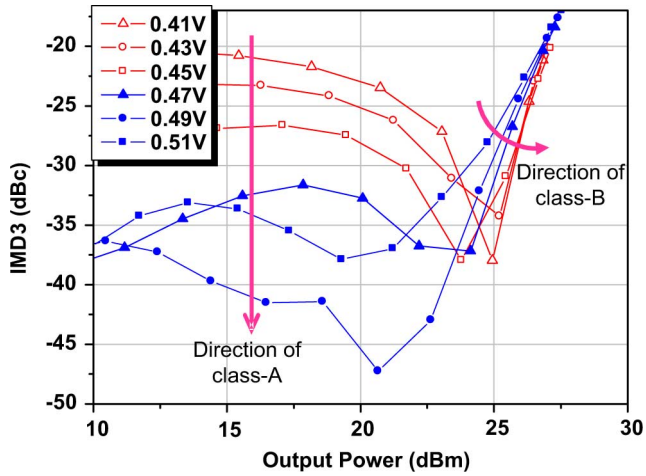

Fig. 1. IMD3 versus output power for different gate biases of the CS device at the gate of the CG device of 2.8 V.

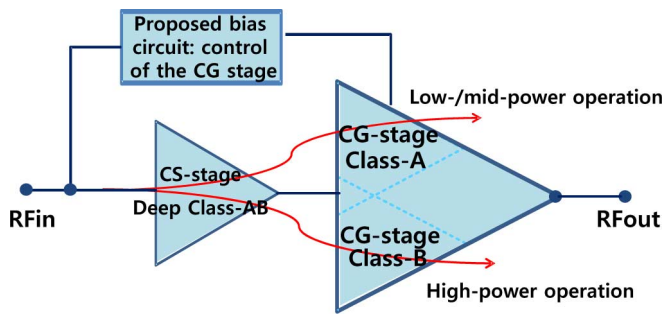

Fig. 2. Block diagram of the proposed linearization.

a gain-compression stage (class-A) compensates the AM-AM distortion through reduction of the gain deviation. The examples are MGTR and multi-stage cascade structures [24], [25]. In a similar manner, the CG stage can be employed to reduce the gain deviation and IMD generated by the CS stage under the deep class-AB operation. Fig. 2 shows a block diagram of the linearization process. The CS amplifier operates in deep class-AB mode while the CG amplifier in Class-A mode in low and middle power regions. In a high power region, the CG amplifier operates in class-B mode. In summary, the CS stage operates in deep class-AB mode for the good high power performance while the CG stage operates in either class-A or class-B mode according to the input power level to absorb the intermodulation nonlinear distortion.

B. Linearization Technique Using Adaptive Bias Circuits

In a large signal operation, the drain current of a CMOS PA is dependent on the drain bias as well as the gate bias. The drain bias of the CS device is determined by the CG gate bias in the cascode structure, as follows:

$$V_{drain\_CS} \cong V_{cg} + V_{env\_signal} - V_{th\_CG} \tag{1}$$

where V_{cg} and V_{th_CG} are the gate and threshold voltages of the CG device, and V_{env_signal} is an envelope signal of the input signal. Hence, the gate bias of the CG device can be controlled for the optimized performance in designing cascode PAs. Simulation results of the gain and IMD3 for a two-tone signal

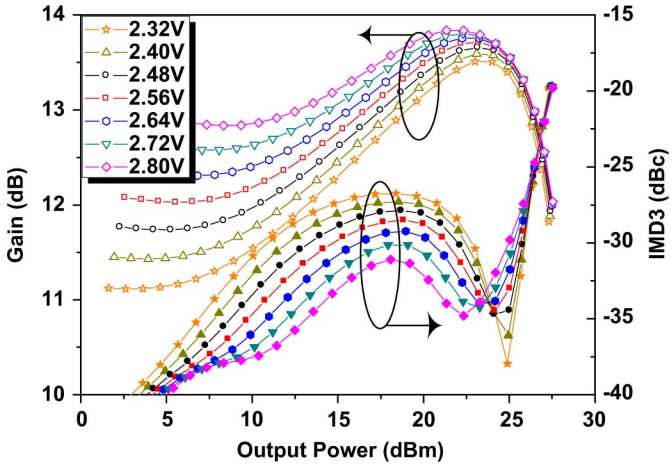

Fig. 3. Simulated gain and IMD3 (10-MHz tone spacing) characteristics according to the output power for different gate biases of the CG device (2.80 V&2tilde;.32 V) with 0.46 V gate bias of the CS device. (Hollow symbol: Gain, Filled symbol: IMD3).

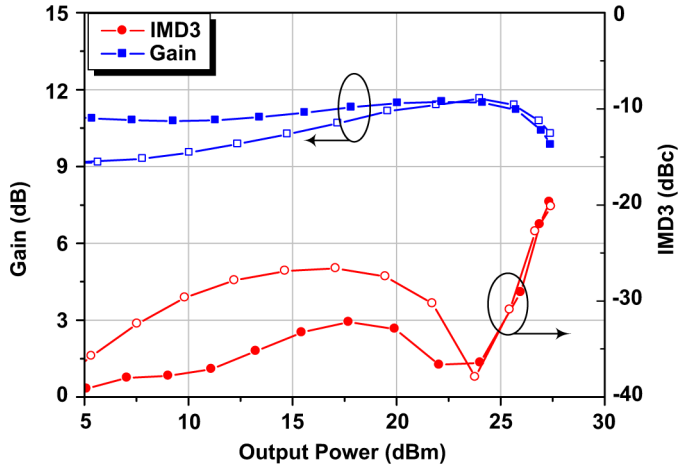

Fig. 5. Simulated gain and IMD3 (10-MHz tone spacing) according to the output power at the gate bias of the CS device of 0.46 V (deep class-AB bias) with the optimal CG bias (filled symbol) and the constant CG bias of 2.4 V (hollow symbol).

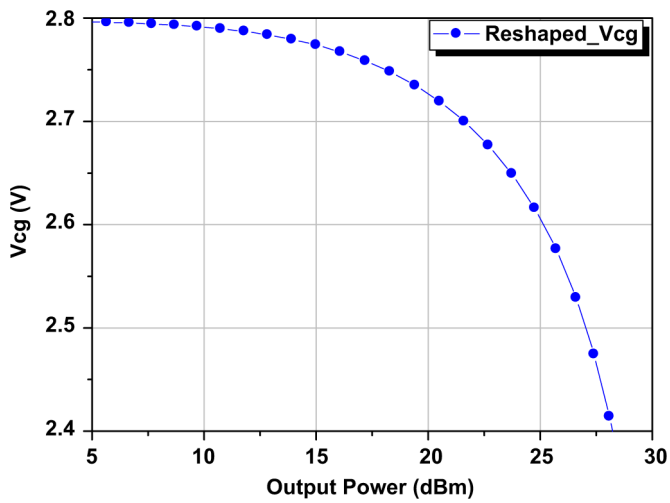

Fig. 4. Simulated optimally shaped gate bias of the CG device according to the output power.

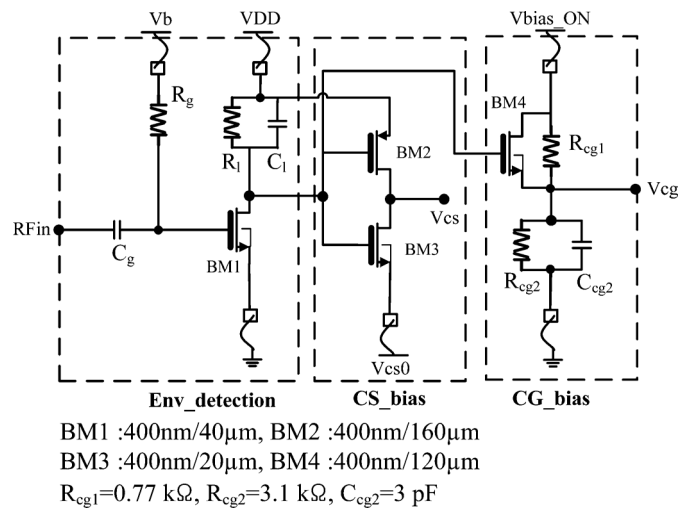

Fig. 6. Schematic of the proposed adaptive bias circuit for the gates of the CG and the CS stages.

with 10-MHz tone spacing at 1.85-GHz center frequency are depicted in Fig. 3. For the simulation, the gate bias of the CS is fixed at 0.46 V and that of the CG is varied. The gain deviation that causes AM-AM distortion decreases with increasing the CG gate bias. In contrast, the IMD3 behavior is quite complicated according to the CG gate bias. For a linear operation, the CG gate bias should be high (2.8 V) for output power less than 23 dBm and low (2.4 V) for over 23-dBm output power. Fig. 4 shows the optimum CG gate bias for the linearity according to the output power level. When the optimal CG gate bias is applied to the PA, the gain deviation and IMD3 are improved simultaneously by 2 dB and 6 dB, respectively, in the wide range of the low output region as shown in Fig. 5. Therefore, we use this optimally shaped CG bias to improve the linearity and gain deviation at the low power region, while the PA operated in a deep class-AB bias to get the better performance at the high power region. We have already reported the measured adjacent channel leakage ratio (ACLR), gain and power-added efficiency (PAE) as a function of the average output power with the CG gate bias [15]. For a 10-MHz bandwidth LTE signal at 1.85 GHz, the PA with the proposed bias circuit improves ACLR_{E-UTRA} ranging from 7.0 dB to 2.5 dB over the constant bias circuit. Therefore, the PA with the CG bias has a significant improvement in ACLR, which is affected by the reduction of the AM-AM distortion and IMD3.

An envelope signal injection to the gate of the CS stage can improve the linearity at high power regions as reported in [26], [27]. To further improve the performance of the CMOS PA, the envelope injection technique is adopted using a class-D bias circuit [19]. To simplify the adaptive bias circuits, the envelope injection circuit is merged with the CG bias circuit. The schematic of the adaptive bias circuit is shown in Fig. 6. The integrated adaptive bias circuit consists of three parts: an envelope detector, CS bias and CG bias. The envelope detector amplifies the input signal (RF_{in}) using the NMOS device (BM1) and rejects RF carrier signal using the resistor (R_l) and capacitor (C_l) networks. A class-D envelope amplifier (BM2 and BM3) injects an envelope signal into the gate of the CS stage with the initial gate bias $(\mathrm{V}cs0)$, and a voltage divider bias circuit with the NMOS device (BM4) controls the gate bias of the CG stage. When the

input envelope signal increases, the output node of envelope detector decreases, the PMOS (BM2) of the envelope amplifier begins to charge the V_{cs} from the initial value $(\mathrm{V}cs0)$ to the optimum value, and the resistance of the NMOS (BM4) increases to make the gate voltage of the CG stage (V_{cg}) from the initial value to a lower value. Controlling the bias from class-A to class-B of the CG stage is determined by the voltage difference between the Vcg and the drain voltage of the CS stage. As the input power increases, the V_{cg} decreases. Therefore, the class of the CG stage moves from A to B due to the decreasing voltage difference. It is difficult to design an envelope injection circuit for a wide bandwidth signal because the performance of the circuit degrades as the signal bandwidth increases. For reliability, all transistors of the bias circuits employ thick oxide devices to prevent the breakdown.

As mentioned earlier, the gate bias circuits operate at the envelope signal, generating large memory effects. Therefore, we employ the second harmonic control circuits at the source of the CS and the gate of the CG stages to eliminate the sideband asymmetry (IMD or ACLR). In the next section, the memory effect reduction technique for the PAs will be discussed in more detail.

III. Memory Effects Reduction Using Second-Order Harmonic Control

A. Investigation on Memory Effect in RF Amplifiers

The memory effect is mainly caused by the reflections of the envelope frequency and second harmonics at the device terminals [28]. Hence, to reduce the sideband asymmetries, it is the best practice to short the envelope impedance. In a real device, to make a short circuit condition at the envelope impedance $(\Delta\omega)$, a low-pass filter consisting of external components is needed to generate a large time constant [29]. These filters can also lead to AM-PM distortion in the PA. Therefore, control of the second harmonic (2ω) impedances can be a practical solution to reduce the sideband asymmetries, as proposed in [30].

To analyze the causes of the memory effects, we review the regeneration process of the IMD that were introduced in earlier studies [31]. The drain current (i_d), the most significant nonlinear distortion source, can be expanded in the following two dimensional Taylor-series, where only the dominant terms are included

$$i_d(v_g, v_d) = G_m v_g + G_d v_d + G_{m2} v_g^2 + G_{d2} v_d^2 + G_{md} v_g v_d + G_{m3} v_g^3 + \cdots \quad (2)$$

where v_g and v_d is the gate and drain signal voltages, and the G terms represent the transconductance, drain conductance and cross terms, respectively. The higher order nonlinearities are ignored to reduce the complexity of the analysis. The optimum load impedance of the PA at the fundamental frequency $(\mathrm{R}_L\,(\omega_c))$ is a pure real value due to the resonance of the imaginary part. Assuming the same amplitude two-tone input signal of A, including with the envelope injection, the input signal v_s is given by

$$v_s(t) = A[\cos(\omega_1 \cdot t) + \cos(\omega_2 \cdot t)] + B\cos(\Delta\omega \cdot t) \quad (3)$$

is applied, the lower and upper IM3s of the drain voltage can be derived [32], [33] and simplified as

$$V_{d3}(2\omega_2 - \omega_1) = R_L(\omega_c) \cdot [\, \frac{3}{4} G_{m3} A^3 + \frac{1}{2} Z_L(\omega_2 - \omega_1) G_{m2} \cdot (G_{md} A^3 + 2AB) + \frac{1}{4} Z_L(2\omega_c) G_{m2} G_{md} A^3 \,] \quad (4)$$

$$V_{d3}(2\omega_1 - \omega_2) = R_L(\omega_c) \cdot [\, \frac{3}{4} G_{m3} A^3 + \frac{1}{2} Z_L(\omega_1 - \omega_2) G_{m2} \cdot (G_{md} A^3 + 2AB) + \frac{1}{4} Z_L(2\omega_c) G_{m2} G_{md} A^3 \,] \quad (5)$$

where ω_1 and ω_2 are the lower and upper two-tone input frequencies, respectively, $\Delta\omega$ is the difference frequency of $(\omega_1 - \omega_2)$, ω_c is the center frequency of $(\omega_1 + \omega_2)/2$, and Z_L is the frequency-dependent load impedance which generates a memory through its imaginary part. The significant difference between the (4) and (5) is the phase $(\theta(\Delta\omega) = \tan^{-1}[\mathrm{Im}(Z_L(\Delta\omega))/\mathrm{Re}(Z_L(\Delta\omega))])$ of the envelope IM3 terms that are changed to the opposite direction according to the tone spacing, while the second harmonic IM3 terms have the same phase $(\theta(2\omega) = \tan^{-1}[\mathrm{Im}(Z_L(2\omega))/\mathrm{Re}(Z_L(2\omega))])$. Therefore, in (4) and (5), the resultant IM3 terms are generated through composition of the third-order nonlinearity (intrinsic IM3) and the two second-order and fundamental interacted nonlinearities (memory IM3). Since the intrinsic IM3 is almost a real value due to the real fundamental load impedance, the term does not generate the memory. On the other hand, the second-order terms can generate the memory effects.

There are two cases that can eliminate the sideband asymmetries; the second harmonic load termination is real or shorted and the load at the envelope frequency is terminated at a short-circuit condition. However, it is preferred to have a shorted second harmonic termination because of the resulting lower IMD3 and the needs of large external capacitors to terminate the envelope signal.

B. Control of Second Harmonic Impedances in a Differential Cascode PA

A differential cascode amplifier has two common nodes , one at the source of the CS and another at the gate of the CG stage. The common nodes create a virtual ground at odd harmonics, including the fundamental frequency, but they do not create a ground at even harmonics. The low-impedance terminations at the common nodes for the even harmonics are essential for a RF amplifier design. In the real device, however, it is difficult to make the low-impedance condition at the envelope and second harmonic frequency at the nodes of devices if a harmonic control circuit is not provided, as explained in [30]. If the source impedance of the CS stage does not terminate at the second harmonic, the linearity of the amplifier is deteriorated by the series feedback of the impedance. From (4) and (5), the gate impedance of the CG stage, which is a part of the output load seen by the CS stage, should be terminated properly. This termination allows significant reduction of the memory effects and second-order nonlinear distortions.

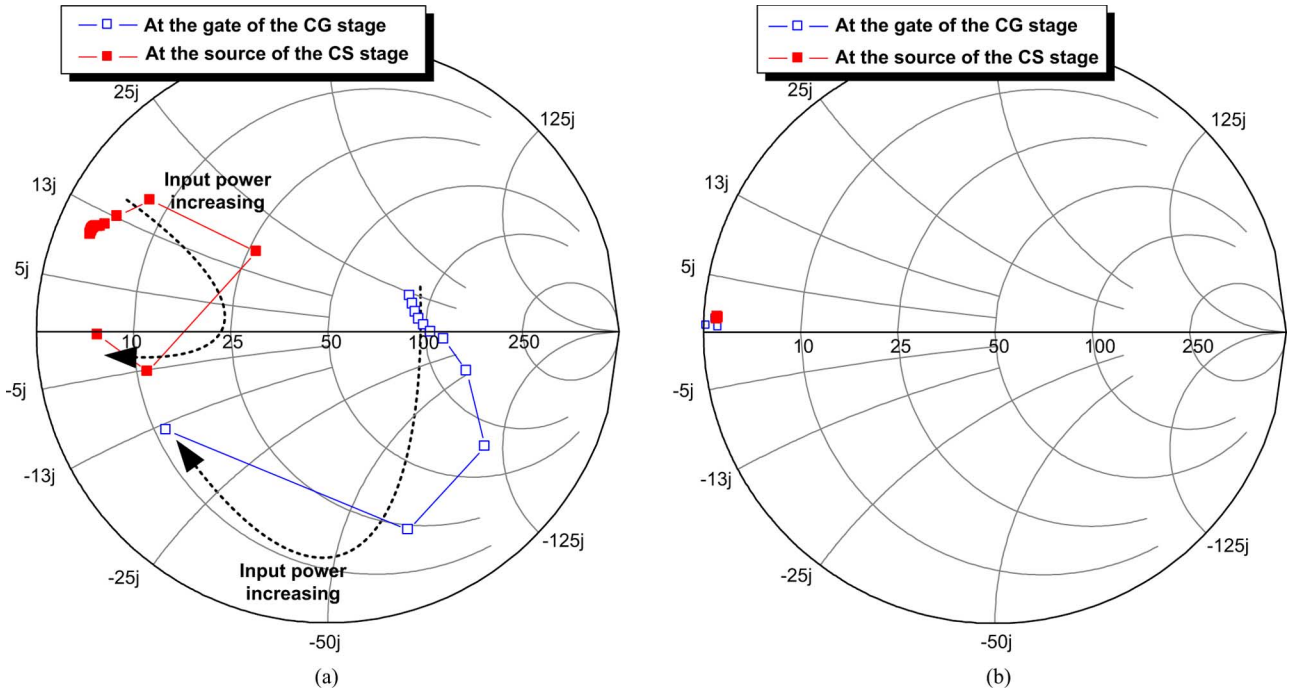

Fig. 7. Second harmonic impedances at the gate of the CG and the source of the CS stages according to input power (a) without and (b) with second harmonic control circuits.

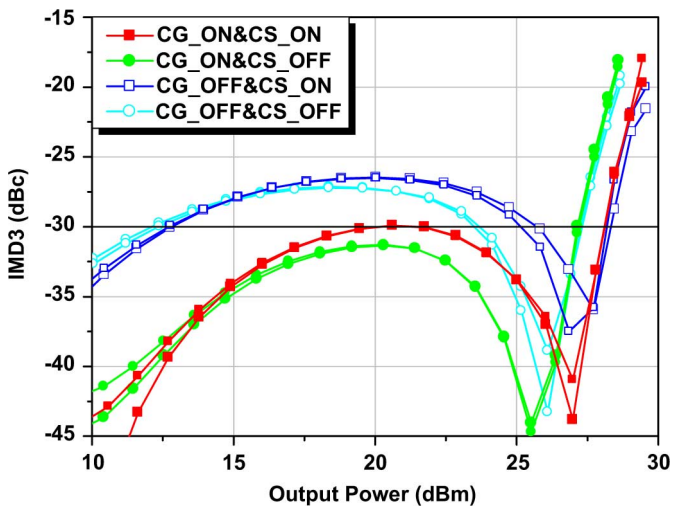

Fig. 8. Simulated IMD3s according to the output power for the two linearizations at the gate of the CG and the source of CS stages. The harmonic control circuits are employed for the four cases: CG_ON&CS_ON, CG_ON&CS_OFFCG_OFF&CS_ON, and CG_OFF&CS_OFF. The constant biases (CG_OFF or CS_OFF) are $\mathrm{Vcg0} = 0.46\,\mathrm{V}, \mathrm{Vcg0} = 2.4\,\mathrm{V}$. 'CG_ON': optimal reshaped bias at the gate of the CG amplifier, and 'CS_ON': envelope injection at the gate of the CS amplifier.

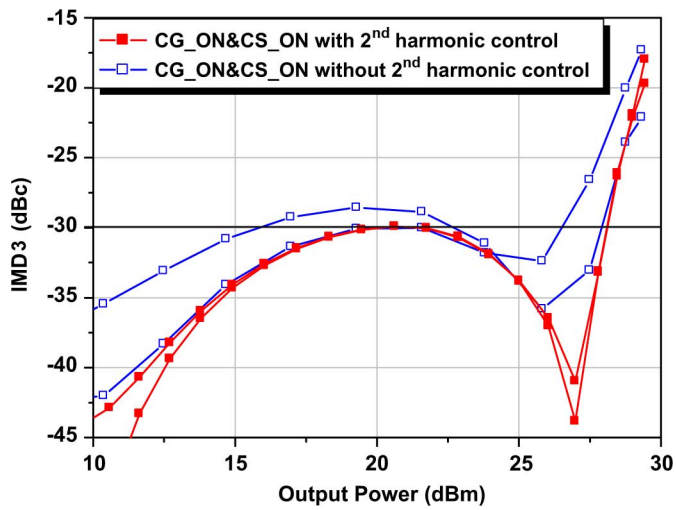

Fig. 9. Simulated IMD3s according to the output power with/without the second harmonic control circuits at the gate of the CG and the source of the CS stages. The adaptive bias circuits at the gate of the CG and the gate of CS stages circuits are employed.

Fig. 7(a) shows the second harmonic impedances at the gate of the CG and the source of the CS stages of the PA according to the input power at 1.85-GHz frequency. As shown, the both second harmonic impedances are not properly shorted. These second harmonic impedances can make the sideband asymmetric and degrade the IMD3 by (4) and (5). After applying the second harmonic control circuits, the second harmonic impedances at the common nodes are properly terminated to a short-circuit condition, as shown in Fig. 7(b).

To verify the linearization techniques, a simulation result of the IMD3 using a two-tone input signal with spacing 10 MHz at 1.85-GHz center frequency is performed. For the four cases in each adaptive bias circuit, the simulated IMD3s are compared in Fig. 8. At the low and mid power regions, the CG bias circuit improves the IMD3 without degrading IMD3 at the high power region, whereas the CS bias circuit improves the IMD3 at the high power region, significantly. Therefore, through the combination of each bias circuit, the linearity and efficiency of the PA can be improved at the overall range of the output power.

Even though the proposed PA employs the envelope signal injection and the adaptive CG bias control at each gate, the memory effects can be suppressed by the second harmonic control, as shown in Fig. 9. This result verifies that almost all of the memory effects in the PA can be suppressed, when applying

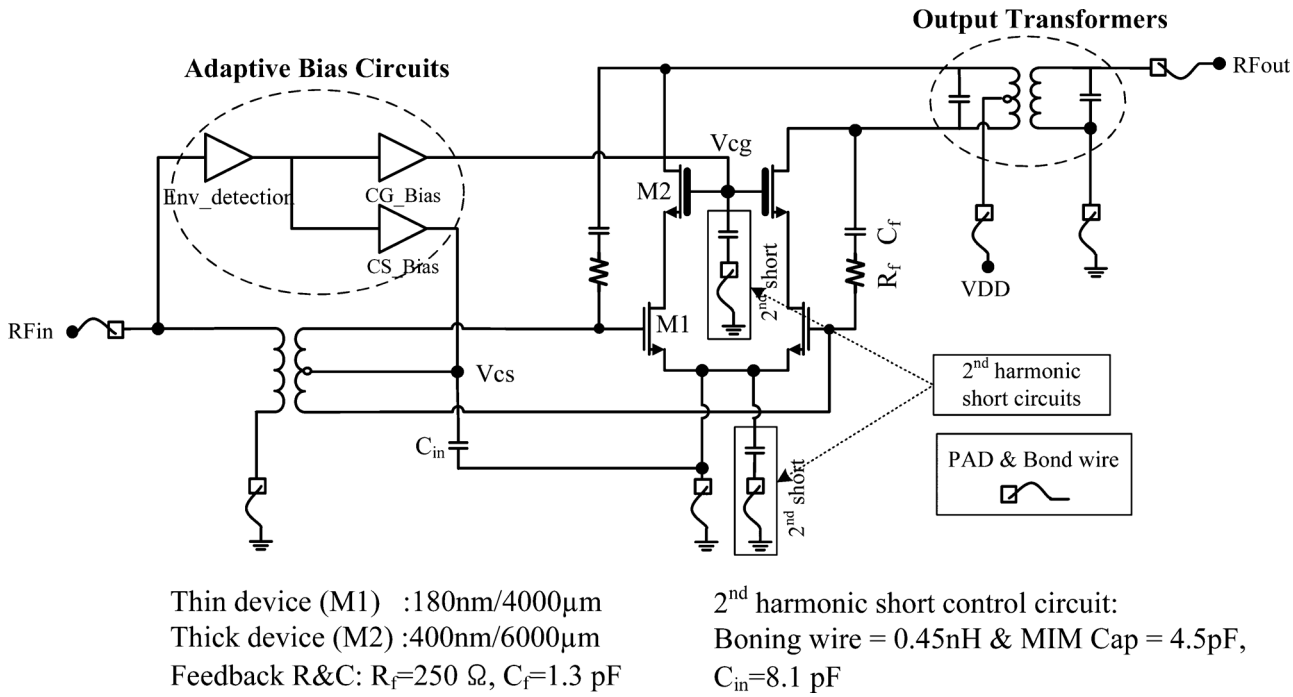

Fig. 10. Overall schematic of the fully-integrated CMOS PA with the adaptive bias circuits.

the second harmonic control circuits at the common nodes. As a consequence, we can improve the linearity performance of the PA using the adaptive gate bias circuits with reduction of the sideband asymmetry.

IV. Implementation and Measurement Results

A. Implementation

The schematic of the differential cascode PA with the proposed adaptive bias and harmonic control circuits is shown in Fig. 10. A thick-oxide $0.4-\mu\mathrm{m}$ device for the CG stage and thin-oxide $0.18-\mu\mathrm{m}$ device for the CS stage are stacked in a cascode structure to mitigate the problem of the low breakdown voltage. The total gate width of the thin and thick devices are $4000\ \mu\mathrm{m}$ and $6000\ \mu\mathrm{m}$, respectively. A feedback network with series resistor $(250\ \Omega)$ and capacitor (1.3 pF) between the drain of the CG and the gate of the CS is used to improve linearity and stability.

The second harmonic control circuit is composed of a MIM capacitor (4.5 pF) and an inductor (0.45 nH) implemented by a down-bonding wire, which is designed to resonate at the second harmonic frequency. To further reduce the gate-source voltage of the CS stage, C_{in} (8.1 pF) is employed to short the second harmonic impedance.

The insertion loss of the output power combiner in a differential structure is mainly dependent on a quality factor of the material to build it. For comparison purposes, two PAs are fabricated: PA1 is a fully-integrated version with an on-chip transformer, which means that all the matchings are on-chip; PA2 is the same as PA1 except that its output matchings are off-chip using printed circuit board (PCB) lines, which have a thicker metal than that of the CMOS one to reduce the insertion loss. The only difference between the two PAs is the configuration of the output matching network. The optimum output impedance of the power cell is 6–7 ohm at each cell, which

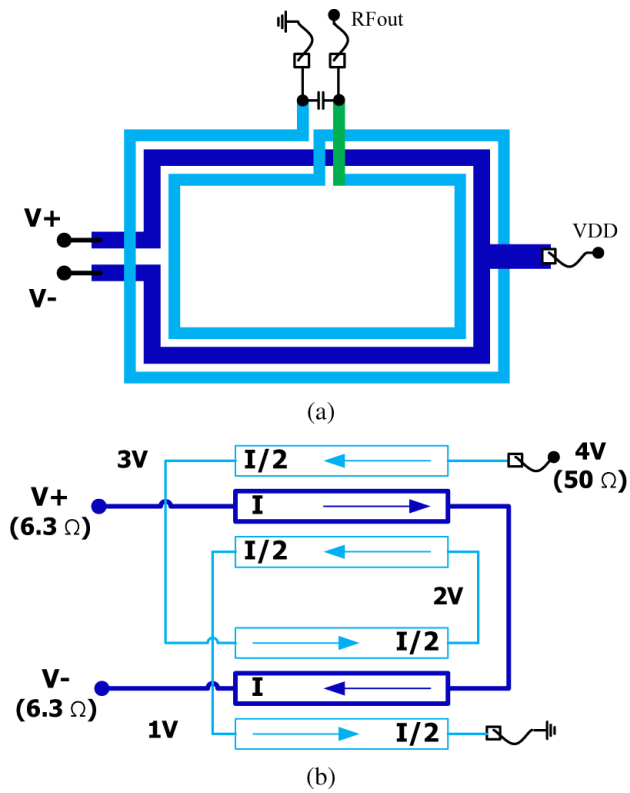

Fig. 11. (a) Layout and (b) schematic of the proposed 1:2 on-chip transformer.

is determined through the load-pull simulation. Generally, the transformer occupies about 60% of the total PA area. To reduce the size of the on-chip transformer and match directly to the optimum output impedance, 1:2 transmission-line transformer (TLT) is employed as shown in Fig. 11. The spacing between the primary and secondary of the transformer is $10\ \mu\mathrm{m}$. The widths

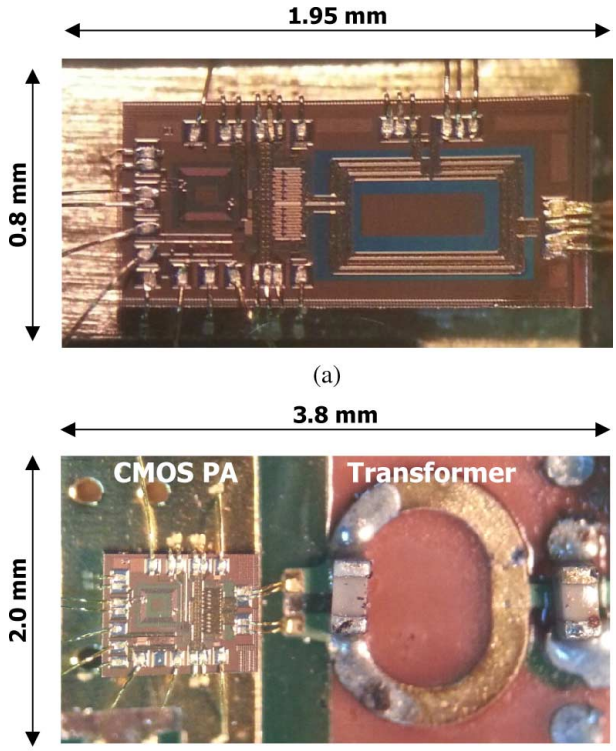

Fig. 12. Microphotographs of two designed CMOS PAs. (a) with on-chip transformer (PA1) and (b) with off-chip PCB transformer (PA2).

of the primary and secondary are 35 μm and 20 μm, respectively. The size of the on-chip output transformer is 0.85 mm $\times 0.54$ mm, and the insertion loss including the two matching capacitors is 1.15 dB at 1.85 GHz. In contrast, the insertion loss of the off-chip output matching network, including the two external chip capacitors, is 0.54 dB at 1.85 GHz and its size is 1.9 mm $\times 1.9$ mm. The PAs with the proposed bias circuits are fabricated using a $0.18-\mu$m RF CMOS technology. The fully-integrated chip (PA1) and the off-chip output transformer based chip (PA2) occupy an area of 1.95 mm $\times 0.80$ mm and 3.8 mm $\times 2.0$ mm, including the bonding pads, respectively. Therefore, there are trade-off relationships of the size (cost) and the insertion loss in the two transformers.

B. Measurement Results

The chip dies are directly attached to the ground plane of the PCB of FR-4 using an electrically conductive silver epoxy. All signal and bias feeding pads are wire bonded to the PCB with gold wires. Since all of the matching circuits are integrated on-chip in the PA1, there is no external component on the PCB. The bias condition of the PAs with no input signal is a 3.5-V supply voltage and 42-mA current. Micrographs of the two fabricated PAs are presented in Fig. 12.

For the two PAs, the two-tone signal measurement is performed at a 1.85-GHz center frequency with 10-MHz tone spacing. Fig. 13 shows the measured IMD3s and IMD5s of the PA1 as a function of the output power using the CG bias circuit, but with different linearizations: the on/off status of the CS bias circuit and with/without the second harmonic control. The IMD5 is also improved at the overall range of the output power

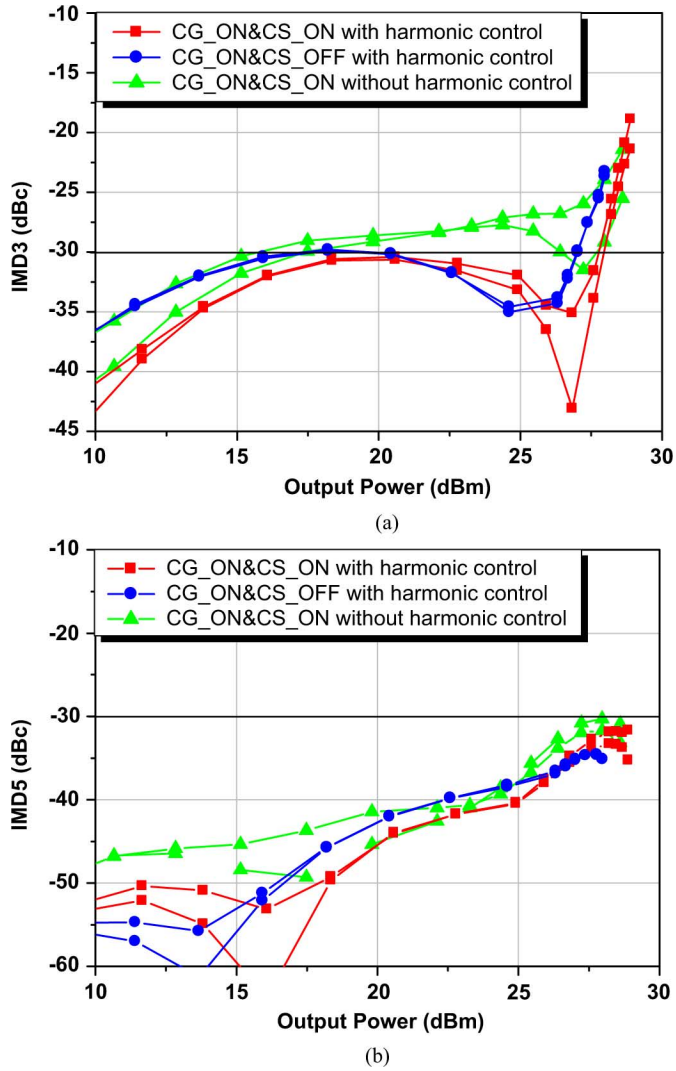

Fig. 13. Measured IMD3s (a) and IMD5s (b) according to the output power of the PA with on-chip transformer (PA1) for optimally shaped CG bias circuit but with different linearizations (CG_ON): the ON&OFF status of envelope signal injection to the gate of the CS stage (CS_ON&CS_OFF) and with/without the second harmonic control circuits at the gate of the CG and the source of the CS stages.

when the bias and harmonic control circuits are applied and the IMD5 is always lower than the IMD3. With the proposed linearization techniques, the peak linear output power and PAE are improved significantly. Also, the sideband asymmetry of the upper and lower IMD3s is not observed except at the sweep-spot region. Fig. 14 shows the measured gain, PAE, and IMD3 of the PA1 with respect to the output power together with the simulation results. The measurement and simulation results are in a good agreement as shown in the figure.

For a LTE application, the fabricated PAs are tested with 10-MHz bandwidth 16-QAM 7.5-dB PAPR LTE signal. The ACLR is measured under evolved universal terrestrial radio access (E-UTRA) specification with a 9-MHz resolution bandwidth at a 1.85-GHz center frequency and a 10-MHz offset. To check effects of the signal bandwidth to the adaptive bias circuits, the PA is tested using the LTE signal with 10–50-MHz channel bandwidths at 1.85 GHz. Even though the measured ACLR_{E-UTRA} is degraded as the signal bandwidth increases,

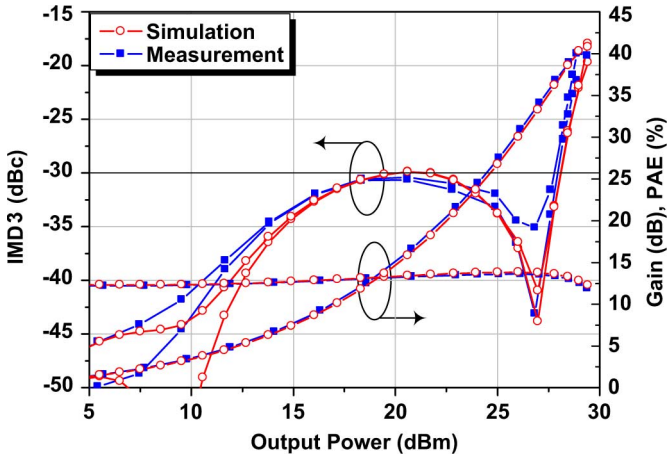

Fig. 14. Simulated and measured Gain, PAE, and IMD3 of the PA1 with the adaptive bias (CG_ON&CS_ON) and the second harmonic control circuits.

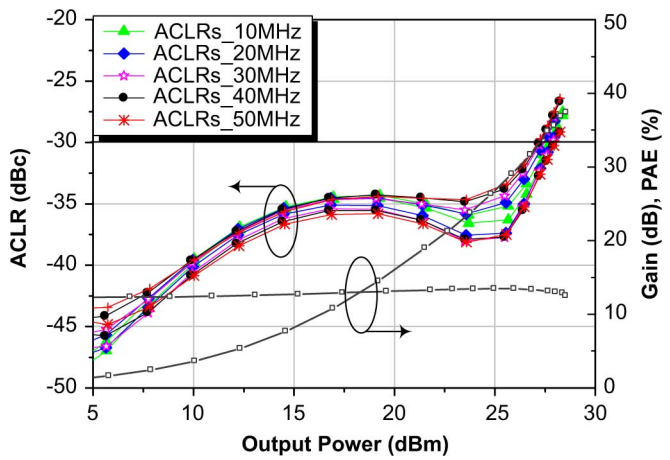

Fig. 15. Measured ACLRs for different bandwidth of the LTE signal (10–50 MHz) at 1.85 GHz of the PA1 with the adaptive bias (CG_ON&CS_ON) and the second harmonic control circuits.

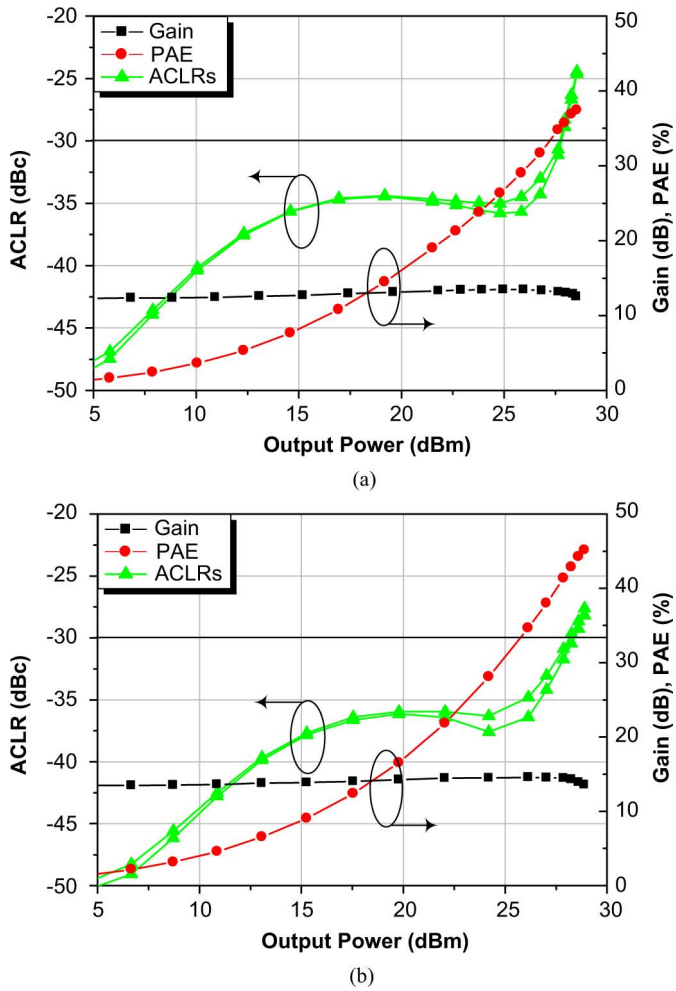

Fig. 16. Measured performances of the designed PAs with two proposed linearization at the gate of the CG and the source of the CS stages for the 10-MHz LTE signal at 1.85 GHz: (a) on-chip transformer (PA1) and (b) off-chip PCB transformer (PA2).

the PAE and gain are the same and the maximum degradation of the linear output power is only 0.4 dB at an ACLR_{E-UTRA} of -30 dBc, as shown in Fig. 15. The measured performances of the PAs to confirm the LTE operation at 1.85-GHz center frequency are shown in Fig. 16. The PA1 and the PA2 can deliver an average output power and PAE of 27.5/27.8 dBm and 35.2/41.0%, respectively, with an ACLR_{E-UTRA} of -31.0 dBc and an error vector magnitude (EVM) of 4.6%. The maximum difference between the lower and upper ACLR_{E-UTRA} is less than 1.5 dB across all the output power level. The measured ACLR_{E-UTRA} and EVM satisfy the LTE specifications of -30 dBc and the industry requirement of 5.6%, respectively. The proposed PAs has significant improvements in average PAE and ACLRs by controlling the bias condition of gates and reducing the sideband asymmetries. The peak average output power and PAE of the PA1 are improved by 1.2 dB and 6.0%, respectively, compared to previous work [15]. The performances of our PAs are compared with recent state-of-art PAs for wireless communication applications and are summarized in Table I. In this work, the designed PA with the proposed linearization can deliver highly linear and efficient performances without DPD and envelope-tracking (ET) techniques.

V. Conclusion

Highly linear and efficient CMOS PAs with adaptive gate bias control circuits has been developed. We have demonstrated linearization techniques using the proposed gate bias circuits together with the harmonic control circuits in the PA for handset applications. The envelope injection bias circuit, which properly injects the envelope signal into the gate of the CS stage, improves the IMD3 by canceling the distortions in the PA at a high power region. By applying the optimized bias to the CG stage, the PA can be operated at a deep class-AB bias of the CS stage through the reduction of gain deviation and distortions. Because these gate bias circuits generate memory effects, the second harmonic control circuits at the source of the CS and the gate of the CG stages have been used to eliminate the sideband asymmetry (IMD or ACLR). These bias circuits with the harmonic control circuits improve the peak average output power and PAE significantly. The measurement results show maximum 1.5-dB sideband asymmetric of ACLR_{E-UTRA} and $1.2-$ dB improvement in a peak average power. The PAs with integrated TLT and PCB-based transformer deliver a PAE of 35.2/41.0%, an average output power of 27.5/27.8 dBm, respectively with an ACLR_{E-UTRA} of -31.0 dBc and EVM

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART RESULTS

Ref.	Modulation	Freq. (GHz)	P_{out} (dBm)	PAE (%)	EVM* (%)	Output matching	PA Technology	Characteristic
[34]	LTE 20-MHz	2.53	29.0	43.0	1.9	Off-chip	HBT	ET-based PA with DPD
[35]	LTE 16-QAM 10-MHz	0.93	25.1	15	5.6	On-chip	CMOS 90-nm	clover shape DAT 2-V supply
[36]	WLAN 64-QAM 20-MHz	2.4	26.5	39.3	4.9	Off-chip	HBT	Two-stage dual-bias circuit
[37]	LTE 16-QAM 10-MHz	1.74	27.0	39.8	3.8	Off-chip	HBT	ET-based PA dual-mode
[9]	WLAN 64-QAM 20-MHz	2.4	19.5	24.8	5.6§	On-chip	CMOS 0.13-μm	MGTR Gate bias circuit
[38]	LTE 16-QAM 5-MHz	1.75	24.2	43.0	4.8	Off-chip	SiGe BiCMOS 0.35-μm	ET-based PA
[30]	LTE 16-QAM 50-MHz	1.4 - 2.0	27.5 - 27.1	36.5 - 31.2	4.7†	On-chip	CMOS 0.18-μm	broad & wideband operation
This work	LTE 16-QAM 10-MHz	1.85	27.8	41.0	4.6	Off-chip	CMOS 0.18-μm	ABC‡ with harmonic control
			27.5	35.2	4.6	On-chip		

* LTE standard specifications (industry): EVM $<$ 12.5% (5.6%).
† EVM data with 20-MHz bandwidth LTE signal
‡ ABC : Adaptive Bias Circuits for the CG and CS devices
§ represented EVM in the paper: -25 dB, converted EVM: 5.6%

of 4.6% at 1.85-GHz for a 10-MHz bandwidth 16-QAM 7.5-dB PAPR LTE signal. These results verify that the proposed design can deliver efficient linear power amplification for mobile wireless applications. This proposed linearization technique is a practical solution for implementing CMOS PAs for handset applications.

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