A Polar Transmitter With CMOS Programmable Hysteretic-Controlled Hybrid Switching Supply Modulator for Multistandard Applications

Jinsung Choi, *Student Member, IEEE*, Dongsu Kim,
Daehyun Kang, *Student Member, IEEE*, and Bumman Kim, *Fellow, IEEE*

***Abstract*—This paper presents the realization of a linear polar transmitter supporting multistandard applications. The harmonic-tuned class-AB biased (class-AB/F) power amplifier (PA) with the novel envelope shaping method linearly amplifies the input signal with high efficiency. The hybrid switching supply modulator with programmable hysteretic comparator enables the multimode operation whatever the envelope signal characteristics such as the peak-to-average power ratio and the bandwidth are. The designed polar transmitter is fabricated with CMOS 0.13-μm technology and InGaP/GaAs 2-μm HBT process for the supply modulator and the PA, respectively. For the IEEE 802.16e m-WiMax signal, it shows a power-added efficiency (PAE), an average output power ($P\mathrm{out}$), and a gain of 34.3%, 23.9 dBm, and 27.9 dB, respectively. Without any predistortion techniques, it satisfies the overall spectrum emission mask specifications. The relative constellation error and the error vector magnitude for the m-WiMax signal are −30.5 dB and 2.98%, respectively. For a WCDMA signal, it presents a PAE, a $P\mathrm{out}$, and a gain of 46%, 29 dBm, and 27.8 dB, respectively. For the EDGE signal, it delivers a PAE of 45.3% at a $P\mathrm{out}$ of 27.8 dBm with a gain of 29.4 dB. There is about a 7% improvement of the overall PAE for EDGE through the optimum multimode operation.**

***Index Terms*—CMOS analog integrated circuits (ICs), dc–dc power conversion, multimode, power amplifiers (PAs), transmitters, wireless communication.**

I. Introduction

As MULTIPLE handheld devices are merged into a single mobile unit, an energy-efficient unit is required for long battery time within the limited power resource. The power amplifier (PA), which is the most energy-consuming component, should have a high efficiency with a good linearity. As the data rate increases within a limited bandwidth, the peak-to-average power ratio (PAPR) gets higher. This results in the PA operating at a backoff region for the linearity, where the efficiency of the PA is not high. To enhance the low efficiency at the backoff region, many types of efficiency enhancement techniques have been investigated for a long time [1]–[12].

The polar transmitter is ideally an optimum structure, which has very high efficiency at all power ranges assuming a highly efficient PA and supply modulator are used. The assumption, however, is very difficult to achieve, especially for the supply modulator, because of the limited bandwidth of the high-efficiency switching amplifier and the low efficiency of the wide bandwidth linear amplifier. In [4], they have designed a fully integrated CMOS supply modulated PA for global system for mobile communications (GSM)/EDGE. It employed a low dropout (LDO) regulator to modulate the high-efficiency class-E PA. However, for a high PAPR signal such as orthogonal frequency-division multiplexing (OFDM), efficiency of the LDO is not high enough, and the CMOS PA still provides a low efficiency even if it employs high-efficiency topologies. There are some movements to utilize a switch-mode power supply for its high efficiency. In [12], they have employed a 130-MHz switch-mode power supply, which converts the time-varying envelope signal to a binary pulse wave. This signal is then amplified and filtered to recover the input waveform. To get a highly linear output signal, a second-order low-pass filter is employed. It induces a large form factor and power loss. Moreover, the available bandwidth is limited by the switching frequency, while the efficiency is inversely proportional to it. If a high-speed device based on nm-CMOS technology is available, a high-efficiency switching amplifier operating at the high switching frequency can be realized with a good circuit design technique [13].

Recently, some researchers have combined the advantage of the wide-bandwidth linear amplifier and the high-efficiency switching amplifier in various ways [8]–[11]. Kitchen *et al.* [8] have combined the LDO regulator with the switching regulator to boost up efficiency of the LDO while maintaining the linearity. Compared to the standalone LDO, the efficiency is increased, but this architecture has a limitation in achieving high efficiency at a low output voltage because the voltage drop across the PMOS in the LDO is larger than $V_{\mathrm{sat.}}$ at the low output voltage. Kwak *et al.* [9] have employed a master–slave architecture using a wideband linear class-AB amplifier and a high-efficiency switching amplifier, i.e., the hybrid switching amplifier (HSA). To provide most of the current to the load

Manuscript received November 18, 2008; revised March 05, 2009. First published May 27, 2009; current version published July 09, 2009. This work was supported by the Korean Government (MOST) under Korea Science and Engineering Foundation (KOSEF) Grant R01-2007-000-20377-0, by the Ministry of Knowledge Economy, Korea, under the Information Technology Research Center (ITRC) Support Program supervised by the Institute of Information Technology Advancement (IITA) (IITA-2009-C1090-0902-0037), and by the Electronics and Telecommunications Research Institute (ETRI) System-on-Chip (SoC) Industry Promotion Center, Human Resource Development Project for Information Technology (IT) SoC Architect.

The authors are with the Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk 790-784, Korea (e-mail: jinsungc@ieee.org).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2009.2021880

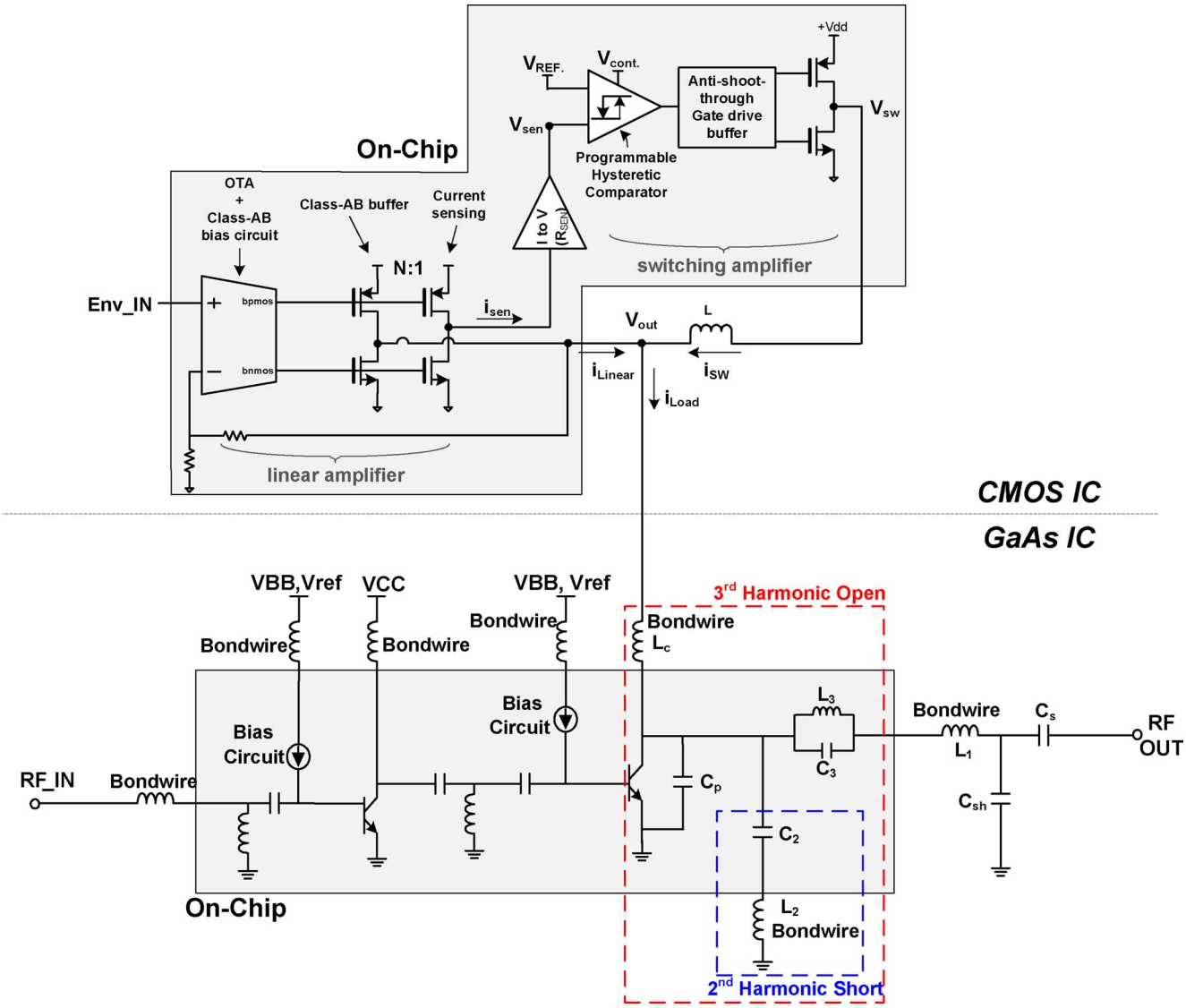


Fig. 1. HBT class-AB/F PA with CMOS programmable hysteretic-controlled supply modulator.

through the switching amplifier, the pulsewidth modulation with a high switching frequency (5–10 times of the signal bandwidth) is used. This design approach delivers a very high efficiency, but the bandwidth of the linear amplifier should cover the switching frequency to compensate the ripple from the switching converter. In [10] and [11], they have modified the design of the HSA by alleviating the burden of the switching amplifier. The switching amplifier does not follow most of the high slew-rate load current any more, and it operates as a quasi-constant current source. The linear amplifier supplies and sinks the current to regulate the load according to the envelope signal. Fortunately, this topology is very suitable for the envelope signal of the modern wireless communication system, which has most of the power at the low-frequency region. Even though the concept of the HSA is changed, the high-efficiency switching amplifier still provides most of the current required for the load.

While the literature up to date reports various designs of high-efficiency supply modulators for the *supply modulated PA*, some of them have just employed the conventional linear PA whose efficiency is not high enough, and others have designed their own PA, but not an optimum design for the high-efficiency handset transmitter application. Moreover, it is designed only for a specific single application. Also, the linkage between the supply modulator and PA is not carefully considered to maximize the efficiency and linearity.

In this paper, we present a fully integrated two-chip solution for the polar transmitter, as illustrated in Fig. 1, consisting of a high-efficiency class-AB/F HBT PA and a high-efficiency CMOS supply modulator supporting multistandard applications. In Section II, the needs for the supply modulated PAs are presented. In Section III, the novel envelope shaping method is presented. Section IV provides the design and circuit implementation of the multimode supply modulator. The experimental results are presented in Section V. The designed polar transmitter supports multistandard applications such as EDGE, WCDMA, and m-WiMax with excellent efficiencies.

II. High-Efficiency Class-AB/F PA for Linear Polar Transmitter

The high-efficiency switching amplifier like a class-E PA is commonly used for the polar transmitter because the input of the PA only contains the phase information. However, the spectral regrowth during conversion from in-phase/quadrature (I/Q) to polar signal burdens the broadband input matching for the PA. Moreover, the feed-through of the input signal at the zero envelope power deteriorates the linearity, especially AM–AM. Thus, the input of the PA is preferred to be a complex modulation signal containing the envelope and phase information together. In addition, as the switching amplifier generates a large amount of third-order intermodulation (IM3) components requiring the additional linearization technique, the harmonic-tuned class-AB biased (class-AB/F) PA is employed here to avoid the burden of power dissipation by digital signal processing [digital pre-distortion (DPD)] [17].

Compared with the class-E PA, the class-AB/F PA has a lesser stress issue for the peak voltage. The maximum output voltage swing is just two times of the supply voltage. It has a conduction angle of π with an harmonic control circuit located in front of the matching circuit. This can control the impedance appropriately for the saturated operation. The half sinusoidal output current at the device output generates a flatten square periodic voltage through the harmonic control. This saturated amplifier ideally delivers 100% efficiency with a high power density if all the harmonics are properly controlled [14].

Not only does it shows high efficiency and high power density, it also presents an acceptable linearity with the class-AB bias condition [15]–[17]. It is appealing in the aspect that the painful effort to the DPD technique can be fairly alleviated or removed. In the monolithic integrated circuit (IC) application, however, the class-AB/F PA has been an unwelcome topology for the complexity and the difficulty in achieving the perfect harmonic control circuit. Usually, therefore, the harmonics are controlled up to third order, and even this has been implemented off chip. The main obstacle to the on-chip implementation of the harmonic control circuit is the low-Q factor of the on-chip spiral inductor. This inductor can be replaced with a high-Q slab inductor through its careful electromagnetic simulation. It enables higher third harmonic impedance and lower loss, resulting in higher efficiency. The above-mentioned merits of the class-AB/F PA (less stress on the device, acceptable linearity, high power density, and high efficiency through the on-chip harmonic control circuit) make it more attractive to the application for the supply modulated handset PA integrated circuit (IC).

III. Envelope Waveform Shaping Method

For the infinite peak-to-minimum power ratio of the modern wireless communication system such as OFDM, the supply modulator should have a rail-to-rail swing range at the output. Even if the supply modulator does it, the PA shows nonlinear characteristics, especially AM/PM, at the supply voltage below the knee region [18]. It usually does not matter for a low PAPR signal [12] since most of the supply voltage is modulated above one-half the V_{dd}, where the $V_{dd}(t)$ to $V_{\rm out}(t)$ and the $V_{dd}(t)$ to $\phi(t)$ are not serious. However, as the PAPR of the signal

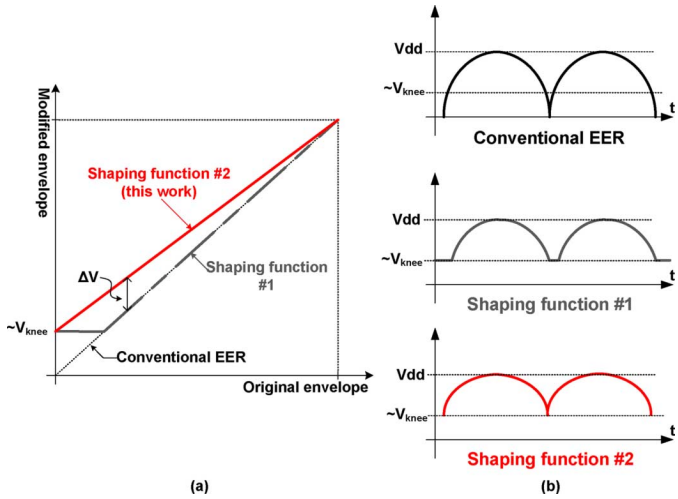


Fig. 2. Novel envelope shaping method for linear amplification. (a) Transfer function. (b) Time-domain waveforms.

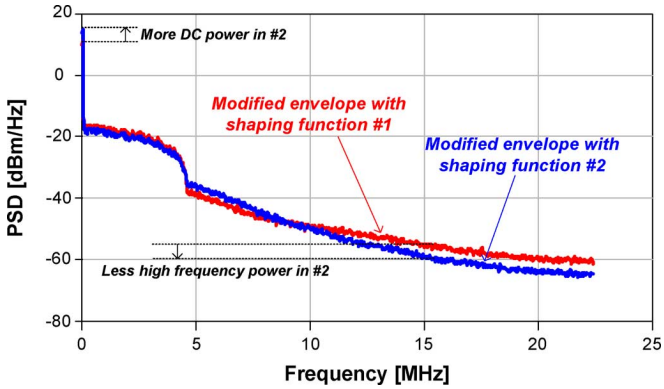


Fig. 3. Spectra of the modified envelope with shaping function #1 and #2.

increases, the average supply voltage of the PA is lowered so that it spends most of the time at a low V_{dd}, where the nonlinearity is significant.

To overcome the problem, a novel envelope waveform shaping function shown in Fig. 2 is employed in this work. It can be defined as

$$\text{Envelope}' = \left(1 - \frac{V_{\rm knee}}{V_{\rm peak}} \cdot 10^{x/20}\right) \cdot \text{Envelope} + V_{\rm knee} \quad (1)$$

where x is the power backoff level from the maximum average output power. Compared with the general shaping function (#1), which just clips the low-level signal, the proposed shaping function presents less high-frequency power so that the bandwidth requirement of the supply modulator is alleviated, as shown in Fig. 3. As the gain of the general device gradually decreases with the supply voltage, the proposed shaping function presents higher supply voltage to the PA at the low power region. It has an effect of increasing the gain at that region and compensating the AM/AM distortion. The block diagram of the polar transmitter with the envelope shaping block is shown in Fig. 4. A simple implementation for the integration with the adder and the variable gain block is needed.

The modified envelope signal makes the PA always operate above the $V_{\rm knee}$ so that the serious $V_{dd}(t)$ to $V_{\rm out}(t)$ and the

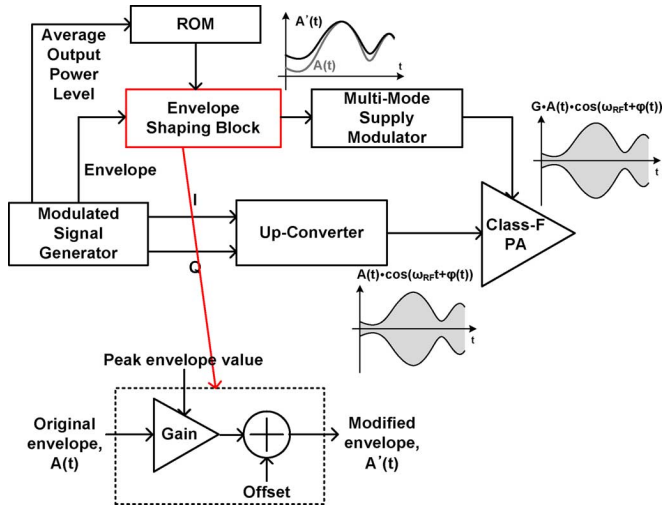


Fig. 4. Block diagram of the proposed polar transmitter with envelope shaping block.

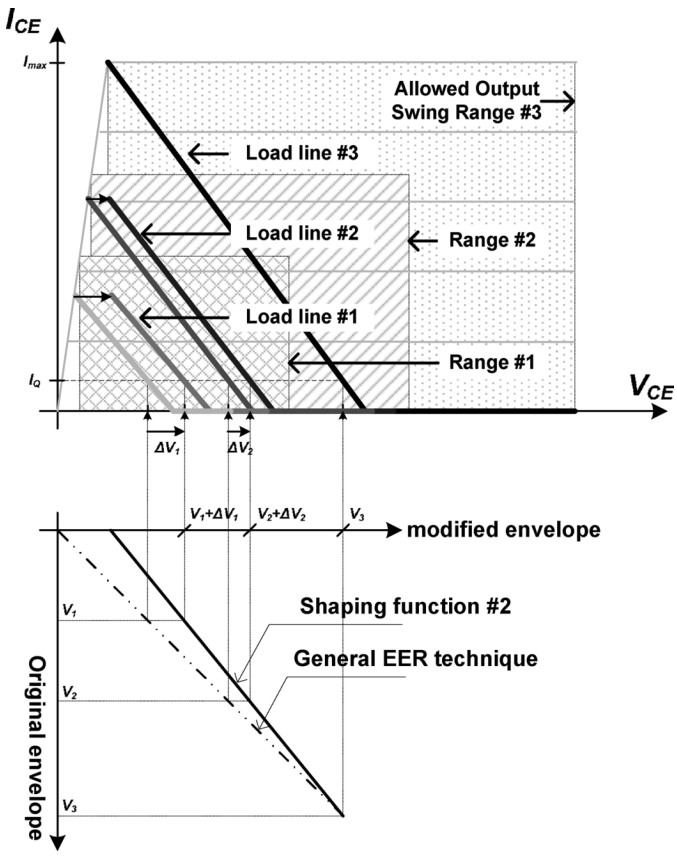


Fig. 5. Load line and the allowed maximum output swing range box in the presented polar transmitter operation.

$V_{dd}(t)$ to $\phi(t)$ are prevented. The load lines for the instantaneous output power levels are presented in Fig. 5. Through the envelope shaping, at the output level of V_1, the supply voltage is changed to $V_1 + \Delta V_1$. It results in an increase of the minimum voltage at the collector of the device from V_{knee1} to $V_{\text{knee1}} + \Delta V_1$. As the output level increases from V_1 to V_2, the offset voltage decreases from ΔV_1 to ΔV_2. It means less power loss at higher output power where the contribution to the overall efficiency and temperature of the PA chip is large.

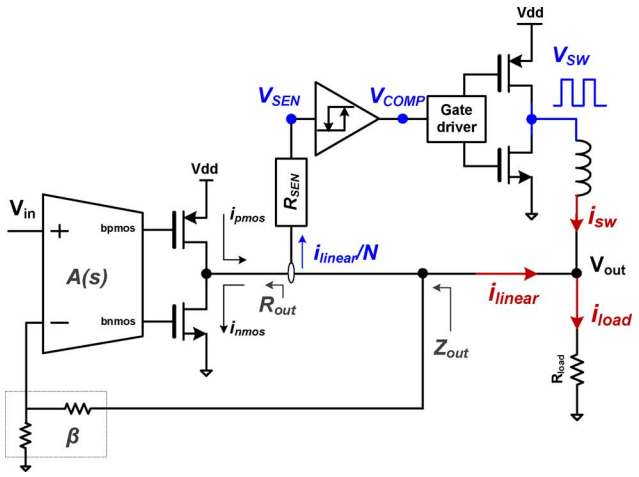


Fig. 6. Simplified block diagram of the HSA.

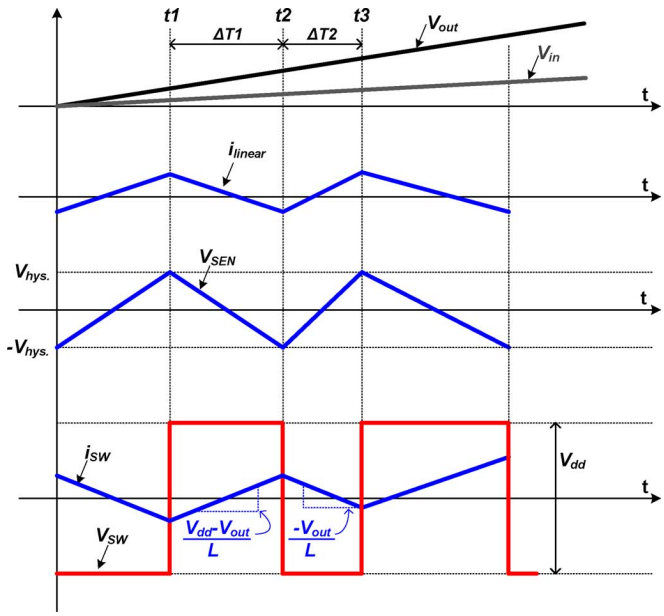


Fig. 7. Operating waveforms of the HSA.

At a very low power region, the supply modulation does not have any effect of improving the efficiency, compared to the fixed supply voltage operation. Therefore, the proposed envelope shaping is adopted until the efficiency of the supply modulated PA is the same as that of the fixed supply PA. The dynamic range of the proposed PA is equal to the conventional linear PA, while the efficiency is boosted up at the most energy consuming region.

IV. Multimode Supply Modulator

A. Operation Principles of HSA

As a supply modulator, the HSA shown in Fig. 6 simultaneously achieves a high fidelity and high efficiency. The linear amplifier operates as an independent voltage source to amplify the input signal through the feedback network, while the switching amplifier acts as a dependent current source to supply most of the current needed at the output. The current sensing unit detects the current flowing from the linear amplifier to the output and it changes the state of the switching amplifier according to

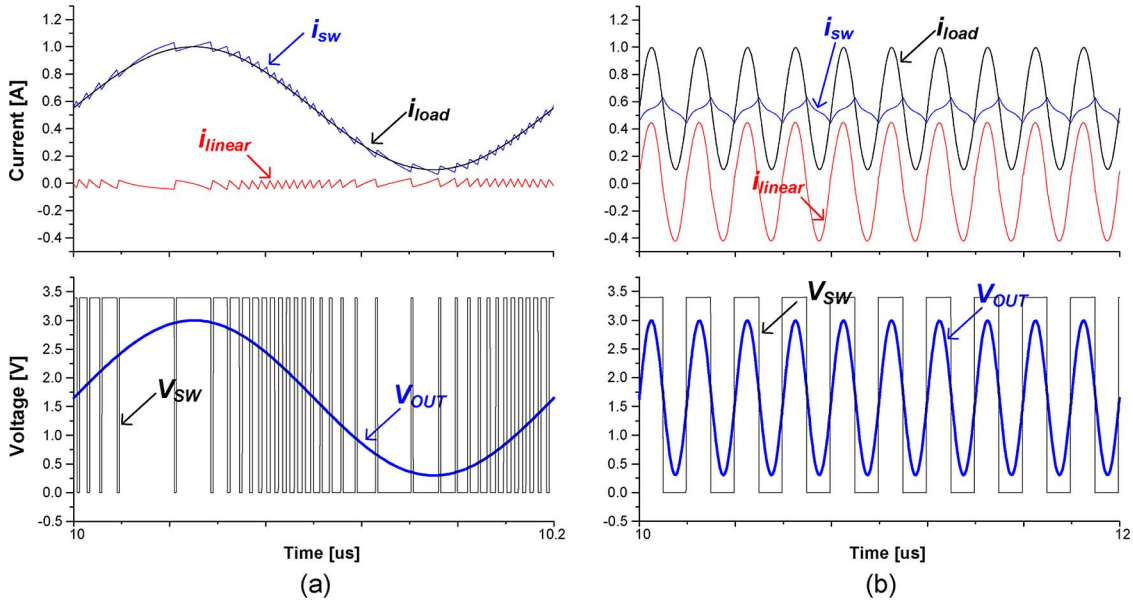


Fig. 8. Operating waveforms of the HSA as: (a) switch-mode assisted linear amplifier and (b) linear amplifier with constant current source. With the sinusoidal input signal of $1.65\ \mathrm{V} + 1.35\ \mathrm{V} \cdot \sin\{2\pi \cdot (5\ \mathrm{MHz})t\}$, the switching frequency f_{sw} is about 250 MHz for the HSA operating in (a). On the other hand, for the HSA operating in (b), f_{sw} is about 5 MHz with the same input signal.

the magnitude and polarity of the sensed current. The detailed operating waveforms in each node are illustrated in Fig. 7. As the input signal, V_{in} increases, current from the linear amplifier, i_{linear} increases, which is proportional to the sensing current. The sensed current is converted to the voltage V_{sen}, and it is directly applied to the input of the hysteretic comparator. At $t1$, V_{sen} then gets larger than the positive hysteresis voltage and the output of the comparator changes its state from 0 to 1, turning on the switch and increasing the current from the switching amplifier i_{sw} with the slope of $(V_{dd}-V_{\mathrm{out}})/L$ during $\Delta T1$. As i_{sw} increases, i_{linear} decreases and V_{sen} is also decreased. At $t2$, V_{sen} then becomes smaller than the negative hysteresis voltage, the output of the comparator is changed from 1 to 0, and the switch is turned off, resulting in the decrease of i_{sw} with the slope of $-V_{\mathrm{out}}/L$ during $\Delta T2$. Continuing this type of operation, the high efficiency switching amplifier finally provides most of the current required to the load, while the wideband linear amplifier compensates the switching ripple.

As the switching frequency is a reciprocal of the switching period $\Delta T1 + \Delta T2$, the switching frequency is

$$f_{\mathrm{sw}} = \frac{R_{\mathrm{sen}} V_{\mathrm{out}}(V_{dd} - V_{\mathrm{out}})}{2V_{dd} N L V_{\mathrm{hys.}}} \tag{2}$$

where V_{dd}, $V_{\mathrm{hys.}}$, R_{sen}, and N are the supply voltage, the hysteresis voltage of the comparator, the current to voltage ratio, and the current sensing ratio in the sensing unit, respectively. The maximum switching frequency is observed when V_{out} is equal to $V_{dd}/2$. It can be expressed as

$$f_{\mathrm{sw,max}} = \frac{R_{\mathrm{sen}} V_{dd}}{8 N L V_{\mathrm{hys.}}}. \tag{3}$$

From (3), the peak ripple current from the switching amplifier $[V_{\mathrm{hys.}}/(R_{\mathrm{sen}}/N)]$ is inversely proportional to f_{sw}. Since the linear amplifier supplies the current with inverse phase to compensate the ripple from the switching amplifier, the power loss of the linear amplifier is inversely proportional to f_{sw} while the switching loss is proportional to f_{sw}. The minimum idle power loss is given by

$$\begin{aligned} P_{\mathrm{sw}} &= K_1 \cdot f_{\mathrm{sw}} \\ P_{\mathrm{lin}} &= K_2 \cdot \frac{1}{f_{\mathrm{sw}}} \\ P_{\mathrm{total}} &= P_{\mathrm{sw}} + P_{\mathrm{lin}} = K_1 \cdot f_{\mathrm{sw}} + K_2 \cdot \frac{1}{f_{\mathrm{sw}}} \geq 2\sqrt{K_1 K_2} \end{aligned} \tag{4}$$

where K_1 and K_2 are the proportional constants [19].

To provide most of the current through the switching amplifier, the inductor should be able to supply the current at any signal frequency to meet the required slew rate. This condition is expressed as follows:

$$\frac{di_{\mathrm{Load}}}{dt} = \frac{2\pi f_s V_o}{R_{\mathrm{Load}}} \cdot \cos(2\pi f_s t) \leq \frac{V_{dd} - V_o \sin(2\pi f_s t)}{L} \tag{5}$$

$$L \leq \frac{R_{\mathrm{Load}}(V_{dd} - V_o \sin(2\pi f_s t))}{2\pi f_s V_o \cos(2\pi f_s t)} \tag{6}$$

where $V_{\mathrm{out}} = V_o \sin(2\pi f_s t)$. The maximum value can be obtained by differentiating (6) and equalizing it to zero. The required maximum inductance is then given by

$$L \leq \frac{R_{\mathrm{Load}} \cdot \sqrt{V_{dd}^2 - V_o^2}}{2\pi f_s V_o}. \tag{7}$$

Substituting (7) to (3), the required f_{sw} is

$$f_{\mathrm{sw,max}} \geq \frac{\pi f_s V_{dd} R_{\mathrm{sen}} V_o}{4 V_{\mathrm{hys.}} N R_{\mathrm{Load}} \sqrt{V_{dd}^2 - V_o^2}}. \tag{8}$$

The HSA satisfying the above relationship has been named as the switch-mode assisted linear amplifier because the switching amplifier supplies most of the load current with high fidelity [20]–[23].

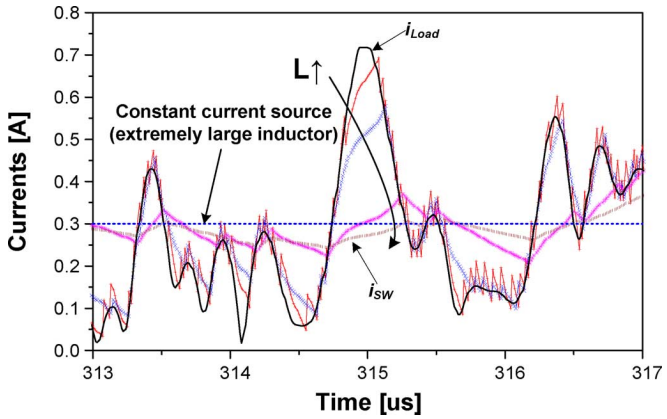


Fig. 9. Simulated $i_{\rm sw}$ waveforms with varying inductance. For the given bandwidth, the optimum switching frequency can be determined by sweeping the inductance value. For the 5-MHz 8.6-dB m-WiMax signal, the optimum inductance of 2.2 μH is found, and the switching frequency is about 3.75 MHz.

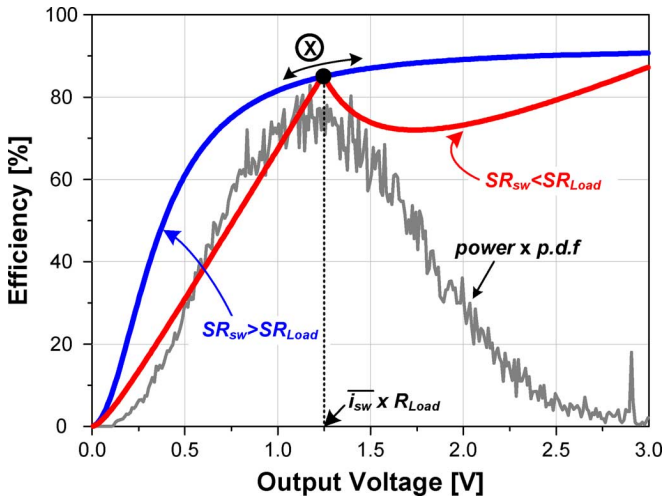


Fig. 10. Simulated efficiency of the HSA. Depending on the relative magnitude ratio between $SR_{\rm sw}$ and $SR_{\rm Load}$, the efficiency curves are drawn. The optimum amount of $i_{\rm SW}$ is determined by considering the signal power generation distribution (power $\times$ p.d.f.).

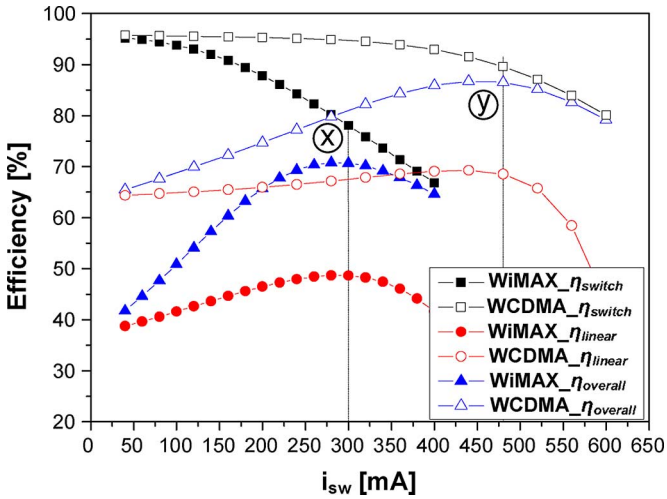


Fig. 11. Optimum amount of $i_{\rm SW}$ for maximum overall efficiency $\eta_{\rm overall}$ of the HSA operating with WCDMA and m-WiMax signals, where $\eta_{\rm linear}$ and $\eta_{\rm switch}$ are the efficiencies of the linear amplifier and the switching amplifier, respectively.

The output ripple voltage should be as low as possible to get a linear output waveform. The ripple voltage at the output node can be expressed as

$$V_{\rm out\_ripple}(s) = i_{\rm sw\_ripple}(s) \cdot (Z_{\rm out}(s)//R_{\rm Load}). \quad (9)$$

To satisfy the 802.16e m-WiMax standard requesting -50-dBc spurious response at the $2 \cdot f_s$ offset frequency, assuming that the current from the switching amplifier contains 10% ripple current on it, the output impedance of the linear amplifier needs to be 30 dB lower than $R_{\rm Load}$ at all relevant frequencies. If the $R_{\rm Load}$ of 4.2 Ω is assumed, the required output impedance of the linear amplifier is

$$Z_{\rm out} < \frac{R_{\rm Load}}{30\ {\rm dB}} \simeq 0.13\ \Omega. \quad (10)$$

The low-output impedance can be accomplished by a wide-bandwidth high-gain amplifier with a proper feedback network. In Fig. 6, the output impedance can be expressed as

$$Z_{\rm out}(s) = \frac{R_{\rm out}}{1 + \beta A(s)} \quad (11)$$

where $R_{\rm out}$ is the output impedance of the class-AB buffer and $A(s)$ is the frequency response of the operational transconductance amplifier (OTA). Since $R_{\rm out}$ and β are nearly constants, $Z_{\rm out}$ has a reverse frequency response to $A(s)$. Considering the general low-pass characteristic of the OTA, $Z_{\rm out}$ gets higher as the frequency increases.

B. Wideband Operation of HSA

For a wideband operation of the switch-mode assisted linear amplifier, the switching frequency $f_{\rm sw}$ should be very high, resulting in efficiency degradation of the switching amplifier by the switching loss. For example, as shown in Fig. 8(a), when the 5-MHz input signal is applied to this amplifier, the switching frequency is 250 MHz, about 50 times higher than the input signal frequency. This is too high to efficiently provide the switching current. Moreover, to compensate the switching ripple current, the bandwidth of the linear amplifier has to cover the switching frequency so that it consumes a large amount of dc power, a further degradation of the overall efficiency.

Let us then assume a different mode of operation in which the switching amplifier does not cover the slew rate required to the load current. In this case, the inductance determined by (7) is increased for lower slew rate of the switching amplifier. As the switching amplifier is not able to supply most of the signal current to the load any more, the linear amplifier helps providing the insufficient signal current to the load, as well as compensating the ripple current. As shown in Fig. 8(b), the switching current $i_{\rm SW}$ is nearly constant and the switching frequency is proportional to the input signal. That is, for the same input signal, the switching frequency of the HSA is now significantly reduced and the bandwidth requirement for the linear amplifier is also reduced. Therefore, in the circuit design, by increasing the inductance from (7), the optimum switching frequency minimizing the power loss described in (4) can be found for the given wideband input signal. For the 5-MHz 8.6-dB PAPR m-WiMax signal, the optimum inductance is set to 2.2 μH, which gives the switching frequency of 3.75 MHz. The current waveforms of the switching amplifiers with various inductances are shown in Fig. 9. At the extreme

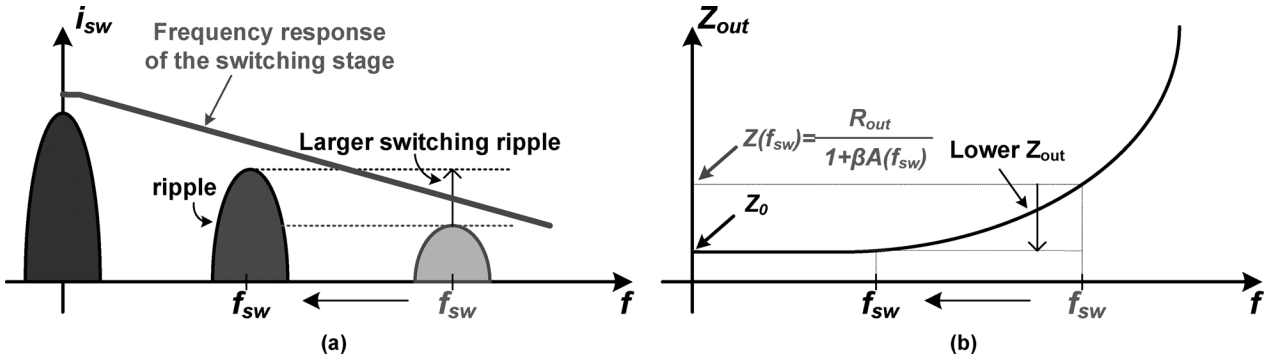


Fig. 12. (a) Spectra of $i_{\rm sw}$ from the switching stage. (b) Output impedance of the class-AB buffered linear amplifier.

case of very large inductance, a constant current source can replace the switching amplifier. Such an HSA can be expressed as a linear amplifier with a parallel current source.

Note that when the HSA is optimized for wideband applications, the operation for a narrowband signal is automatically changed to the switch-mode assisted linear amplifier. This is because the slew rate of the switching amplifier is fixed at the design stage of the wideband HSA, while the slew rate of the load current is reduced. In this work, the maximum operating condition of (8) is set to the EDGE signal. For wider bandwidth applications, the designed HSA operates close to the linear amplifier with a parallel current source.

The efficiency of the HSA depends on the relative slew rate of the switching amplifier compared to the slew rate of the load current. By sweeping the dc output voltage, the efficiency curves in Fig. 10 are obtained. For the low slew rate load such as dc, the HSA operates as the switch-mode assisted linear amplifier and the efficiency is close to that of the switching amplifier. There is a little efficiency degradation coming from the ripple compensation of the linear amplifier. However, for the high slew-rate load such as m-WiMax, the HSA operates as the linear amplifier with a parallel current source. For the simple simulation and its explanation, in here, the switching amplifier in HSA is replaced with the ideal constant current source, and the efficiency curve for $SR_{\rm sw} < SR_{\rm Load}$ in Fig. 10 is drawn with this simplified circuit. This efficiency curve can be explained easily by dividing the output voltage region into three. When the current from the constant current source, $i_{\rm SW}$ is larger than the required load current ($i_{\rm Load}$), all of the load current is provided from the high-efficiency switching amplifier, and the excess current sinks to the NMOS in the class-AB buffer as $i_{\rm nmos}$. This region corresponds to the output voltage region, which is lower than the point X in Fig. 10. When $i_{\rm SW}$ is equal to $i_{\rm Load}$, all of the current flowing to the load is still provided by the current source, and there is no excess current. As the required $i_{\rm Load}$ gets larger than $i_{\rm SW}$, the linear amplifier starts to supply the current to the load as $i_{\rm pmos}$. The low efficiency of the linear amplifier slightly degrades the overall efficiency near the point X. As it supplies more current to the load, the overall efficiency is increased again.

C. Multimode Operation of HSA

For the linear amplifier with the parallel current source, the peaking point X moves along the efficiency curve of the switch-mode assisted linear amplifier according to the amount of the current from the switching amplifier $i_{\rm SW}$. For the amplification of the modulated signal, the power generation at each output voltage is determined by the multiplication of the probability distribution function (p.d.f.) and signal power, and the point X should be located at the peak power generation point [5], [6]. For the m-WiMax signal with 8.6-dB PAPR, the optimum point of X is set to 1.26 V, which means an $i_{\rm SW}$ of 300 mA for the load impedance of 4.2 Ω. In Fig. 11, $i_{\rm SW}$ is swept from 40 to 400 mA to verify the above discussion. The highest efficiency is achieved when $i_{\rm SW}$ is 300 mA, and it is exactly matched to the point X in Fig. 10. The efficiencies for the linear stage, switching stage, and overall stage are calculated as follows:

$$\eta_{\rm linear} = \frac{V_{\rm out} \cdot i_{\rm pmos}}{P_{\rm DC\_linear}} \tag{12}$$

$$\eta_{\rm switch} = \frac{V_{\rm out} \cdot (i_{\rm sw} - i_{\rm nmos})}{P_{\rm DC\_switch}} \tag{13}$$

$$\eta_{\rm overall} = \frac{V_{\rm out} \cdot i_{\rm load}}{P_{\rm DC\_overall}}. \tag{14}$$

For the WCDMA signal with 3.5-dB PAPR, on the other hand, the optimum point of Y is set to 2.016 V, which means a $i_{\rm SW}$ of 480 mA for the same load impedance of 4.2 Ω. To support two signals having different PAPR, therefore, the amount of $i_{\rm SW}$ should be changed.

In the HSA, the adaptation of $i_{\rm SW}$ is automatically performed by the sensing and comparison operations. With the large L for the wideband operation, $i_{\rm SW}$ can be expressed as

$$\begin{aligned}\overline{i_{\rm SW}} &= \gamma \cdot (\overline{i_{\rm sen}} \cdot R_{\rm sen} - V_{\rm ref}) \\ &= \gamma \cdot \left(\frac{\overline{i_{\rm Load} - i_{\rm SW}}}{N} \cdot R_{\rm sen} - V_{\rm ref} \right)\end{aligned} \tag{15}$$

where γ is the transconductance gain of the switching stage and $V_{\rm ref}$ is the reference voltage of the comparator. Arranging the above equation (15) for $i_{\rm SW}$, the following equation is obtained:

$$\overline{i_{\rm SW}} = \frac{\gamma}{1 + \gamma \cdot \dfrac{R_{\rm sen}}{N}} \cdot \left(\overline{i_{\rm Load}} \cdot \frac{R_{\rm sen}}{N} - V_{\rm ref} \right). \tag{16}$$

As $i_{\rm Load}$ has a linear relationship with the input envelope signal, the amount of ${i_{\rm SW}}^2$ is inversely proportional to the PAPR.

For a wideband signal, whose slew rate is higher than the slew rate of the switching amplifier, the switching frequency is proportional to the input signal frequency, as mentioned in Section IV-B. The hysteresis value is not related to the switching frequency so it is set to 0 mV to minimize the power loss by the hysteretic operation. For a relatively narrowband signal, whose slew rate is lower than the slew rate of the switching amplifier,

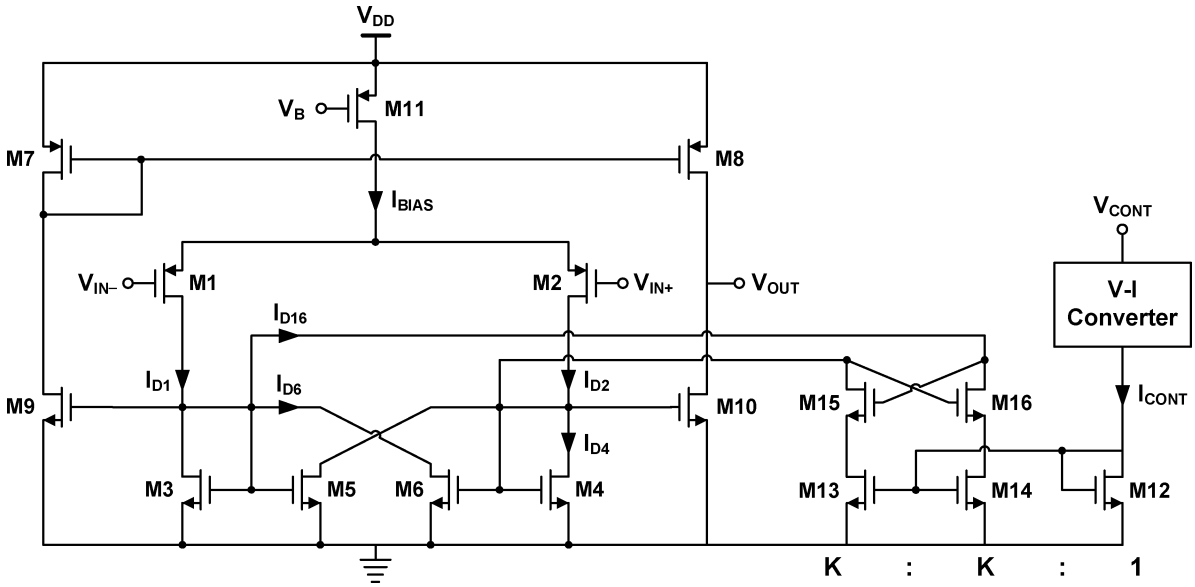


Fig. 13. Schematic of the programmable hysteretic comparator.

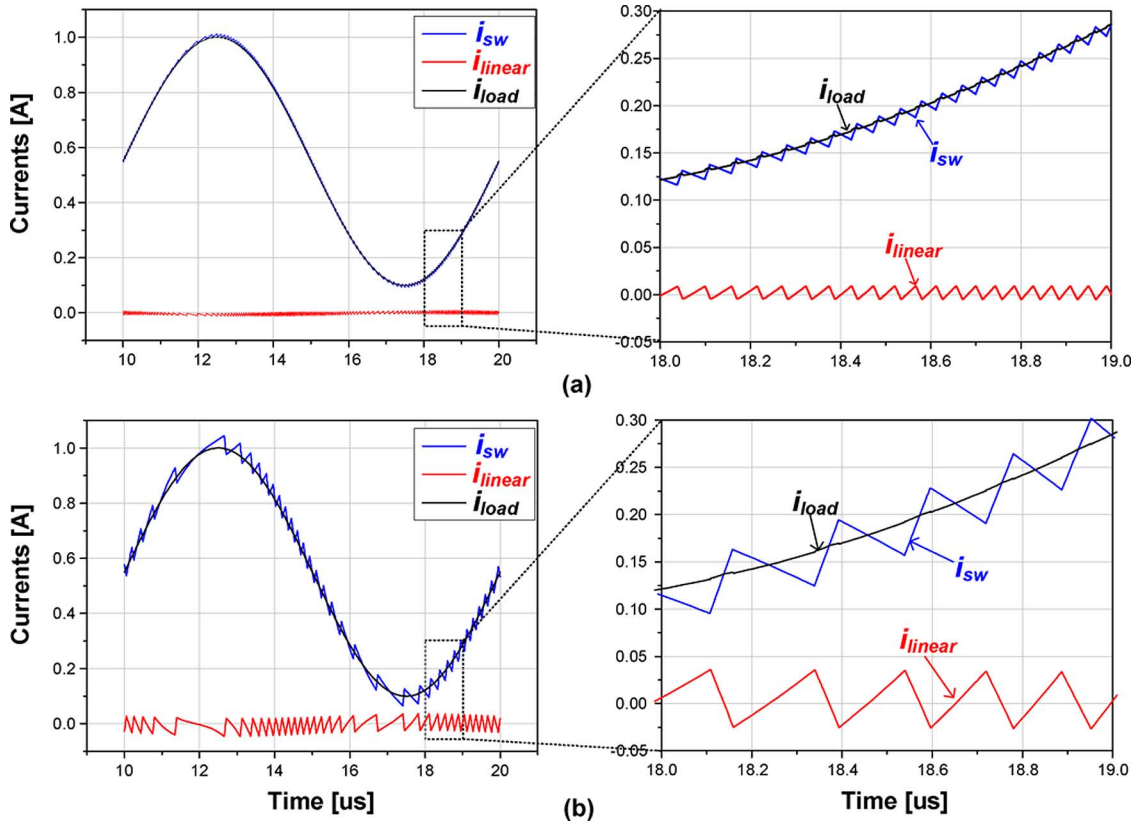
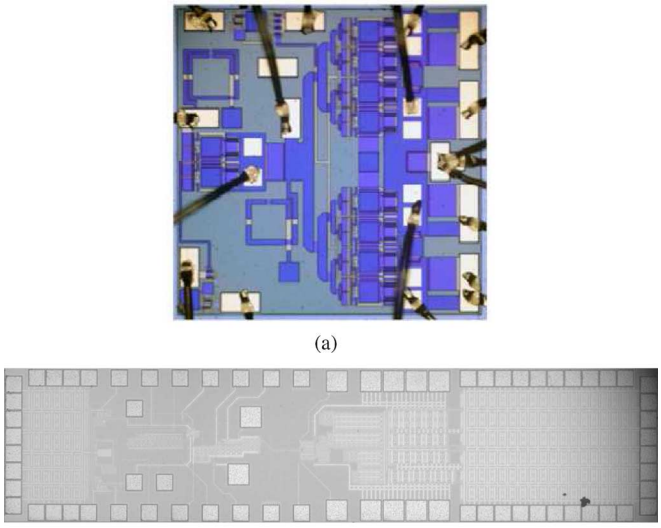


Fig. 14. Control of the switching frequency: simulated current waveforms of the linear/switching stage and the output load: (a) with $V_{\mathrm{CONT}} = 0$ V and (b) with $V_{\mathrm{CONT}} = 1$ V.

the HSA operates as a switch-mode assisted linear amplifier. i_{SW} is not a quasi-static current anymore, but it actively follows i_{Load}. The switching frequency is now the function of the circuit parameters. As the high-efficiency switching stage provides most of the load current, the overall efficiency is close to the efficiency of the switching stage. However, with the switching condition optimized for the wideband signal, the switching frequency is excessively large, which is directly connected to the switching loss. To reduce the switching frequency according to the input signal bandwidth, $V_{\mathrm{hys.}}$ in (3) should be increased to meet the condition for the minimum power loss in (4). The hysteresis value is proportional to the magnitude of the ripple current. In addition, in a general switching converter, the lower switching frequency induces a lower filtering effect by the LC filter because the cutoff frequency is fixed, as shown in Fig. 12(a). As a result, the ripple voltage at the output degrades the linearity of the overall amplifier. However, the HSA replaces the capacitor with the class-AB buffered



(a)

(b)

Fig. 15. Chip photographs. (a) Class-AB/F PA. (b) Supply modulator. The sizes of (a) and (b) are 1.2×1.2 mm^2 and 3×0.65 mm^2, respectively.

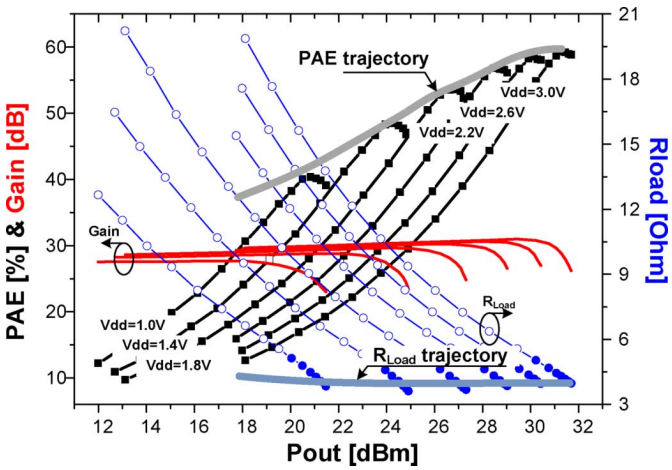


Fig. 16. Measured output power, gain, and impedance seen by the supply modulator versus the output power. The class-AB/F PA is biased in the class-AB mode.

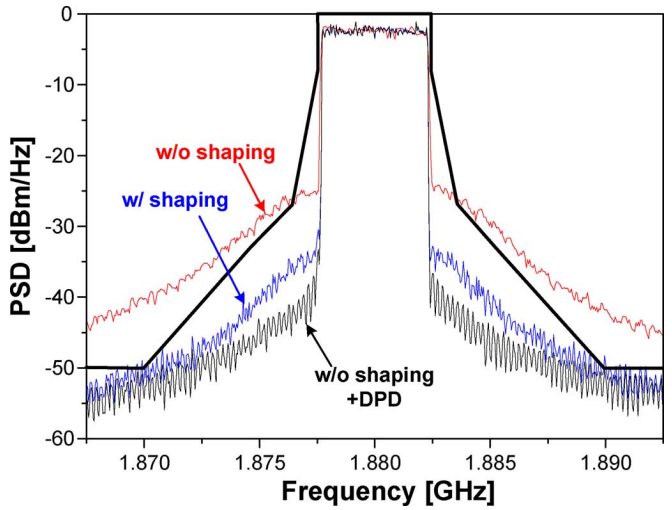


Fig. 17. Measured spectra for the IEEE 802.16e m-WiMax signal.

linear amplifier, whose output impedance is very low at the low-frequency region, as depicted in Fig. 12(b). In the HSA,

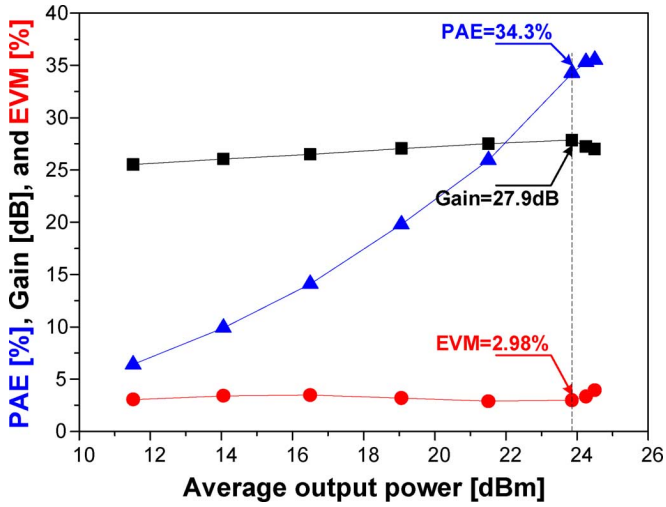


Fig. 18. Measured PAE, gain, and EVM for 802.16e m-WiMax system. No DPD technique is adopted.

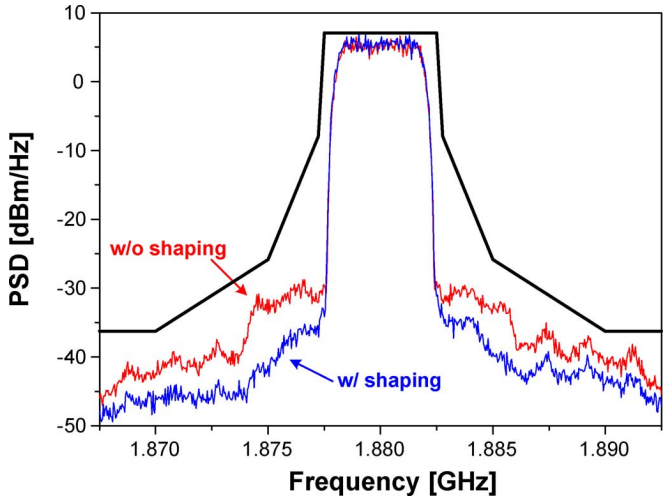


Fig. 19. Measured spectra for the WCDMA signal.

the hysteresis value can be increased without generating a large distortion due to the low Z_{out} at the switching frequency.

D. Programmable Hysteretic Comparator

The programmable hysteretic comparator is designed to vary the hysteresis value according to the input signal's bandwidth. The transistor-level circuits are illustrated in Fig. 13. It consists of the conventional hysteretic comparator and a positive feedback control circuit. The additional feedback control circuit regulates the currents through M15 and M16. It has an effect of scaling the size of M5 and M6, which determine the amount of positive feedback. Assuming the device sizes of M3, M4, M5, and M6 are equal, the effective positive feedback factor α' is given by

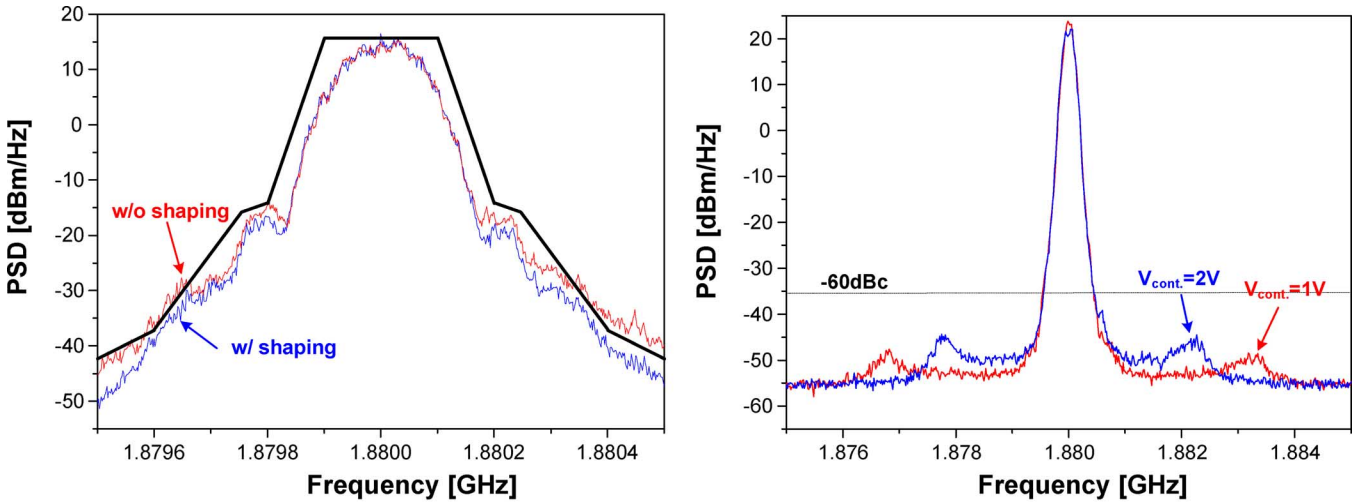
$$\alpha' = \frac{I_{\text{BIAS}} + KI_{\text{CONT}}}{I_{\text{BIAS}} - KI_{\text{CONT}}} \tag{17}$$

where

$$K = \frac{\left(\frac{W}{L}\right)_{13,14}}{\left(\frac{W}{L}\right)_{12}}. \tag{18}$$

TABLE I
PERFORMANCE OF THE POLAR TRANSMITTER WITH PROPOSED ENVELOPE SHAPING TECHNIQUE

	Pout [dBm]	Gain [dB]	PAE [%]	RCE [dB]	EVM [%]
w/o shaping, no DPD	22.9	25.9	34.9	–21.6	8.25
w/o shaping + DPD	23.7	26.7	37	–38.5	1.19
w/ shaping, no DPD	**23.9**	**27.9**	**34.3**	**–30.5**	**2.98**
	(24.5)	(27)	(35.5)	(–27.4)	(3.93)



(a) (b)

Fig. 20. Measured spectra for the EDGE signal. (a) 1-MHz span with $V_{\mathrm{cont.}} = 2$ V. (b) 10-MHz span with hysteresis control for optimum operation.

The hysteresis voltage is expressed as

$$V_{\mathrm{hys.}} \simeq \sqrt{\frac{I_{\mathrm{BIAS}}}{\mu_p C_{\mathrm{ox}} \left(\frac{W}{L}\right)_{1,2}}} \cdot \frac{KI_{\mathrm{CONT}}}{I_{\mathrm{BIAS}}}. \tag{19}$$

With the linear V–I converter, the $V_{\mathrm{hys.}}$ is linearly proportional to V_{CONT} with ± 10 mV/V.

For the sinusoidal wave of $1.65\ \mathrm{V} + 1.35\ \mathrm{V} \cdot \sin\{2\pi \cdot (100\ \mathrm{kHz})t\}$ with $V_{\mathrm{CONT}} = 0$ V, the maximum switching frequency is about 20 MHz, as shown in Fig. 14(a). With $V_{\mathrm{CONT}} = 1$ V, the maximum switching frequency is reduced to 5 MHz, while the magnitude of the ripple is increased, as described in Fig. 14(b). Seen from the load current, the increased magnitude of the ripple current at the output is negligible thanks to the low output impedance of the class-AB buffered linear amplifier at the reduced switching frequency.

V. EXPERIMENTAL RESULTS

The proposed polar transmitter is fabricated with an InGaP/GaAs 2-μm HBT process for the class-AB/F PA and a CMOS 0.13-μm process for the supply modulator with 3.3-V compatible devices. The PA is integrated on a chip, except two capacitors of the output matching network. For the supply modulator, all circuit components are integrated on a chip, except the large inductor. As shown in Fig. 15, the overall die size is less than 3.5 mm^2 for the two chips.

The fabricated class-AB/F PA delivers 31.2-dBm output power with 30-dB gain at 3-V dc supply voltage. Fig. 16 presents the measured PAE and gain of the PA with the impedance seen by the supply modulator. It is calculated from the dc supply voltage and current of the power stage. Varying the supply voltage from 1 to 3 V, the PAE changes from 40% to 60%, while the modulator's load impedance is nearly 4 Ω (filled circles of R_{Load} in Fig. 16). The designed supply modulator works with a 3.3-V single supply and is able to drive the RF PA with a maximum efficiency of 89%. The worst case gain bandwidth product (GBW) is about 120 MHz over the peak-to-peak output swing range from 0.3 to 3 V for the 4.2-Ω load.

TABLE II
HYSTERETIC WINDOW CONTROL FOR EDGE

	P_{DC_Linear}	$P_{DC\_Switching}$	PAE [%]
$V_{cont.}$=0V	162.4mW	1229.2mW	38.6
$V_{cont.}$=1V	180.8mW	1041.5mW	43.6
$V_{cont.}$=2V	189.2mW	995.6mW	45.3

TABLE III
PERFORMANCE SUMMARY OF THE MULTIMODE SUPPLY MODULATOR

Parameters	Values
Supply Voltage	3.3V
Output voltage range	0.3-3V
Output RMS current	0-750mA
Peak efficiency	89%
Worst-case GBW	120MHz
f_{sw} for EDGE	2.12MHz
for WCDMA	2.88MHz
for m-WiMax	3.75MHz
$V_{hys.}$ for EDGE	20mV
for WCDMA	0mV
for m-WiMax	0mV

TABLE IV
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART RESULTS

	Application	PAPR	Bandwidth	$\eta_{S.M.}$	Pout	Gain	Overall PAE	DPD
[4]	EDGE	3.5dB	384kHz	-	23.8dBm	-	22%	Yes
[9]	EDGE	3.5dB	384kHz	†89%	-	-	-	Yes
[11]	CDMA	5dB	1.25MHz	†82%	28dBm	-	32%	-
[12]	WCDMA	3.4dB	3.84MHz	83%	27dBm	25dB	46%	No
[10]	WLAN	>8dB	20MHz	65%	20dBm	11dB	28%	Yes
This work	EDGE	3.5dB	384kHz	84%	27.8dBm	29.4dB	45.3%	No
This work	WCDMA	3.4dB	3.84MHz	84%	29dBm	27.8dB	46%	No
This work	m-WiMax	8.6dB	5MHz	75%	23.9dBm	27.9dB	34.3%	No

†Efficiency at Vout=3V_{DC}

Without the envelope shaping, the overall efficiency for m-WiMax is about 34.9% with 22.9-dBm output power. However, as expected in Section III, the serious $V_{dd}(t)$ to $\phi(t)$ deteriorates the linearity so that digital feedback pre-distortion (DFBPD) technique is applied [24]. It not only linearizes the PA, but also increases the efficiency with more output power. The linearized polar transmitter without the envelope shaping shows the PAE of 37% with the output power of 23.7 dBm. The error vector magnitude (EVM) is lowered from 8.25% to 1.19%. For the handset applications, however, the power overhead for the signal processing is very critical. Including this power consumption, the overall PAE will be degraded. The proposed envelope shaping method reduces the nonlinearity at a low V_{dd} region so that the transmitter operates very linearly compared with the transmitter without the shaping. Fig. 17 shows the spectra for the polar transmitter with and without the envelope shaping method. With the proposed envelope shaping, the nonlinear characteristics are considerably improved. There is about 10-dB adjacent channel leakage power ratio (ACLR) improvement over the channel bandwidth of 25 MHz with this shaping technique. The transmitter with the envelope shaping method has a negligible degradation of the PAE by the gain enhancement at the low supply voltage and the higher efficiency of the supply modulator, where the latter results from the reduced PAPR of the shaped envelope. The PAE of 34.3% at $P\mathrm{out}$ of 23.9 dBm is achieved with the EVM of 2.98% without any DPD technique. From 11.5 to 24.5 dBm (*or higher*), the PA operates in the envelope tracking mode. At the lower power region, the supply voltage is fixed to 1 V. This is the point where the efficiency of the supply modulated PA is the same as that of the fixed 1-V supply PA. Fig. 18 shows the performance of the transmitter versus the average output power for IEEE 802.16e m-WiMax system. Fig. 19 shows the measured spectra for the WCDMA signal with/without the envelope shaping. The performance of the polar transmitter showing the effectiveness of the proposed envelope shaping technique is given in Table I.

The behavioral model for the supply modulated PA is changed for every power level control operation in the mobile application. It means the PA should be re-modeled for each average power. This results in multiple lookup tables (LUTs), directly connected to more power consumption. This fact makes the proposed DPD-less polar transmitter more attractive for the handset applications.

For the WCDMA signal, this transmitter delivers a PAE of 46% at an average output power of 29 dBm with a gain of 27.8 dB. Since the PAPR is lower than that of m-WiMax, the amount of current from the switching stage is automatically increased on the operation of the HSA. The hysteresis value is not changed due to the similar bandwidth of them. It satisfies the spectrum emission mask at that power level.

For the EDGE signal, the designed polar transmitter optimized for m-WiMax presents a PAE of 38.6% at a $P\mathrm{out}$ of 27.8 dBm and a gain of 29.4 dB. Similar to the m-WiMax case, the transmitter with the shaped envelope satisfies the spectrum emission mask. Since there are significant differences in bandwidth between EDGE and m-WiMax, the optimum hysteresis value should be increased. As $V_{\mathrm{cont.}}$ gets higher, the amount of ripple current is increased, but the switching frequency is decreased. Fig. 20(a) shows the spectra with a 1-MHz span. Fig. 20(b) shows the spectra with the hysteretic window control. At $V_{\mathrm{cont.}} = 0$ V, the ripple power is so small that it is hard to observe it in the spectra. At $V_{\mathrm{cont.}} = 2$ V, the hysteresis value is about 20 mV and the following switching frequency of 2 MHz is observed. Table II presents the performance variation of the transmitter according to the hysteretic window control for the EDGE signal. Table III summarizes the performance of the multimode supply modulator. The overall performance of the polar transmitter with the recent state-of-the art results are summarized in Table IV.

VI. CONCLUSIONS

We have designed a highly efficient and linear polar transmitter for multistandard applications. The supply modulator and PA are optimized for a high efficiency with the proper topology selection. The novel envelope shaping function enables the highly linear operation of the high-efficiency supply modulated PA by avoiding the operation at the dangerous region of 0 V to V_{knee}. The HBT class-AB/F PA with an on-chip harmonic control circuit shows an excellent efficiency characteristic with good linearity. The CMOS supply modulator integrates all the circuit elements on a chip, except the large inductor, and supports the multistandard application with the programmable hysteretic comparator. The overall polar transmitter shows a PAE of 45.3%/46%/34.3%, a gain of 29.4 dB/27.8 dB/27.9 dB at a $P\mathrm{out}$ of 27.8 dBm/29 dBm/23.9 dBm for EDGE/WCDMA/m-WiMax, respectively. Without any DPD techniques, it satisfies the overall spectrum emission mask specifications, and the relative constellation error (RCE) and EVM for m-WiMax system are −30.5 dB and 2.98%, respectively.

REFERENCES

[1] L. Kahn, "Single-sideband transmission by envelope elimination and restoration," *Proc. IRE*, vol. 40, no. 7, pp. 803–806, Jul. 1952.

[2] D. K. Su and W. J. McFarland, "An IC for linearizing RF power amplifiers using envelope elimination and restoration," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2252–2258, Dec. 1998.

[3] J. Staudinger, B. Gilsdorf, D. Newman, G. Norris, G. Sadowniczak, R. Sherman, and T. Quach, "High efficiency CDMA power amplifier using dynamic envelope tracking technique," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2000, pp. 873–976.

[4] P. Raynaert and S. Steyaert, "A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2598–2608, Dec. 2005.

[5] S. Hong, Y. Y. Woo, I. Kim, J. Kim, J. Moon, H. S. Kim, J. S. Lee, and B. Kim, "High efficiency GaN HEMT power amplifier optimized for OFDM EER transmitter," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2007, pp. 1247–1250.

[6] I. Kim, Y. Y. Woo, S. Hong, and B. Kim, "High efficiency hybrid EER transmitter for WCDMA application using optimized power amplifier," in *Proc. 37th Eur. Microw. Conf.*, Munich, Germany, Oct. 2007, pp. 182–185.

[7] J. Choi, J. Yim, Y. Yang, J. Kim, J. Cha, D. Kang, D. Kim, and B. Kim, "A $\Delta\Sigma$-digitzed polar RF transmitter," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 12, pp. 2679–2690, Dec. 2007.

[8] J. Kitchen, W. Chu, I. Deligoz, S. Kiaei, and B. Bakkaloglu, "Combined linear and Δ-modulated switched-mode PA supply modulator for polar transmitters," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2007, pp. 82–83.

[9] T. Kwak, M. Lee, B. Choi, H. Le, and G. Cho, "A 2 W CMOS hybrid switching amplitude modulator for EDGE polar transmitter," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2007, pp. 518–519.

[10] F. Wang, D. F. Kimball, D. Y. Lie, P. M. Asbeck, and L. E. Larson, "A monolithic high-efficiency 2.4-GHz 20-dBm SiGe BiCMOS envelope-tracking OFDM power amplifier," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1271–1281, Jun. 2007.

[11] W. Chu, B. Bakkaloglu, and S. Kiaei, "A 10 MHz-bandwidth 2 mV-ripple PA-supply regulator for CDMA transmitters," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2008, pp. 448–449.

[12] V. Pinon, F. Hasbani, A. Giry, D. Pache, and C. Garnier, "A single-chip WCDMA envelope reconstruction LDMOS PA with 130 MHz switched-mode power supply," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2008, pp. 564–565.

[13] P. Hazucha, G. Schrom, J. Hahn, B. A. Bloechel, P. Hack, G. E. Dermer, S. Narendra, D. Gardner, T. Karnik, V. De, and S. Borkar, "A 233-MHz 80%-87% efficient four-phase DC–DC converter utilizing air-core inductors on package," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 838–845, Apr. 2005.

[14] F. H. Raab, "Maximum efficiency and output of class-F power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 6, pp. 1162–1166, Jun. 2001.

[15] P. Colantonio, F. Giannini, G. Leuzzi, and E. Limiti, "On the class-F power amplifier design," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 9, no. 2, pp. 129–149, 1999.

[16] P. Colantonio, J. A. Garcia, F. Giannini, C. Gomez, N. B. Carvalho, E. Limiti, and J. C. Pedro, "High efficiency and high linearity power amplifier design," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 15, no. 5, pp. 453–468, 2005.

[17] D. Kang, D. Yu, K. Min, K. Han, J. Choi, D. Kim, B. Jin, M. Jun, and B. Kim, "A higly efficient and linear class-AB/F power amplifier for multimode operation," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 1, pp. 77–87, Jan. 2008.

[18] J. C. Pedro, J. A. Garcia, and P. M. Cabral, "Nonlinear distortion analysis of polar transmitters," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 12, pp. 2757–2765, Dec. 2007.

[19] N. I. Kim, S. H. Jung, J. Y. Ryoo, and G. H. Cho, "Ripple feedback filter suitable for analog/digital mixed-mode audio amplifier for improved efficiency and stability," in *Proc. IEEE Power Electron. Specialists Conf.*, Jun. 2002, pp. 45–49.

[20] G. B. Yundt, "Series or parallel-connected composite amplifiers," *IEEE Trans. Power Electron.*, vol. PE-1, no. 1, pp. 48–54, Jan. 1986.

[21] H. Ertl, J. W. Kolar, and F. C. Zach, "Basic considerations and topologies of switched-mode assisted linear power amplifiers," *IEEE Trans. Ind. Electron.*, vol. 44, no. 1, pp. 116–123, Feb. 1997.

[22] R. A. R. Zee and E. Tuijl, "A power-efficient audio amplifier combining switching and linear techniques," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 985–991, Jul. 1999.

[23] G. R. Walker, "A class B switch-mode assisted linear amplifier," *IEEE Trans. Power Electron.*, vol. 18, pp. 1278–1285, Nov. 2003.

[24] Y. Y. Woo, J. Kim, J. Yi, S. Hong, I. Kim, J. Moon, and B. Kim, "Adaptive digital feedback predistortion technique for linearizing power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 5, pp. 932–940, May 2007.

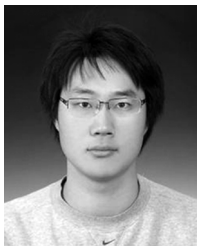
Jinsung Choi (S'07) received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2004 and is currently working toward the Ph.D. degree at POSTECH.

His main interests are analog/RF circuit design in ultra deep-submicrometer CMOS technology, mixed-mode signal-processing integrated-circuit design, and digitally assisted RF transceiver architectures.

Mr. Choi was the recipient of the 2009 Samsung Electronics Bronze Prize of the Human-Tech Thesis Prize.

Dongsu Kim received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2007, and is currently working toward the Ph.D. degree at POSTECH.

His research interests are CMOS RF circuits for wireless communications, with a special focus on highly efficient and linear RF transmitter design.



Daehyun Kang (S'08) received the B.S. degree in electronic and electrical engineering from Kyungpook National University, Daegu, Korea, in 2006, and is currently working toward Ph.D. degree at the Pohang University of Science and Technology (POSTECH), Pohang, Korea.

His research interests include the design of PAs and highly efficient and linear transmitters.

Bumman Kim (M'78–SM'97–F'07) received the Ph.D. degree in electrical engineering from Carnegie Mellon University, Pittsburgh, PA, in 1979.

From 1978 to 1981, he was engaged in fiber-optic network component research with GTE Laboratories Inc. In 1981, he joined Central Research Laboratories, Texas Instruments Incorporated, where he was involved in development of GaAs power field-effect transistors (FETs) and monolithic microwave integrated circuits (MMICs). He has developed a large-signal model of a power FET, dual-gate FETs for gain control, high-power distributed amplifiers, and various millimeter-wave MMICs. In 1989, he joined the Pohang University of Science and Technology (POSTECH), Pohang, Korea, where he is a Namko Professor with the Department of Electrical Engineering, and Director of the Microwave Application Research Center, involved in device and circuit technology for RF integrated circuits (RFICs). He was a Visiting Professor of electrical engineering with the California Institute of Technology, Pasadena, in 2001. He has authored over 250 technical papers.

Dr. Kim is a member of the Korean Academy of Science and Technology and the Academy of Engineering of Korea. He was an associate editor for the the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He is a Distinguished Lecturer of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S).