Optimized Envelope Tracking Operation of Doherty Power Amplifier for High Efficiency Over an Extended Dynamic Range

Jinsung Choi, *Student Member, IEEE*, Daehyun Kang, *Student Member, IEEE*, Dongsu Kim, and Bumman Kim, *Fellow, IEEE*

***Abstract*—This paper presents an optimized envelope tracking (ET) operation of a Doherty amplifier. Compared to the general ET/envelope elimination and restoration transmitter, it has an advantage of the extended dynamic range of 6 dB for the load modulation of a Doherty amplifier. Moreover, by modulating the supply voltage of the carrier amplifier, while that of the peaking amplifier is fixed, the supply modulator provides just half of the current for the same power amplifier output power. It results in a reduced chip size and the crest factor of the supply modulating signal is reduced by 6 dB, enhancing the efficiency of the supply modulator. The designed ET transmitter consisting of the Doherty amplifier and the supply modulator are fabricated in 2-μm HBT and 0.13-μm CMOS processes, respectively. It presents the efficiency improvement over the broad output power region. Especially at the 16-dB backed-off power level, more than 23% of power-added efficiency (PAE) is achieved. For WiBro application, it shows the PAE of 38.6% at an output power of 24.22 dBm with a gain of 24.62 dB. The error vector magnitude is 3.64%.**

***Index Terms*—CMOS analog integrated circuits, dc–dc power conversion, Doherty amplifier, envelope tracking (ET), power amplifiers (PAs), transmitters, wireless communication.**

I. Introduction

As THE modern wireless communication systems request high data rates within a limited bandwidth, the crest factor, which is the power ratio between the average signal power and its peak power, is considerably higher, exceeding 10 dB. The RF power amplifier (PA) operates in the power backoff region to linearly amplify the signal. In general, the efficiency at this region is so low that the usable battery time is limited and the handset unit becomes warm easily. In order to operate the PA with high efficiency, the crest factor reduction technique can be used. By reducing the crest factor, the PA can operate at a less power backoff region and it results in more output power and higher efficiency. However, it is not an ultimate solution for the high crest factor signal. As the crest factor gets higher with evolution of communication systems, the PA inevitably operates in the power-inefficient region. Moreover, if the PA itself has higher efficiency, the crest factor reduction technique helps getting even higher efficiency.

Much research has been done over time to improve PA efficiency at the power backoff region [1]–[17]. Among the various topologies reported in the literature, a Doherty amplifier and a polar modulator (also called the envelope elimination and restoration (EER) technique) are the most popular architectures capable of achieving high efficiency with moderate linearity. While both of them can be highly efficient for signals with the crest factor of around 5–7 dB, similar performance is hard to achieve for signals with a crest factor of more than 10 dB.

In this paper, a transmitter employing the envelope tracking (ET) operation of Doherty amplifier is optimized and implemented. It takes advantages of the ET and Dohetry amplifier without any deterioration of the performance. By modulating the supply voltage of the carrier amplifier for the Doherty amplifier, it boosts up the efficiency of the amplifier at the low-power region. It shows an extended dynamic range of 6 dB compared to the general ET transmitter. The crest factor of the supply modulating signal is also reduced by 6 dB, significantly enhancing the supply modulator efficiency. It is suitable to mobile handset applications requesting a high efficiency with wide power control range. In Section II, the concept of the ET transmitter employing the Doherty technique is presented. Section III deals with circuit implementation of the proposed transmitter. In Section IV, experimental results are presented. The designed ET Doherty amplifier delivers an efficiency of 23% at the 16-dB power backoff level. Considering that the handset is usually operated at the low-power level, this efficiency improvement at the low level is very significant.

II. ET Transmitter With Doherty Amplifier

A. Limitation of General ET/EER Transmitter

The EER transmitter shown in Fig. 1(a) ideally delivers very high efficiency at the entire power range with good linearity. By the Cartesian to polar conversion, the RF up-converted phase information is applied to the input of the PA and the amplitude information is delivered to the drain/collector of the PA through the supply modulator. It accomplishes the high efficiency by

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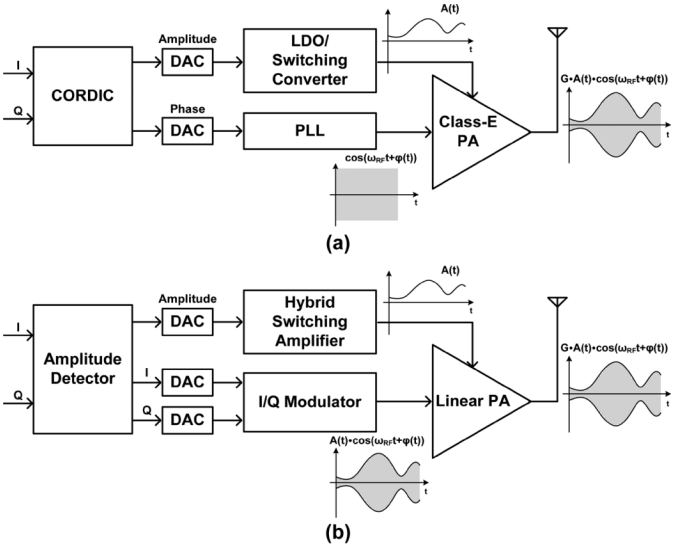

Fig. 1. Block diagrams of: (a) conventional EER transmitter and (b) wideband ET transmitter with the linear PA and the hybrid switching amplifier as a supply modulator.

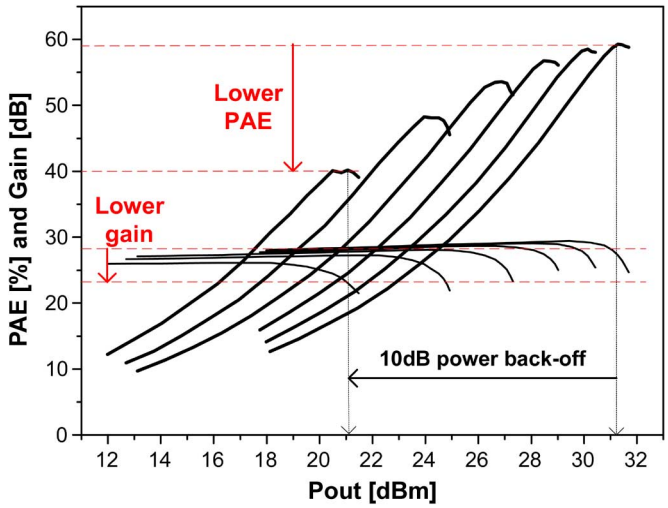

Fig. 2. Simulation results of the PA with various supply voltage. There are significant drops of PAE and gain at the power backoff operation region for the high crest factor.

modulating the supply voltage of the PA. Since only the combination of phase and amplitude restores the original constellation, it requires very accurate dynamic supply with the exact time alignment of phase and amplitude paths. In the transmitter, the input drive power has a constant envelope, which enables the usage of the nonlinear switching-mode amplifier such as class-E for high efficiency. In other words, the excessive input power is driven even for a low output power to saturate the PA. It induces a leakage of the input signal to the output and results in a nonlinear AM/AM characteristic. The broad bandwidth of the phase signal by the nonlinear conversion from the Cartesian to polar signal is also a burden for design of the PA. Not just for the PA, it requires a very high-speed Cartesian to polar converting processor for phase calculation. The recent report on the design of a 430-MHz processor consumes 280 mW for the conversion [18], which is so high that the overall efficiency of the transmitter chain becomes very low. Therefore, the input of the PA should be the Cartesian modulated signal, which has a time-varying envelope information. Moreover, as the switching-mode PA-based EER transmitter generates a large amount of third-order intermodulation (IM3) components, it requires the additional linearization. Therefore, a linear PA biased at class A or AB should be used to avoid the power burden for the linearization [9].

The efficiency of the EER transmitter cannot be good without a high-efficiency supply modulator because the efficiency can be calculated as follows:

$$\eta_{\text{overall}} = \eta_{\text{pa}} \times \eta_{\text{sm}} \tag{1}$$

where η_{pa} and η_{sm} are the efficiencies of the PA and supply modulator, respectively. To provide the envelope information to the PA with a high efficiency, a switching-mode power supply such as a buck converter is generally employed. It presents a very high efficiency of more than 90% for the heavy load, but the bandwidth of the switching mode power supply is limited, mainly by the switching loss. Higher switching speed induces larger switching loss. That is why most of the EER transmitters are still employing wideband linear regulators such as the low drop-out (LDO) regulator.

Recently, the hybrid switching amplifier combining advantages of the high-efficiency switching regulator and wideband linear regulator has been reported for the supply modulator [7]–[10]. It consists of a wideband class-AB buffered linear amplifier and a high-efficiency switching amplifier. The linear amplifier operates as an independent voltage source, while the switching amplifier acts as a dependent current source. The switching amplifier provides most of the current required to the load and the linear amplifier compensates the ripple current. For a wideband envelope signal, it achieves high efficiency and linearity simultaneously. The advanced ET transmitter employing the hybrid switching amplifier, the Cartesian modulator, and the linear PA is illustrated in Fig. 1(b). Note that the high-speed CORDIC processor for the Cartesian to polar conversion is now replaced by the simple amplitude detector.

However, as the crest factor of the signal increases, the average supply voltage applied to the PA decreases. It induces a low average gain so that the overall power-added efficiency (PAE) is reduced. Moreover, the relatively large knee voltage portion results in low efficiency. The simulation results of the PA with various supply voltage show that there is about an 18% drop of PAE and more than 3-dB degradation of the gain at the average operation point for the 10-dB crest factor signal, as illustrated in Fig. 2. The disadvantage is not just applicable to the PA. The supply modulator similarly suffers from it. The increased crest factor means the lower average output power with the same static power consumption. This directly leads to the efficiency degradation of the supply modulator.

In addition, although the crest factor of the signal is increased from 3–5 to 8–12 dB, the modern wireless communication system requests the same average output power to utilize the existing network resource. It requests higher peak output power for the PA. For example, to generate the average output power of 24 dBm for the 10-dB crest factor signal, the PA should

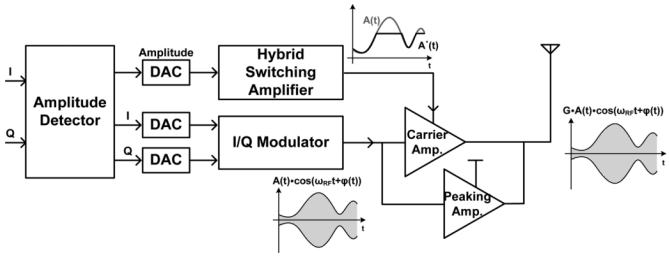

Fig. 3. Block diagram of the proposed ET transmitter with linear Doherty PA.

be designed to provide the peak output power of 34 dBm. Considering that the supply modulator sees the PA as a load, the impedance seen by the supply modulator can be calculated as follows:

$$Z_{\text{Load}} = \frac{V_{CC}}{I_{\text{Load}}/\eta_{\text{pa}}}. \tag{2}$$

For the PA with 50% PAE at 3 V, the load impedance of the supply modulator is about 1.8 Ω. It is not easy to design the supply modulator driving such a low load impedance. To deliver the full-range envelope signal, the final buffer stage should be large enough, requiring large current to drive the large input capacitance of the buffer. Finally, the static current of the linear amplifier increases. It also corresponds to the switching stage of the hybrid switching amplifier. For a large switcher, whose size is optimized to minimize the overall loss, more gate driving stages are required. It increases the loop delay and the static power consumption of the switching stage. There is also a layout issue with more parasitics by routing and the chip size is usually very large. That is, as the crest factor increases, it is hard to achieve the high efficiency and linearity for the ET/EER architecture.

B. Concept of ET Doherty PA

To overcome the limitation of the general EER transmitter mentioned above, the ET transmitter employing a Doherty amplifier is proposed as shown in Fig. 3. The Doherty amplifier is composed of the carrier amplifier and the peaking amplifier. For its load modulation characteristic, the peaking amplifier is turned off at a low-power region, while the carrier amplifier operates with $2R_{\text{opt}}$ impedance. In this work, the supply voltage of the carrier amplifier operating in this low-power region is modulated according to the envelope signal. When the peaking amplifier starts to be turned on, the supply voltage applied to the carrier amplifier maintains the peak voltage of 3 V.

The envelope shaping function for the Doherty amplifier is illustrated in Fig. 4. From the average power backoff level of 0–6 dB, the envelope signal is clipped at 3 V, reducing the crest factor of the envelope signal applied to the carrier amplifier. For its reduced crest factor, the efficiency of the supply modulator is dramatically increased, as shown in Fig. 5. Compared with the efficiency of the supply modulator delivering the original envelope signal, over the broad output power range, more than 15% of the efficiency is improved at the same power backoff level from the maximum average output power. This clipped envelope signal increases not only the efficiency of the supply modulator, but also that of the PA. The crest factor reduction means

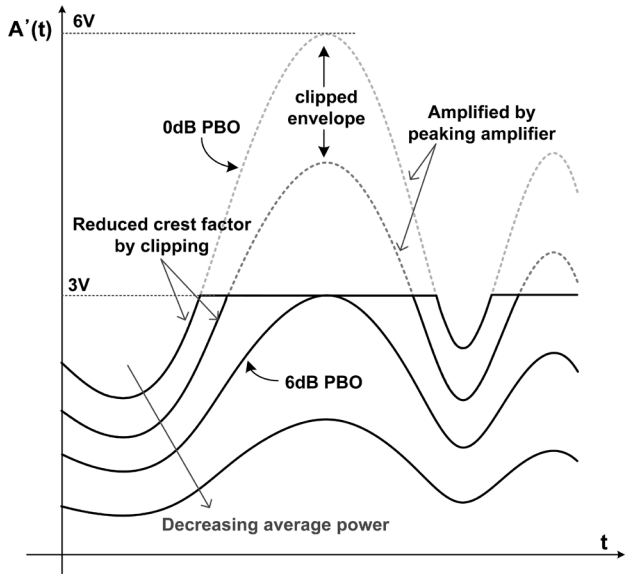

Fig. 4. Time-domain supply voltage waveforms applied to the carrier amplifier at various average output power levels. From the peak power level to the 6-dB backoff power level, the supply voltage waveform is clipped to 3 V so that the crest factor of the envelope signal controlling the supply voltage of the carrier amplifier is significantly reduced. It results in high efficiency of the supply modulator inducing the improvement of the overall PAE, as well as extending the power efficient dynamic range.

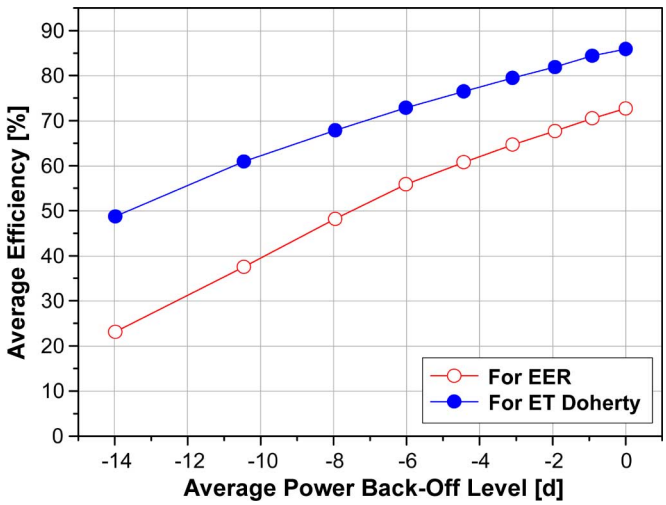

Fig. 5. Simulated efficiencies of the supply modulator for the WiBro system. For the same power backoff level from the maximum average output power, the supply modulator for the Doherty PA presents significantly higher efficiency than that for the EER.

the higher average supply voltage applied to the PA, resulting in a lower gain drop and less effect of the knee voltage; thus, less degradation of the PA efficiency. That is, this modulation shaping makes the PA operate with higher efficiency than the PA in the conventional EER transmitter employing nonclipped envelope signal. Moreover, as the carrier amplifier operates with $2R_{\text{opt}}$ load impedance, it delivers higher efficiency than the conventional supply modulated PA operating with R_{opt}. Therefore, the ET Doherty amplifier presents very high efficiency by the increased average supply voltage, $2R_{\text{opt}}$ load modulation, and the higher efficiency of the supply modulator. The efficiencies of the conventional EER transmitter, Doherty amplifier, and ET

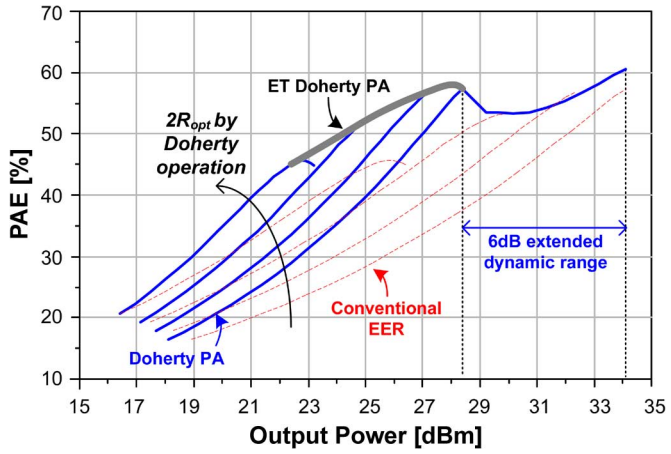

Fig. 6. Efficiency of the ET Doherty PA. Compared to the conventional EER transmitter, it has an extended dynamic range and higher PAE at a low output power region by Doherty operation. This simulation is performed with two PA cells used in Fig. 2.

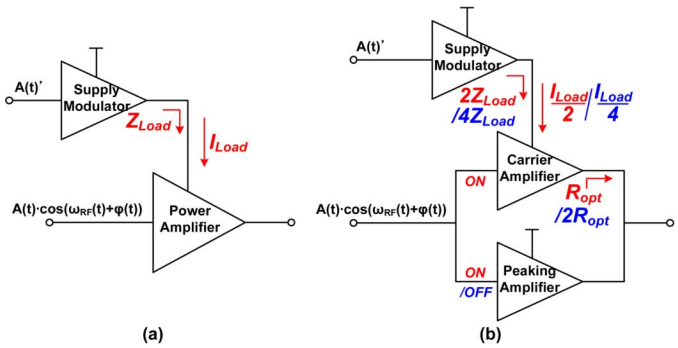

Fig. 7. Load impedances seen by the supply modulator. (a) General polar transmitter. (b) Polar transmitter with Doherty amplifier in a $R_{\rm opt}$ and $2R_{\rm opt}$ operation.

Doherty amplifier are illustrated in Fig. 6. Note that, as the ET Doherty amplifier employs both concepts of ET and Doherty together, the proposed solution becomes an alternative solution for the next-generation communication system.

For the output power control of the mobile handset applications, the peak voltage of the envelope signal applied to the PA is changed from 3 V. When it is backed off by 6 dB from the peak power level, the operation of the proposed ET transmitter becomes similar to the general EER transmitter, in which the supply modulator delivers the full range of the envelope signal to the PA, herein the carrier amplifier (refer to Fig. 4). In other words, the ET Doherty amplifier has a 6-dB extended dynamic range compared with the general EER transmitter, as described in Fig. 6.

In addition, for the Doherty amplifier, the required dc current for the PA is reduced to a half for each amplifier, as shown in Fig. 7. It results in two times larger load impedance of 3.6 Ω at the $R_{\rm opt}$ operation, and at the $2R_{\rm opt}$ operation, the load impedance is increased to 7.2 Ω. That is, with the Doherty amplifier, it is easier to design the supply modulator for the polar transmitter generating a high output power. In the hybrid switching amplifier, the required sizes for the class-AB buffer and the power switch are reduced to a half. Considering these two parts occupy most of the layout, the chip size of the supply modulator is reduced to half.

III. Circuit Implementations

The overall schematic of the proposed ET transmitter is illustrated in Fig. 8. It employs the Doherty amplifier and hybrid switching amplifier as a supply modulator to achieve high efficiency and linearity at the same time. In this section, the detailed design of each block is covered at the circuit level.

A. Class-AB/F Doherty Amplifier

The Doherty amplifier presented here is based on the design described in [17]. It employs the harmonic loading circuit to improve the efficiency of the amplifier without deteriorating the linearity [14]–[16]. It presents more efficiency over the broad output power compared to the general Doherty amplifier employing class-AB/F unit PA cells. In this work, the harmonic tuned Doherty amplifier is designed to operate with 3-V supply voltage considering the voltage drop by the supply modulator, whose supply is directly coupled to a 3.4-V battery. The designed Doherty PA delivers a PAE of 51% at the peak output power of 34 dBm with a gain of more than 25 dB. At the 6-dB backed-off power, it shows 45% PAE. It presents an acceptable linearity with third-order intermodulation distortion (IMD3) of −28 dBc below the output power of 30 dBm. For the supply modulator, the carrier amplifier is seen as the equivalent impedance of 3.6 Ω at the $R_{\rm opt}$ operation and 7.2 Ω at the $2R_{\rm opt}$ operation.

B. Hybrid Switching Amplifier

1) Linear Amplifier: The linear amplifier is composed of the transconductance amplifier (OTA), the class-AB bias circuit, and the output buffer. The important design parameter for the OTA is a large gain bandwidth (GBW) product within the limited dc power consumption. The class-AB OTA with the local common mode feedback (LCMFB) shown in Fig. 9 is employed for its high slew rate and large GBW characteristics compared with other topologies [20]. The common-source type output buffer is employed for the rail-to-rail operation, high current drive ability, and low quiescent current. The size of transistors in the buffer is determined by considering the current driving capability and the voltage drop across them, 16560 μm × 0.3 μm for PMOS and 8280 μm × 0.35 μm for NMOS. It can deliver more than 840 mA to the 3.6-Ω load impedance. Based on the general output voltage swing of the conventional digital-to-analog converter, 0–1 V, the voltage gain of the designed class-AB buffered linear amplifier is set to 3 V/V for the maximum output voltage of 3 V. The worst case bandwidth is about 40 MHz. The additional drive stage for the voltage amplification is not required. The power consumption is 13.2 mW at the idle condition.

2) Current Sensing Unit: In the hybrid switching amplifier, the linear amplifier and switching amplifier are in the master–slave relationship. That is, according to the magnitude and polarity of the current from the linear amplifier, the amount of current from the switching amplifier is determined. Usually, the current sensing is performed through a series sensing

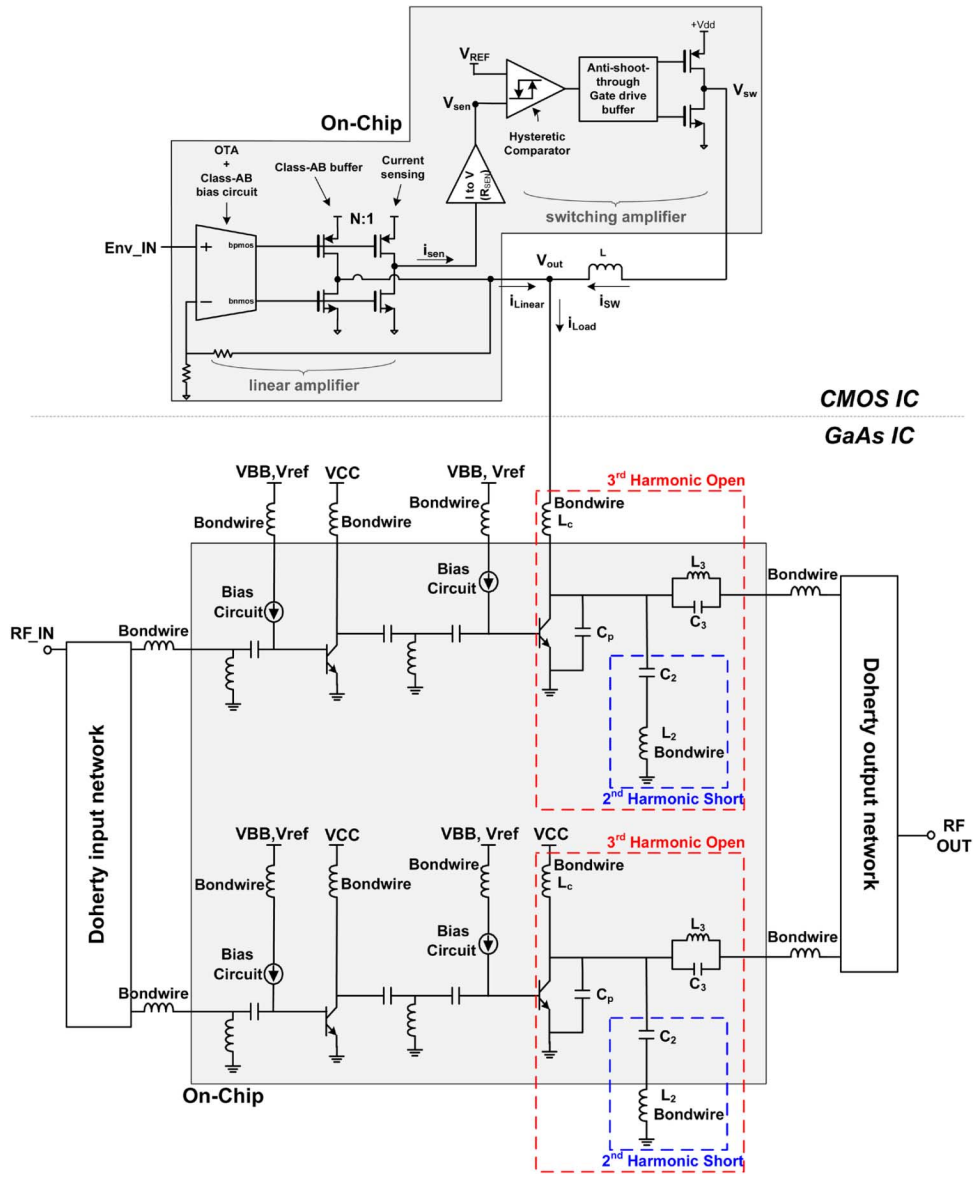

Fig. 8. Schematic of the implemented ET Doherty PA.

resistor whose magnitude is much smaller than the $R_{\rm Load}$ for a low loss. However, this is not a good solution in the integrated circuit technology, in which it is hard to implement the very small resistor in the order of 10 mΩ. Instead of this lossy resistor, the current mirroring technique is employed [21]. It is realized by a matched PMOS and NMOS transistor with N times smaller than that of transistors in the buffer. The scaling downed mirror current is converted to the voltage through the resistor $R_{\rm sen}$ and it is applied to the comparator.

3) Hysteretic Comparator: The schematic of a hysteretic comparator is shown in Fig. 10. It consists of a source-coupled differential pair with positive feedback and a differential-to-single-ended converter. This circuit behaves differently according to the magnitude of positive feedback factor α, which is given by

$$\alpha = \frac{(W/L)_{5,6}}{(W/L)_{3,4}}. \tag{3}$$

With $\alpha > 1$, it behaves as a hysteretic comparator. When it operates as a hysteretic comparator, the positive and negative trip points are equal to

$$V_{TRP\pm} = \pm\sqrt{\frac{2I_{\rm BIAS}}{k'_p(W/L)_{1,2}}}\frac{\sqrt{\alpha}-1}{\sqrt{1+\alpha}} \tag{4}$$

where $k'_p = \mu_p C_{\rm OX}$ is the process transconductance parameter of the pMOS. The designed comparator consumes less than 2.5 mW on the operation of the supply modulator.

4) Switching Amplifier With Low-Loss Gate Driver: The size of the power switch is determined by considering the conduction loss and the switching loss at the specific load impedance, switching frequency, and duty ratio. The average duty ratio depends on the crest factor of the input signal. The shaped envelope signal shows the crest factor of 4 dB so that the average duty ratio is about 63%. The size of PMOS is 42840 μm $\times$ 0.3 μm and the size of NMOS is 20400 μm $\times$ 0.35 μm. After deciding the size of the power switch, the gate driver is designed

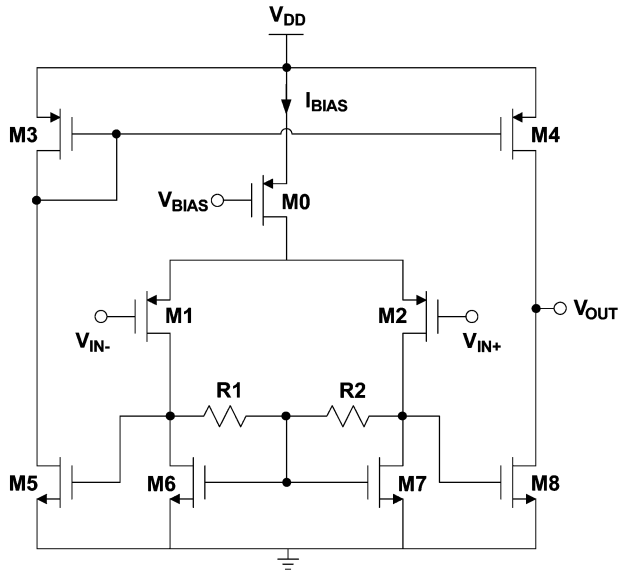

Fig. 9. Class-AB OTA with LCMFB.

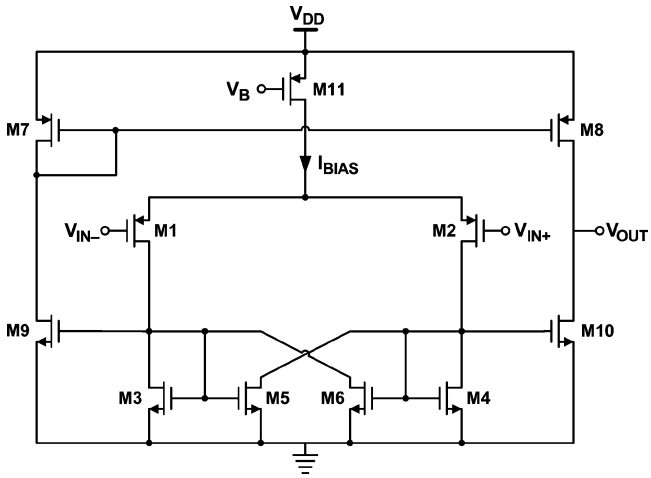

Fig. 10. Hysteretic comparator.

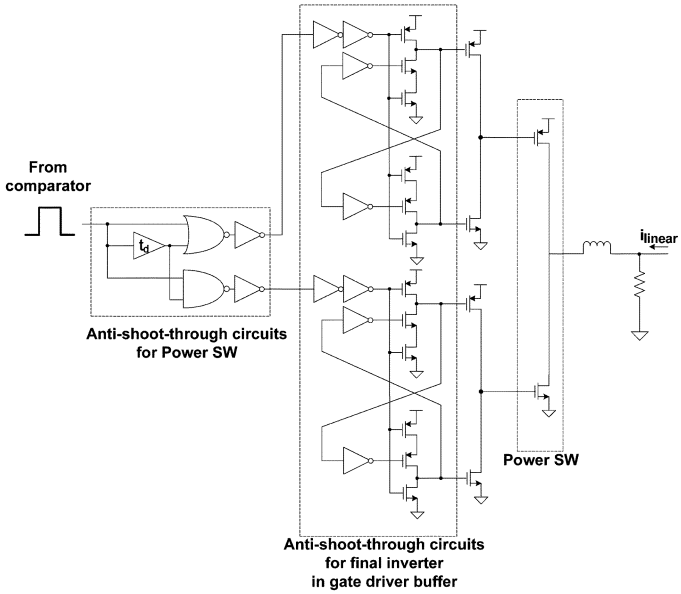

Fig. 11. Buck converter with gate driver.

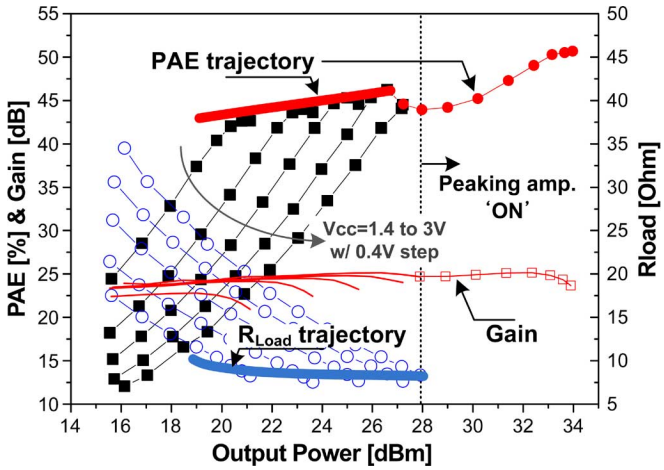

Fig. 12. Measured performance of the fabricated Doherty PA with various supply voltage.

to switch them appropriately. The tapering ratio of 8 is determined through the tradeoff between the propagation delay and the power loss through the multiple drive stages. To protect the device, the conventional antishoot-through circuit is employed. It also has an effect of reducing the power loss by the short-circuit current. Considering the large size of the power switch and the tapering ratio, the additional antishoot-through circuit in [22] is added for the final inverter in the gate driver buffer so that the switching loss in the gate driver is minimized. At the idle condition, which means the highest switching frequency of 7.5 MHz, the switching amplifier including the gate driver draws only 0.7 mA. The schematic of the designed switching amplifier with the low-loss gate driver is shown in Fig. 11.

IV. Experimental Results

The proposed polar transmitter is fabricated with an InGaP/GaAs 2-μm HBT process for the class-AB/F Doherty PA and a CMOS 0.13-μm process for the supply modulator with 3.3-V compatible devices. The unit PA cell is integrated on a chip, except two capacitors. The Doherty PA combines two-unit class-AB/F PAs with the input dividing and output combining circuits. For the supply modulator, every single element in the circuit is fully integrated on a chip, except the 4.7-μH inductor.

The fabricated class-AB/F Doherty PA delivers 34-dBm output power with 25 dB of gain at 3-V dc supply voltage. It presents a PAE of 51% at the peak power, while the efficiency at the 6-dB backed-off power is about 45%. The supply voltage of the carrier amplifier is swept from 1.4 to 3 V, as shown in Fig. 12. The PAE changes from 40% to 45%, while the load impedance seen by the supply modulator is nearly 7 Ω. Under the supply modulated operation, the PAE curve follows the peak PAE points, while the R_{Load} follows the lowest R_{Load} points. As the peaking amplifier is turned on, the supply voltage of the carrier amplifier is fixed to 3 V, similar to the general Doherty PA. The measured efficiency of the implemented supply modulator with various load impedances is shown in Fig. 13.

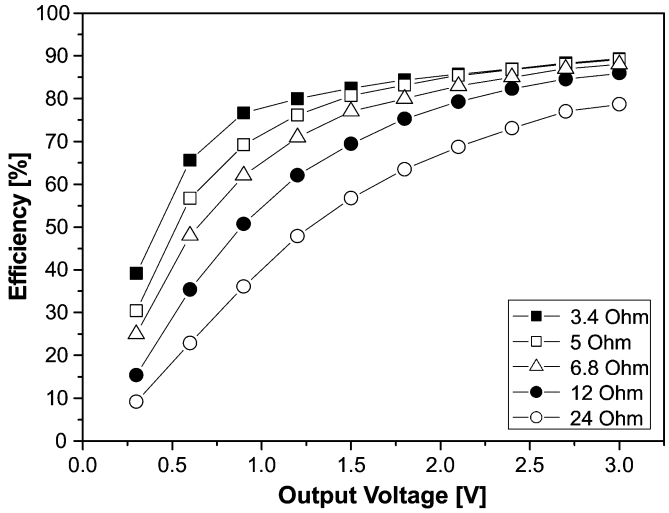

Fig. 13. Measured efficiency of the supply modulator with various load impedances.

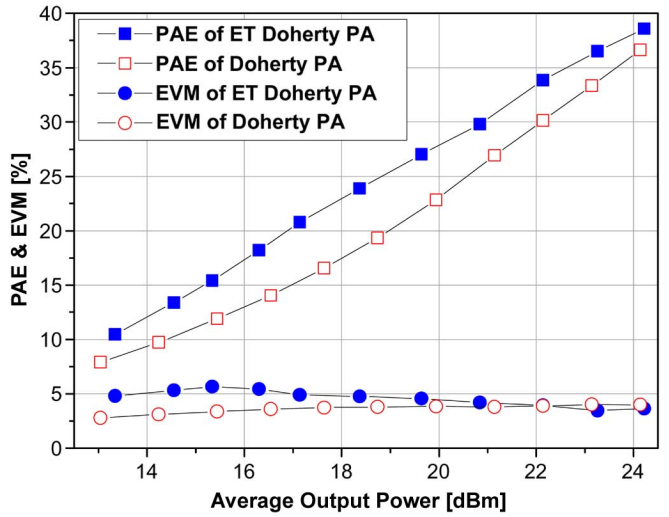

Fig. 14. Measured performance of the ET Doherty PA for 10.75-dB crest factor 5-MHz bandwidth WiBro. The PAE of Doherty PA itself is very high and the supply modulation enhances the PAE further.

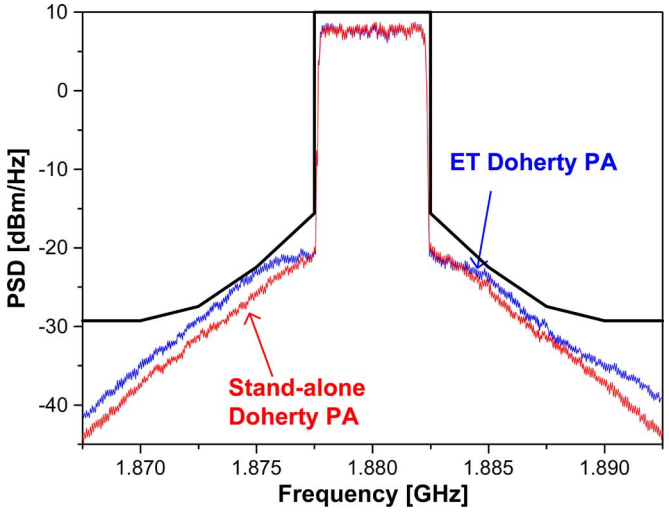

Fig. 15. Measured output spectra of the ET Doherty PA for 10.75-dB crest factor 5-MHz bandwidth WiBro.

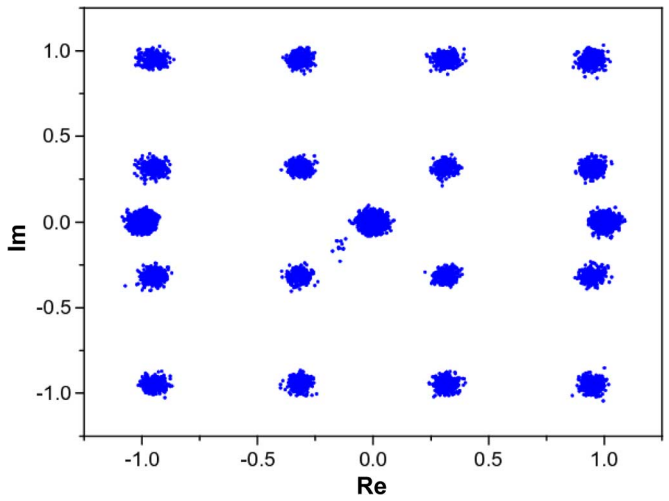

Fig. 16. Measured constellation of the ET Doherty PA for 10.75-dB crest factor 5-MHz bandwidth WiBro. The measured EVM is 3.64%, while the specification requests the EVM of 7.5%.

For the 10.75-dB crest factor and 5-MHz bandwidth WiBro signal, the designed polar transmitter presents a PAE of 38.6% at the output power of 24.22 dBm with a gain of 24.62 dB, while the standalone class-F Doherty PA shows a PAE of 36.6% at the same output power with a gain of 25.6 dB. Over the broad output power range, the PAE of the polar transmitter with Doherty PA is significantly improved, as shown in Fig. 14. It proves that the polar transmitter employing Doherty amplifier is very advantageous for the mobile handset application, which requires a wide dynamic range with high efficiency. There is a little spectral degradation of the linearity by the supply modulation of the carrier amplifier, as shown in Fig. 15. It is measured at the maximum average output power of 24.22 dBm. The constellation diagram at that power level is presented in Fig. 16. The measured error vector magnitude (EVM) is 3.64% and does not exceed the specification of 7.5% over the broad output power range for the WiBro 16 quadrature amplitude modulation (16–QAM) signal. The increment of EVM at the low output power comes from the switching noise of the supply modulator. It can be simply solved by employing the low switching noise technique [23].

V. Conclusions

We have designed a highly efficient and linear ET Doherty PA to boost up the efficiency over the extended dynamic range. By modulating only the carrier amplifier, the effect of the supply modulation occurs below the 6-dB power backoff region, resulting in higher efficiency for a high crest factor signal. It also reduces the current provided to the PA and results in the reduced chip size of the supply modulator. The fabricated ET Doherty PA is composed of the class-AB/F HBT Doherty PA and the CMOS hybrid switching amplifier. It presents a significant improvement of the efficiency over the broad output power region. Especially at the 16-dB power backoff region, the PAE is more than 23%. It is important for the real operation environment since the handset is usually operated at the low-power level. For 10.75-dB crest factor 5-MHz WiBro application, the overall ET Doherty PA shows a PAE of 38.6% at the output power of 24.22 dBm with a gain of 24.62 dB. The measured EVM at that power is 3.64%.

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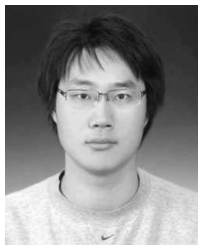

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